

Power Factor Correction Controller

FAN7527B

Description

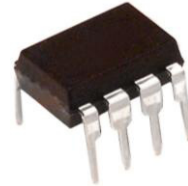
The FAN7527B provides simple and high-performance active Power Factor Correction (PFC). The FAN7527B is optimized for electronic ballasts and low-power, high-density power supplies that require minimum board size, reduced external components, and low power dissipation. Because the R/C filter is included in the current-sense block, an external R/C filter is not necessary. Special circuitry prevents no-load runaway conditions. Regardless of the supply voltage, the output drive clamping circuit limits the overshoot of the power MOSFET gate drive, which improves system reliability.

Features

- Internal Startup Timer
- Internal R/C Filter Eliminates the Need for External R/C Filter
- Precise Adjustable Output Over-Voltage Protection
- Zero Current Detector
- One Quadrant Multiplier
- Trimmed 1.5% Internal Band Gap Reference
- Under-Voltage Lockout with 3 V of Hysteresis
- Totem-Pole Output with High-State Clamp
- Low Startup and Operating Current
- 8-Pin SOP or 8-Pin DIP
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Electronic Ballast
- SMPS

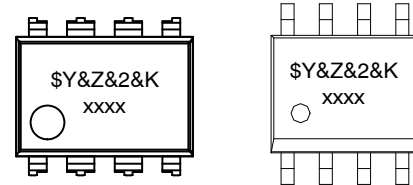


PDIP8 9.42x6.38, 2.54P
CASE 646CM



SOIC8
CASE 751EB

MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = Lot Run Traceability Code
- xxxx = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FAN7527BN	PDIP8 (Pb-Free)	3000 / Tube
FAN7527BMX	SOIC8 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

NOTE: Operating Temperature Range of both devices is -25 to +125°C

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BLOCK DIAGRAM

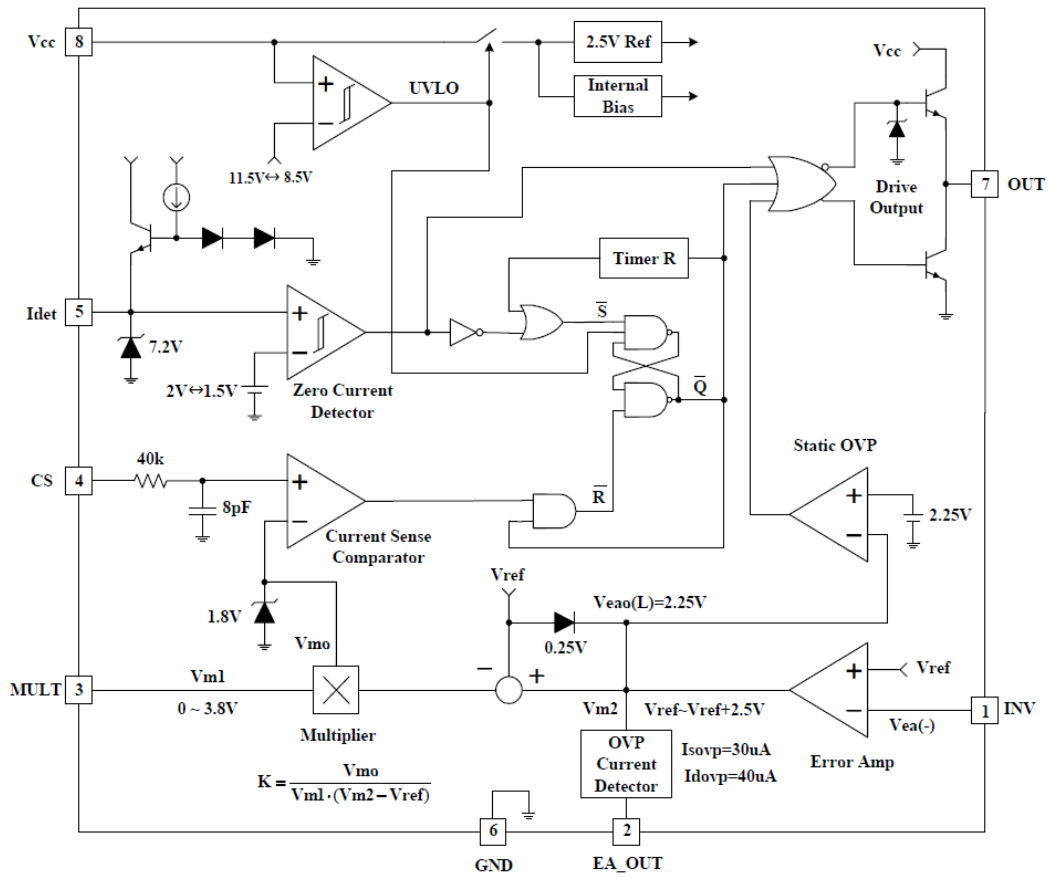


Figure 1. Block Diagram

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PIN CONFIGURATION

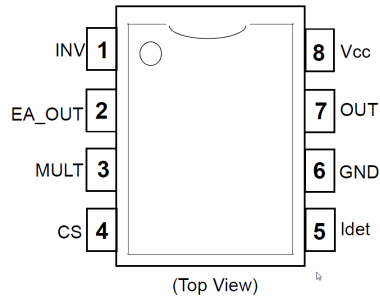


Figure 2. Pin Configuration

PIN DEFINITIONS

Pin #	Name	Description
1	INV	Inverting input of the error amplifier. The output of the boost converter should be resistively divided to 2.5 V and connected to this pin.
2	EA_OUT	Output of the error amplifier. Feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input to the multiplier stage. The full-wave rectified AC voltage is divided to less than 2 V and is connected to this pin.
4	CS	Input of the PWM comparator. The MOSFET current is sensed by a resistor and the resulting voltage is applied to this pin. An internal R/C filter is included to reject high-frequency noise
5	Idet	Zero Current Detection (ZCD) input
6	GND	Ground
7	OUT	Gate driver output. Push-pull output stage is able to drive the power MOSFET with a peak current of 500 mA
8	V _{CC}	Supply voltage of driver and control circuits

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage		30	V
I _{OH} , I _{OL}	Peak Drive Output Current		±500	mA
I _{CLAMP}	Driver Output Clamping Diodes V _O > V _{CC} or V _O < -0.3 V		±10	mA
I _{DET}	Detector Clamping Diodes		±10	mA
V _{IN}	Error Amplifier Multiplier and Comparator Input Voltages	-0.3	6.0	V
T _J	Operation Junction Temperature		+150	°C
T _{OPR}	Operating Temperature Range	-25	+125	°C
T _{STG}	Storage Temperature Range	-65	+150	°C
P _D	Power Dissipation	SOIC8	0.8	W
		PDIP8	1.1	W
Θ _{JA}	Thermal Resistance Junction–Ambient	SOIC8	150	°C/W
		PDIP8	110	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

TEMPERATURE CHARACTERISTICS

(-25°C ≤ T_A ≤ 125°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔV _{REF}	Temperature Stability Reference Voltage (V _{REF})		20		mV
ΔK/ΔT	Temperature Stability for Multiplier Gain (K)		-0.2		% / °C

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ELECTRICAL CHARACTERISTICS

($V_{CC} = 14\text{ V}$, $-25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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UNDER-VOLTAGE LOCKOUT

$V_{th(st)}$	Start Threshold Voltage	V_{CC} Increasing	10.5	11.5	12.5	V
$H_{Y(st)}$	UVLO Hysteresis		2	3	4	V

SUPPLY CURRENT SECTION

I_{ST}	Startup Supply Current	$V_{CC} = V_{th(st)} - 0.2\text{ V}$	10	60	100	μA
I_{CC}	Operating Supply Current	Output Not Switching		3	6	mA
$I_{CC(OVP)}$	Operating Current at OVP	$V_{INV} = 3\text{ V}$		1.7	4.0	mA
I_{DCC}	Dynamic Operating Supply Current	50 kHz, $C_I = 1\text{ nF}$		4	8	mA

ERROR AMPLIFIER SECTION

V_{REF}	Voltage Feedback Input Threshold	$I_{REF} = 0\text{ mA}$, $T_A = 25^{\circ}\text{C}$	2.465	2.500	2.535	V
		$25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	2.440	2.500	2.560	
ΔV_{FEF1}	Line Regulation	$14\text{ V} \leq V_{CC} \leq 25\text{ V}$		0.1	10.0	mV
ΔV_{FEF3}	Temperature Stability of V_{REF} (Note 1)	$-25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		20		mV
$I_{b(ea)}$	Input Bias Current		-0.5		0.5	μA
I_{SOURCE}	Output Source Current	$V_{M2} = 4\text{ V}$	-2	-4		mA
I_{SINK}	Output Sink Current	$V_{M2} = 4\text{ V}$	2	4		mA
$V_{EAO(H)}$	Output Upper Clamp Voltage (Note 1)	$I_{SOURCE} = 0.1\text{ mA}$		6		V
$V_{EAO(L)}$	Output Lower Clamp Voltage (Note 1)	$I_{SINK} = 0.1\text{ mA}$		2.25		V
G_V	Large Signal Open-Loop Gain (Note 1)		60	80		dB
PSRR	Power Supply Rejection Ratio (Note 1)	$14\text{ V} \leq V_{CC} \leq 25\text{ V}$	60	80		dB
GBW	Unity Gain Bandwidth (Note 1)			1		MHz
SR	Slew Rate (Note 1)			0.6		V/ μs

MULTIPLIER SECTION

$I_{b(m)}$	Input Bias Current (Pin 3)		-0.5		0.5	μA
ΔV_{M1}	M1 Input Voltage Range (Pin 3)				3.8	V
ΔV_{M2}	M2 Input Voltage Range (Pin 2)		V_{REF}		$V_{REF} + 2.5$	V
K	Multiplier Gain (Note 1)	$V_{M1} = 1\text{ V}$, $V_{M2} = 3.5\text{ V}$	0.36	0.44	0.52	1 / V
$V_{OMAX(m)}$	Maximum Multiplier Output Voltage	$V_{INV} = 0\text{ V}$, $V_{M1} = 4\text{ V}$	1.65	1.80	1.95	V
$\Delta K/\Delta T$	Temperature Stability of K (Note 1)	$-25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		-0.2		% / $^{\circ}\text{C}$

CURRENT SENSE SECTION

$V_{IO(CS)}$	Input Offset Voltage (Note 1)	$V_{M1} = 0\text{ V}$, $V_{M2} = 2.2\text{ V}$	-10	3	10	mV
$I_{b(CS)}$	Input Bias Current	$0\text{ V} \leq V_{CS} \leq 1.7\text{ V}$	-1.0	-0.1	1.0	μA
$t_{D(CS)}$	Current Sense Delay to Output (Note 1)			200	500	ns

ZERO CURRENT DETECT SECTION

$V_{TH(DET)}$	Input Voltage Threshold	V_{DET} Increasing	1.7	2.0	2.3	V
$H_{Y(DET)}$	Detect Hysteresis		0.2	0.5	0.8	V
$V_{CLAMP(L)}$	Input Low Clamp Voltage	$I_{DET} = -100\text{ }\mu\text{A}$	0.45	0.75	1.00	V
$V_{CLAMP(H)}$	Input High Clamp Voltage	$I_{DET} = 3\text{ mA}$	6.5	7.2	7.9	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 14\text{ V}$, $-25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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ZERO CURRENT DETECT SECTION

$I_{b(DET)}$	Input Bias Current	$1\text{ V} \leq V_{DET} \leq 5\text{ V}$	-1.0	-0.1	1.0	μA
$I_{CLAMP(D)}$	Input High/Low Clamp Diode Current (Note 1)				± 3	mA

OUTPUT SECTION

V_{OH}	Output Voltage High	$I_O = -10\text{ mA}$	10.5	11.0		V
V_{OL}	Output Voltage Low	$I_O = 10\text{ mA}$		0.8	1.0	V
t_R	Rising Time (Note 1)	$C_L = 1\text{ nF}$		130	200	ns
t_F	Falling Time (Note 1)	$C_L = 1\text{ nF}$		50	120	ns
$V_{OMAX(O)}$	Maximum Output Voltage	$V_{CC} = 20\text{ V}$, $I_O = 100\ \mu\text{A}$	12	14	16	V
$V_{OMIN(O)}$	Output Voltage with UVLO Activated	$V_{CC} = 5\text{ V}$, $I_O = 100\ \mu\text{A}$			1	V

RESTART TIMER SECTION

$t_{D(RST)}$	Restart Time Delay	$V_{M1} = 1\text{ V}$, $V_{M2} = 3.5\text{ V}$		150		μs
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OVER-VOLTAGE PROTECTION SECTION

I_{SOVP}	Soft OVP Detecting Current		25	30	35	μA
I_{DOVP}	Dynamic OVP Detecting Current		35	40	45	μA
V_{OVVP}	Static OVP Threshold Voltage	$V_{INV} = 2.7\text{ V}$	2.10	2.25	2.40	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. These parameters, although guaranteed, are not 100% tested in production.

Multiplier Gain:

$$K = \frac{\text{Pin4_Threshold}}{V_{M1} \times (V_{M2} - V_{REF})}$$

where $V_{M1} = V_{PIN3}$, $V_{M2} = V_{PIN2}$

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TYPICAL PERFORMANCE CHARACTERISTICS

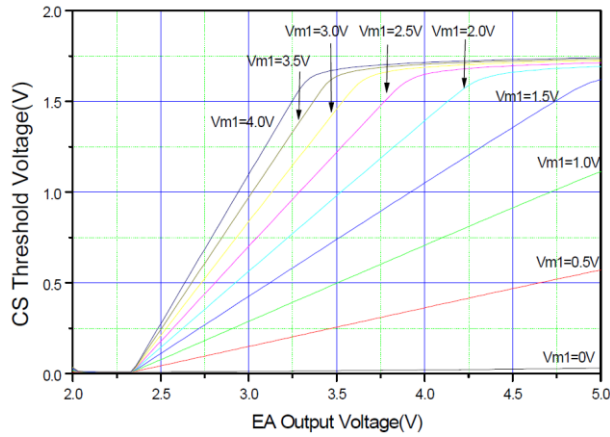


Figure 3. Error Amplifier Output Voltage vs. Current Sensing Threshold

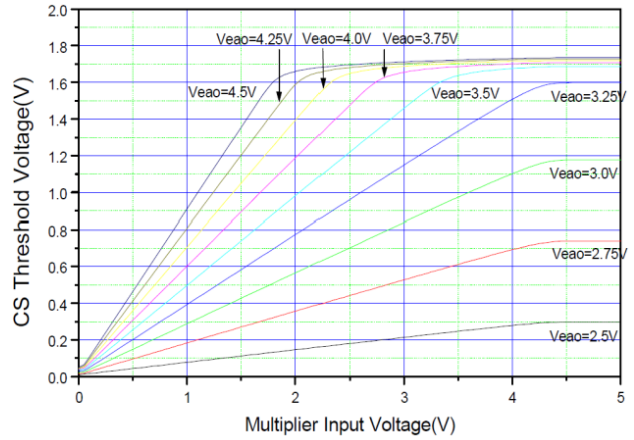


Figure 4. Multiplier Input Voltage vs. Current Sensing Threshold

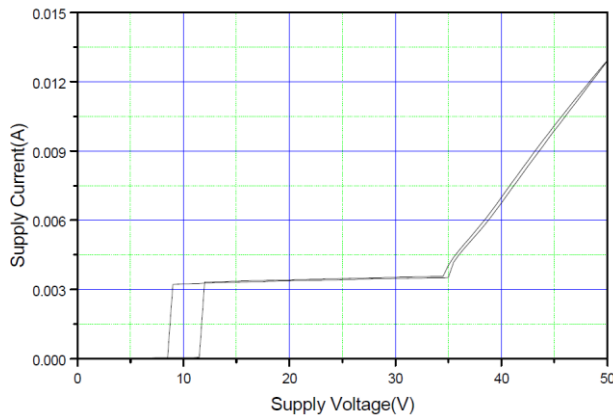


Figure 5. Supply Current vs. Supply Voltage

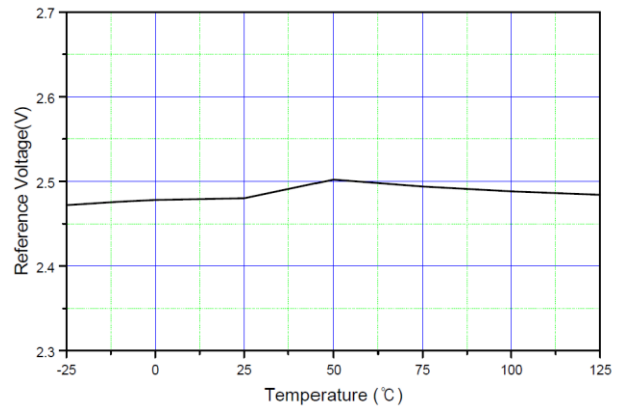


Figure 6. Reference Voltage vs. Temperature

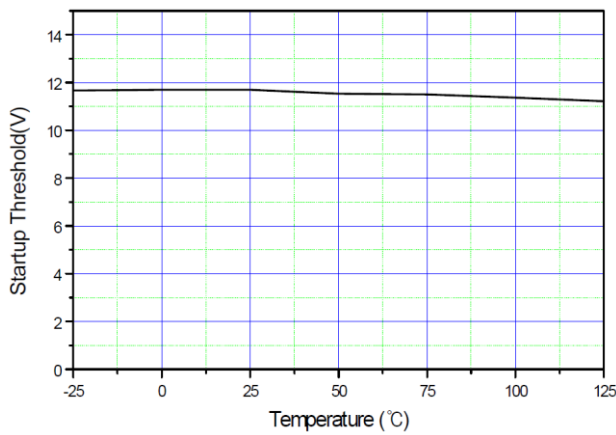


Figure 7. Startup Threshold vs. Temperature

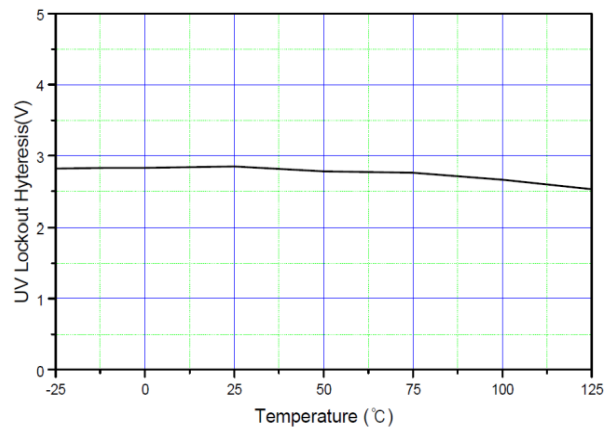


Figure 8. UVLO Hysteresis vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

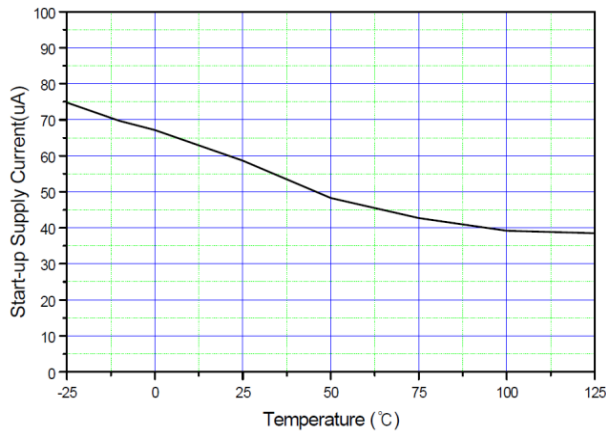


Figure 9. Startup Supply Current vs. Temperature

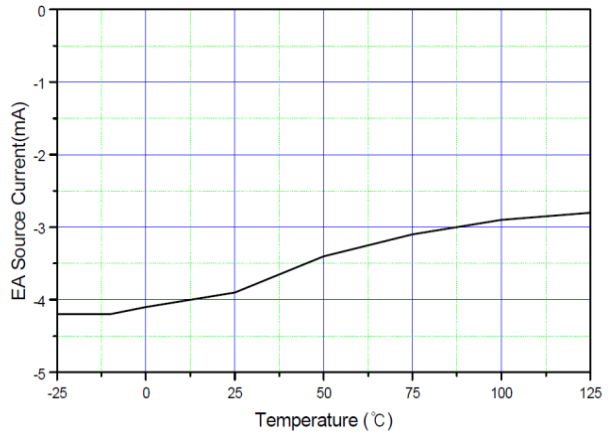


Figure 10. Error Amplifier Source Current

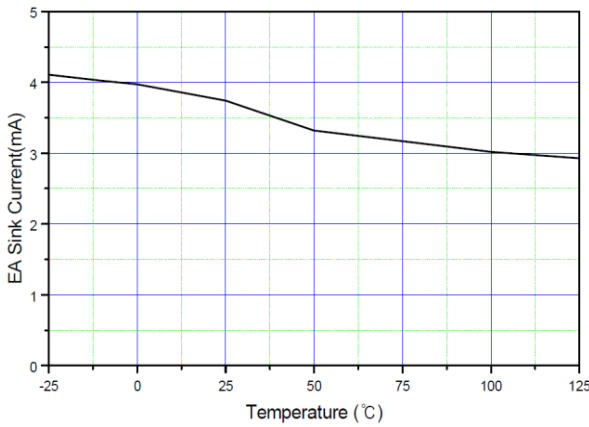


Figure 11. Error Amplifier Sink Current vs. Temperature

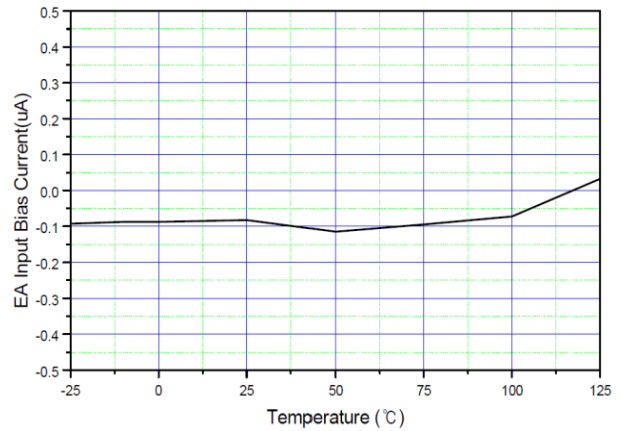


Figure 12. Error Amplifier Input Bias Current vs. Temperature

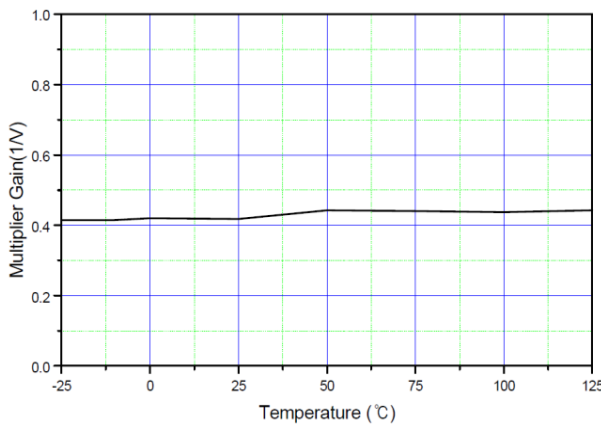


Figure 13. Multiplier Gain vs. Temperature

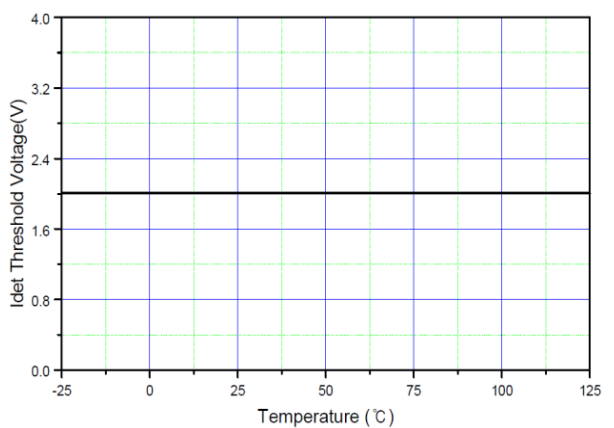


Figure 14. I_{DET} Threshold Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

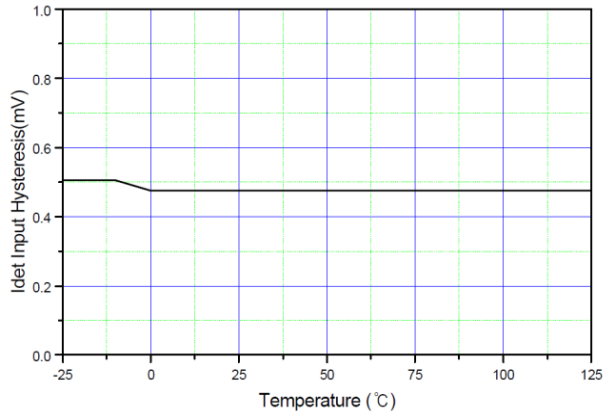


Figure 15. IDET Input Hysteresis vs. Temperature

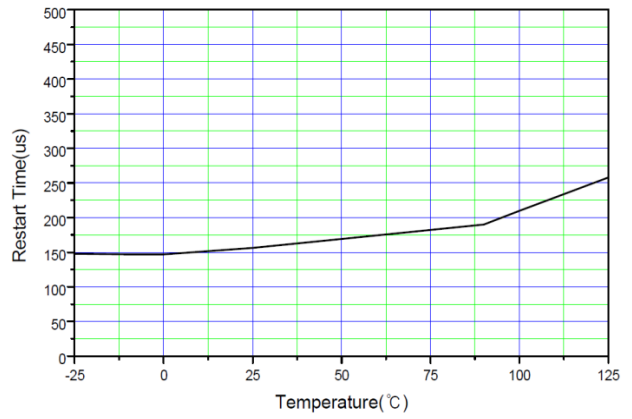


Figure 16. Restart Time vs. Temperature

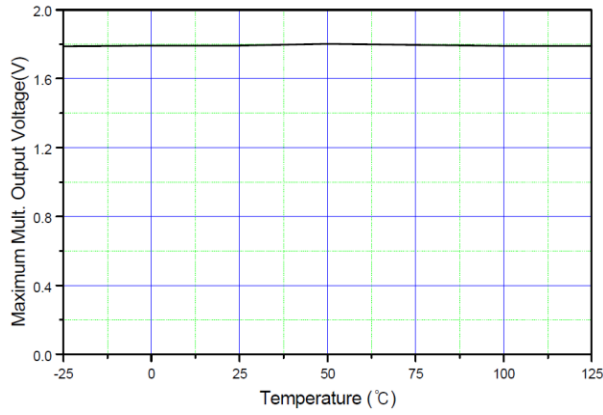


Figure 17. Maximum Multiplier Output Voltage vs. Temperature

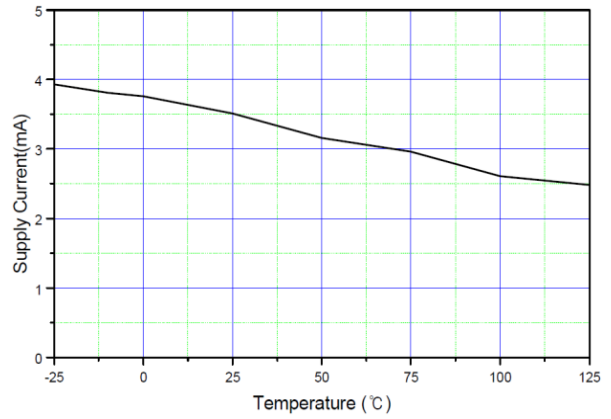
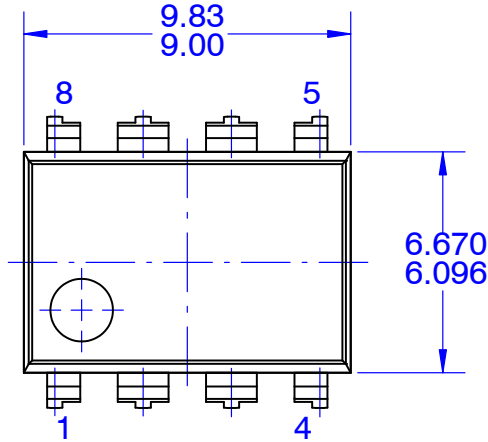


Figure 18. Supply Current vs. Temperature

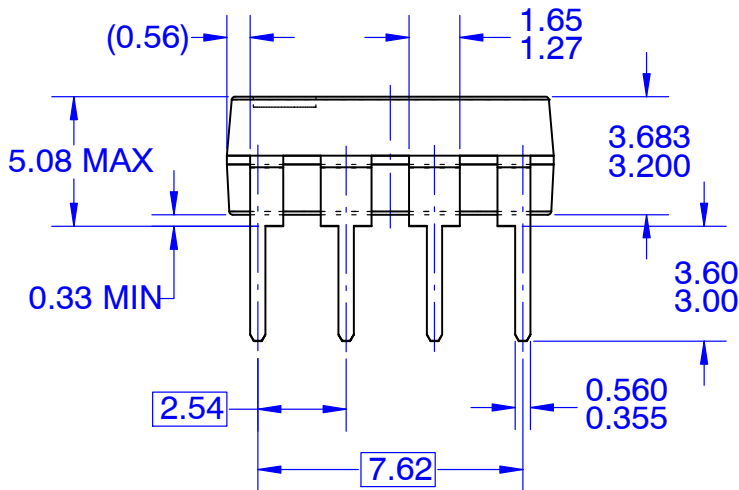
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

PDIP8 9.42x6.38, 2.54P
CASE 646CM
ISSUE O

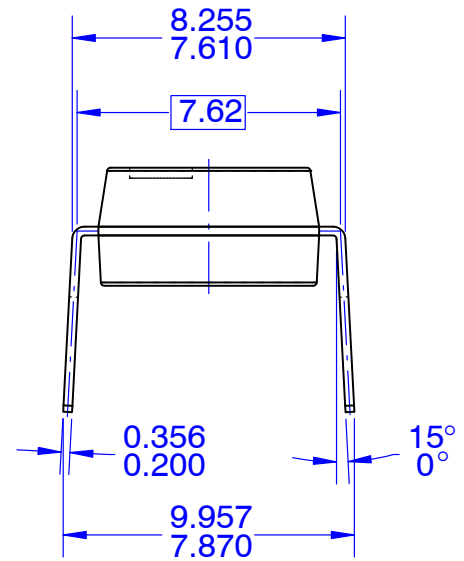
DATE 31 JUL 2016



TOP VIEW



FRONT VIEW




SIDE VIEW

NOTES:

- A. CONFORMS TO JEDEC MS-001, VARIATION BA
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
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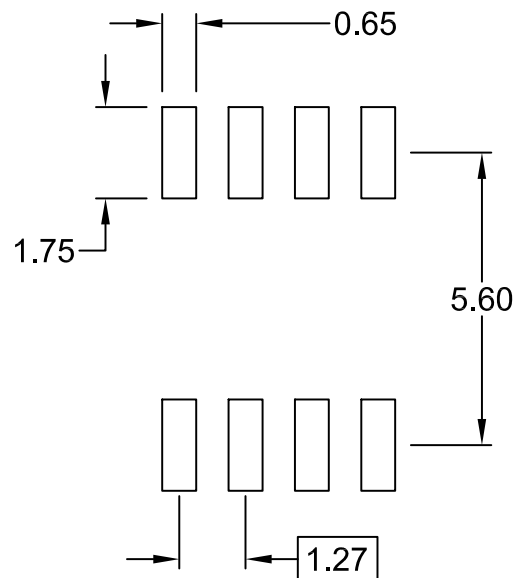
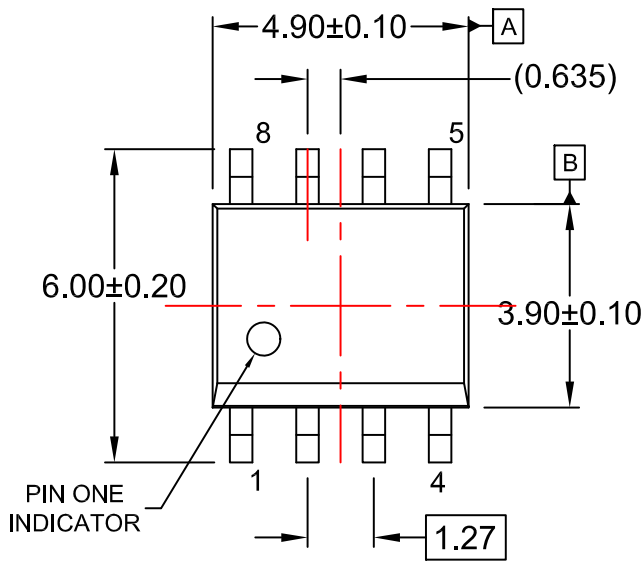
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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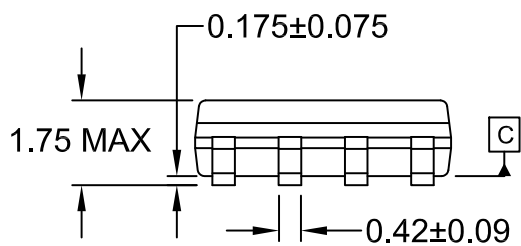


SOIC8
CASE 751EB
ISSUE A

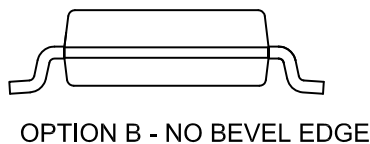
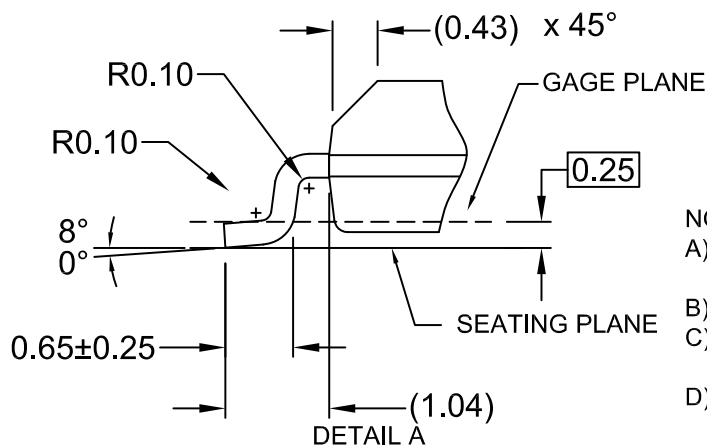
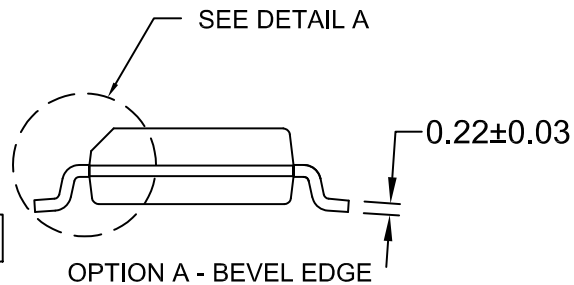
DATE 24 AUG 2017



⊕ 0.25 (M) C B A



⌒ 0.10



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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