TEXAS INSTRUMENTS

THS4601EVM

User's Guide

October 2002 *High Performance Linear Products*

SLOU150

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It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.The input supply voltage ($\pm V_S$) should be $\pm$5 V minimum and no greater than $\pm$15 V. Differential input signal should be no greater than $\pm$4 V. The output current (I_O) should be no greater than 100 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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This is an example of a caution statement.

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A warning statement describes a situation that could potentially cause harm to you.

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Electrostatic Sensitive Components

This EVM contains components that can potentially be damaged by electrostatic discharge, Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an anti-static work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4601 data sheet (literature number SLOS388)
- Application report (literature number SLMA002), *Power Pad Thermally Enhanced Package*, http://www-s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (literature number SLMA004), Power Pad Made Easy, http://www-s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (literature number SSYA008), Electrostatic Discharge (ESD), http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf
- Application report (literature number SLOA102), High Speed PCB Layout Tips, http://www-s.ti.com/sc/psheets/sloa102/sloa102.pdf

Trademarks

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Chapter 1

Introduction and Description

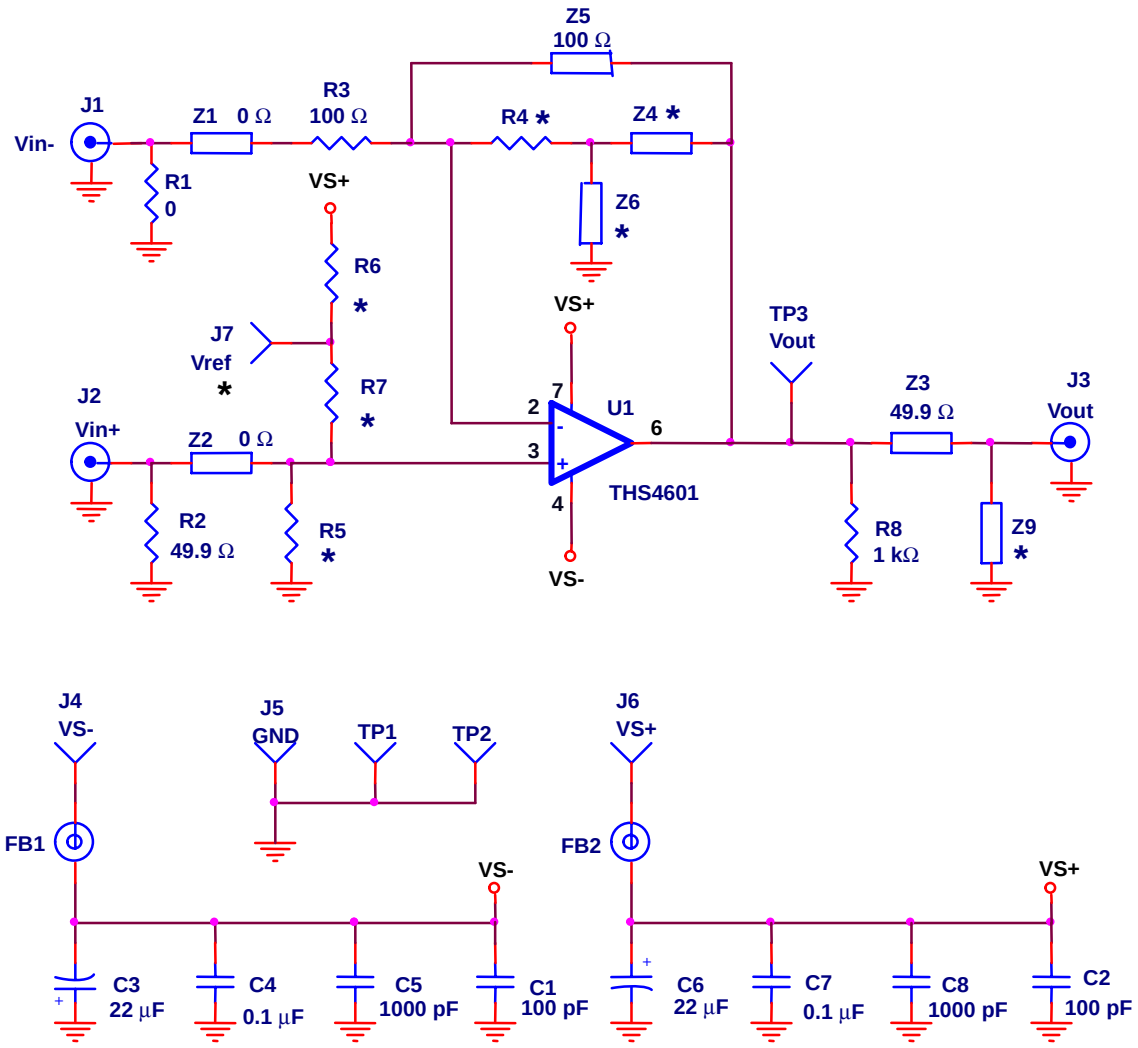
This EVM provides a platform for testing the THS4601 in 8-pin SOIC PowerPAD™ (DDA) package. It contains the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations.

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and monitoring instrument. See Figure 1-1 for a complete schematic diagram. EVM features include:

- ❑ Wide operating supply voltage range: ±5 V to ±15 V operation (see the device data sheet)
- ❑ Inverting and noninverting gain configurations supported
- ❑ Single supply capability—R5 through R7 to provide internal or external reference to the noninverting input
- ❑ Z1 through Z3 for ac coupling
- ❑ Nominal 50-Ω input impedance (R2 or R1). Termination can be configured according to the application requirement.
- ❑ 1-kΩ load resistor R8. 1-kΩ is the standard data sheet load impedance.
- ❑ Footprints for a series resistor (Z3) or an A/D compensation network (Z3 and Z9)
- ❑ T-network in the feedback path can also be used to implement transimpedance networks
- ❑ Power supply ripple rejection capacitors (C3 and C6)
- ❑ Decoupling capacitors (C4, C5, C7, C8, C9, C10)
- ❑ Test point for connection of a high impedance scope probe to op amp output (TP3)
- ❑ Convenient GND test points (TP1 and TP2)
- ❑ PowerPAD heatsinking capability
- ❑ A good example of high-speed amplifier PCB design and layout

Figure 1-1. Schematic of the THS4601EVM



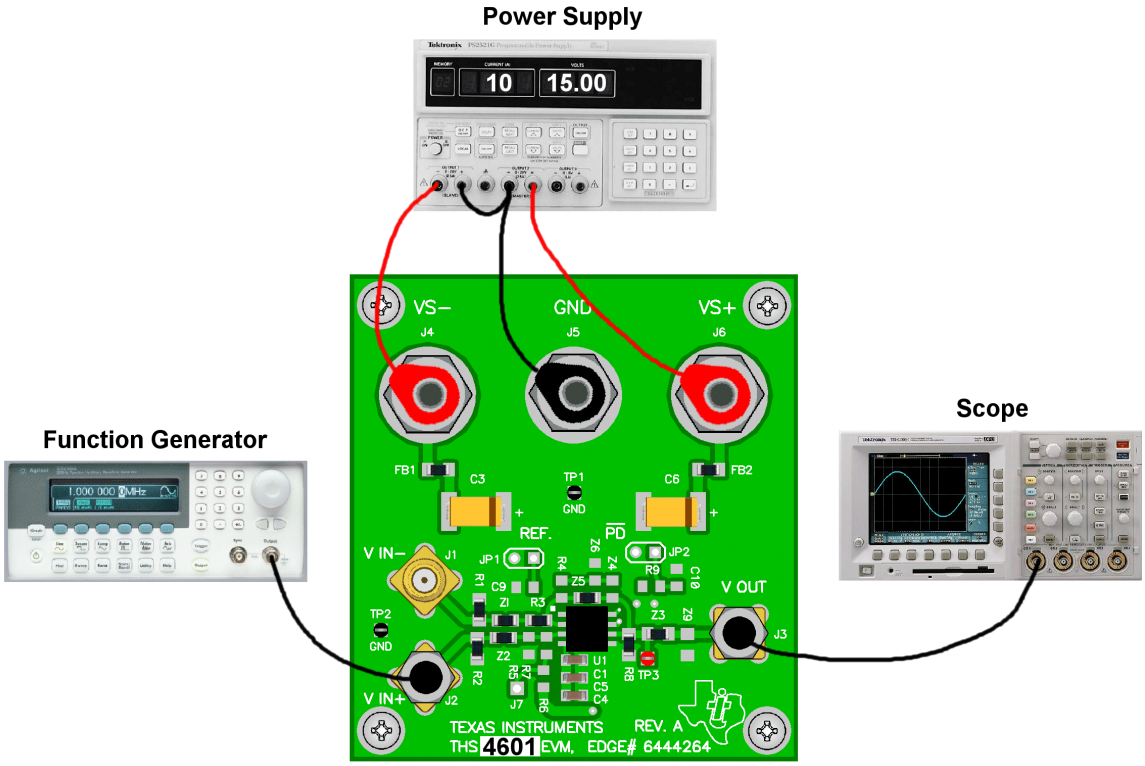
*** Means the associated component is not installed on the EVM**

Chapter 2

Using the EVM

Figure 2-1 shows how to connect power supplies, signal source and monitoring instrument. It is recommended that the user connect the EVM as shown to avoid damage to the EVM or the op amp installed on the board.

Figure 2-1. Test Equipment Connections



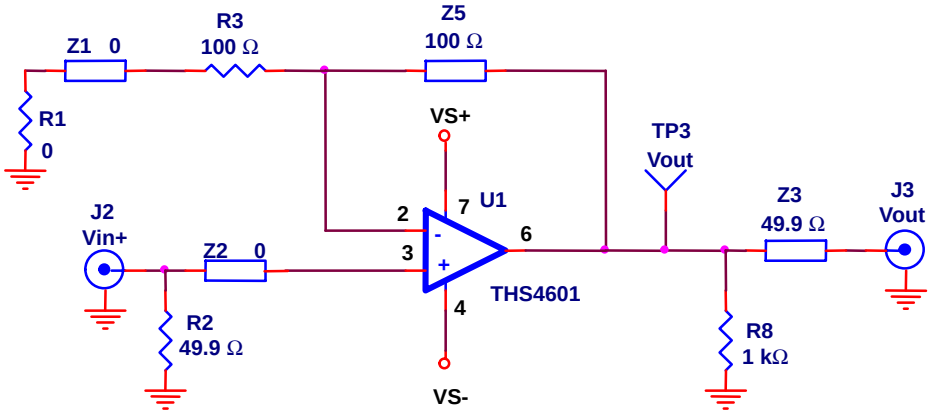
Chapter 3

EVM Applications

Example applications are presented in this chapter. These applications are meant to demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That is the function of an evaluation board.

3.1 Noninverting Gain Stages

Figure 3-1. Default Configuration—DC-Coupled, Dual Power Supply, Noninverting Gain Stage



***Power supply decoupling is not shown**

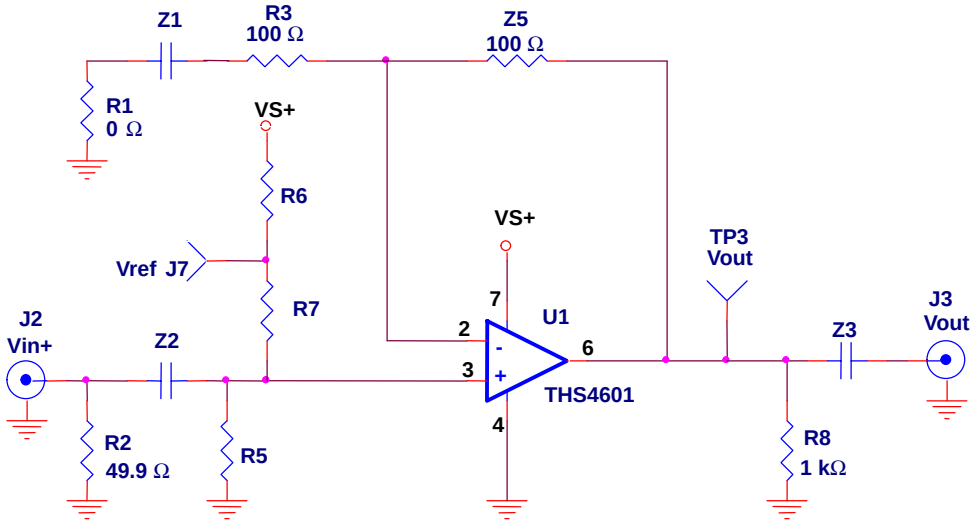
Note: This schematic reflects the default THS4601EVM configuration.

The gain measured from J2 to J3 is 2 when measured with a high impedance instrument at TP3 or J3, as determined by:

$$\frac{V_{out}}{V_{in+}} = 1 + \frac{Z5}{R3}$$

The user might note that R3 and Z5 appear to be rather small resistances. These values were selected to avoid creating a low pass pole with the input capacitance of the THS4601.

Figure 3-2. AC-Coupled, Single Power Supply, Noninverting Gain Stage



***Power supply decoupling is not shown**

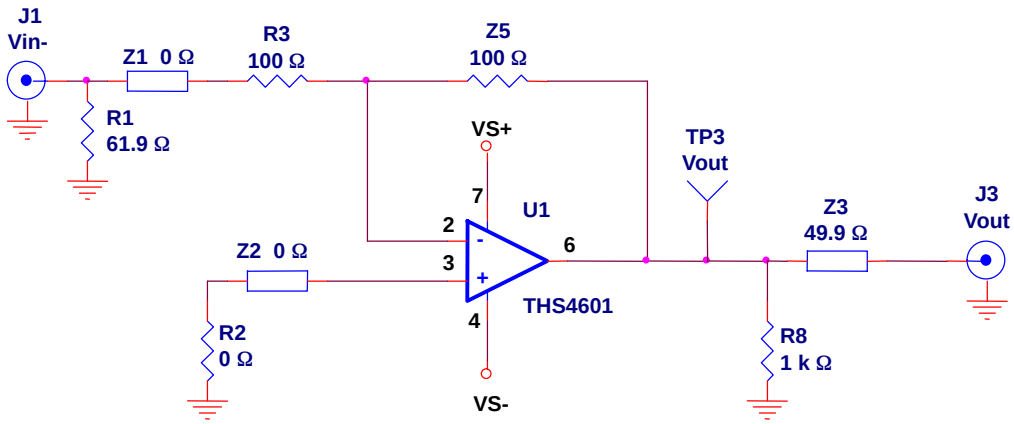
Z1 through Z3 are populated with dc-blocking capacitors, selected so they do not interfere with the frequencies that are of interest. These capacitors create high pass characteristics. R5 through R7 are selected to produce a dc potential on the noninverting input equal, or close to VS+ divided by 2. The THS4601 has low input bias currents, which allow larger bias setting resistors. If the user prefers, an external potential can be introduced at J7—use only R7 and R5. If the source of VS+ in the system is noisy, and there is a less noisy potential available in the system, it can be connected to J7. R7 and R5 can then be used as a voltage divider off of the reference attached to J7 to create the VS+ divided by 2 potential.

The gain measured from J2 to J3 is 2, and is still determined by:

$$\frac{V_{out}}{V_{in+}} = 1 + \frac{Z5}{R3}$$ (in the passband of the stage).

3.2 Inverting Gain Stages

Figure 3-3. DC-Coupled, Dual Power Supply, Inverting Gain Stage



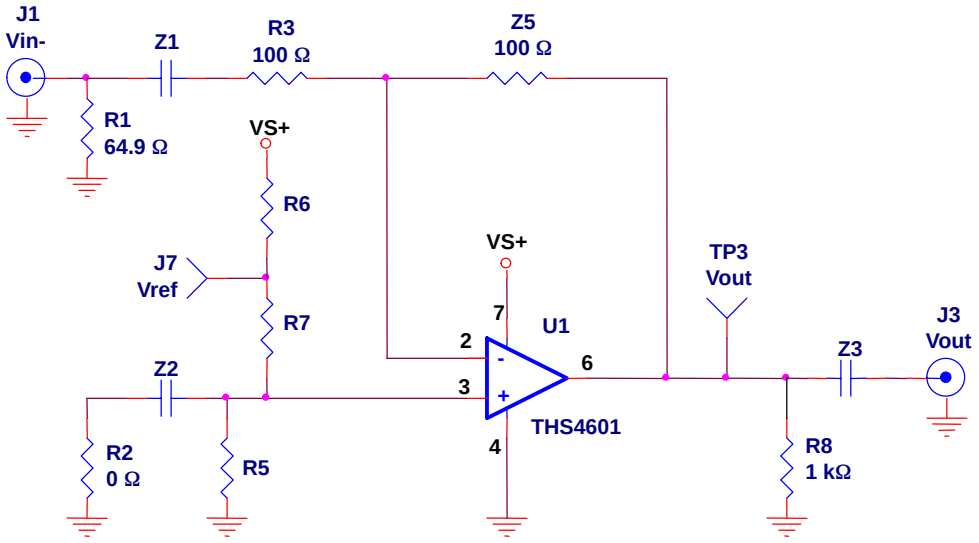
***Power supply decoupling is not shown**

The Gain measured from J1 to J3 is 1, as determined by:

$$\frac{V_{out}}{V_{in-}} = -\frac{Z5}{R3}$$

The circuit provides approximately 50 Ω of input impedance, as determined by R1 || R3 (because R3 is at ground potential due to the action of the ideal op amp model).

Figure 3-4. AC-Coupled, Single Power Supply, Inverting Gain Stage



***Power supply decoupling is not shown**

Z1 and Z3 are populated with dc-blocking capacitors, selected so they do not interfere with the frequencies that are of interest. These capacitors create high pass characteristics. R5 through R7 are selected to produce a dc potential on the noninverting input equal, or close to VS+ divided by 2. The THS4601 has low input bias currents, which allow larger bias setting resistors. If the user

prefers, an external potential can be introduced at J7, and use only resistors R7 and R5. If the source of VS+ in the system is noisy, and there is a less noisy potential available in the system, it can be connected to J7. R7 and R5 can then be used as a voltage divider off the reference attached to J7 to create the VS+ divided-by-2 potential.

The gain measured from J1 to J3 is 1 in the passband, and is still determined by:

$$\frac{V_{out}}{V_{in-}} = -\frac{Z5}{R3}$$ (in the passband of the stage).

The circuit provides approximately 50 Ω of input impedance within the passband, as determined by R1 || R3 (because R3 is at a virtual ground potential due to the action of the ideal op amp model and the decoupling capacitor Z2).

3.3 Transimpedance Amplifier

At first sight this may not appear to be an amplifier at all, but in reality the input is a current and the *gain* of the amplifier is measured in Ω, rather than volts/volt. This configuration is often used in applications where the output of a transducer is current or charge, i.e., photodiode. Applications include optical power measurements in optical networks, x-ray machines (measuring light power once the x-rays have been converted to light), and photomultiplier tube amplifiers.

Due to the capacitance associated with the transducer, a pole has to be created in the feedback loop to ensure stability.

The wide bandwidth and high operating voltage capability of the THS4601 make it unique in the applications by enabling it to offer wide output swings, thereby delivering higher dynamic ranges in a single stage.

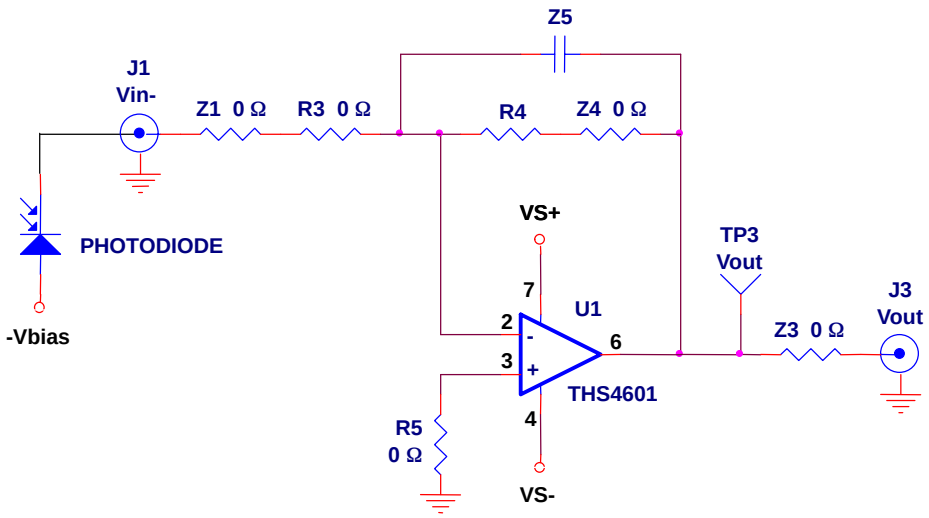
Typically, design of a transimpedance circuit is driven by the characteristics of the current source that provides the input to the gain block. A photodiode is the most common example of a capacitive current source that would interface with a transimpedance gain block. Continuing with the photodiode example, the system designer traditionally chooses a photodiode based on two opposing criteria: speed and sensitivity. Faster photodiodes cause a need for faster gain stages, and more sensitive photodiodes require higher gains, in order to develop appreciable signal levels at the output of the gain stage.

These parameters affect the design of the transimpedance circuit in a few ways. First, the speed of the photodiode signal determines the required bandwidth of the gain circuit. However, the required gain, based on the sensitivity of the photodiode, limits the bandwidth of the circuit. Additionally, the larger capacitance associated with a more sensitive signal source detracts from the achievable speed of the gain block. The dynamic range of the input

signal also places requirements on the amplifier's dynamic range. Knowledge of the source's output current levels, coupled with a desired voltage swing on the output, dictates the value of the feedback resistor, R4. The transfer function from input to output is $V_{OUT} = I_{IN}R_F$.

The large gain-bandwidth product of the THS4601 provides the capability for achieving both high transimpedance gain and wide bandwidth simultaneously. In addition, the high power supply rails provide the potential for a very wide dynamic range at the output, allowing for the use of input sources which possess wide dynamic range. The combination of these characteristics makes the THS4601 a design option for systems that require transimpedance amplification of wideband, low-level input signals. A standard transimpedance circuit is shown in Figure 3-5.

Figure 3-5. Wideband Photodiode Transimpedance Amplifier



As indicated, the current source typically sets the requirements for gain, speed, and dynamic range of the amplifier. For a given amplifier and source combination, achievable performance is dictated by the following parameters: the amplifier's gain-bandwidth product, the amplifier's input capacitance, the source capacitance, the transimpedance gain, the amplifier's slew rate, and the amplifier's output swing. From this information, the optimal performance of a transimpedance circuit using a given amplifier can be determined. Optimal is defined here as providing the required transimpedance gain with a maximally flat frequency response.

For the circuit shown in Figure 3-5, all but one of the design parameters are known; the feedback capacitor must be determined. Proper selection of the feedback capacitor prevents an unstable design, controls pulse response characteristics, provides maximally flat transimpedance bandwidth, and limits broadband integrated noise. The maximally flat frequency response results in Z5 calculated as shown below, where Z5 is the feedback capacitor, R4 is the feedback resistor, C_S is the total source capacitance (including amplifier input capacitance and parasitic capacitance at the inverting node), and GBP is the gain-bandwidth product of the amplifier in Hertz.

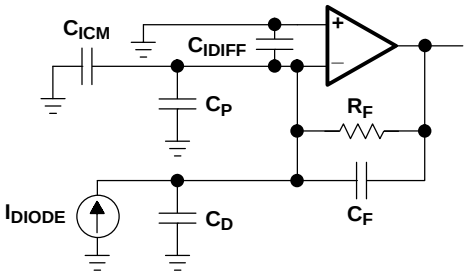
$$Z5 = \frac{\frac{1}{\pi(R4)GBP} + \sqrt{\left(\frac{1}{\pi(R4)GBP}\right)^2 + \frac{4C_S}{\pi(R4)GBP}}}{2}$$

Once the optimal feedback capacitor has been selected, the transimpedance bandwidth can be calculated:

$$F_{-3dB} = \sqrt{\frac{GBP}{2\pi(R4)\left(C_S + Z5\right)}}$$

The total source capacitance C_S is the sum of several distinct capacitances as shown in Figure 3-6.

Figure 3-6. Parasitic Capacitances in Photodiode Applications



$$C_S = C_{ICM} + C_{IDIFF} + C_P + C_D$$

where

C_{ICM} is the common-mode input capacitance.

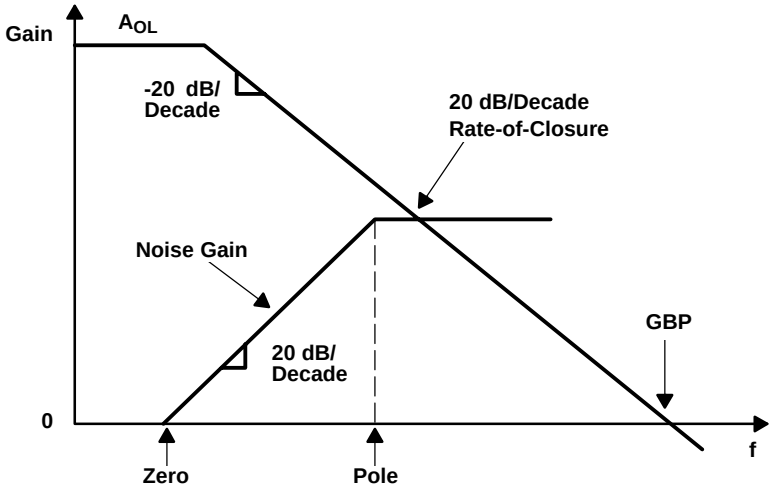
C_{IDIFF} is the differential input capacitance.

C_D is the diode capacitance.

C_P is parasitic capacitance at the inverting node.

As shown in Figure 3-7, the feedback capacitor provides a pole in the noise gain of the circuit, counteracting the zero in the noise gain caused by the source capacitance. The pole is set such that the noise gain achieves a 20 dB per decade rate-of-closure with the open-loop gain response of the amplifier, resulting in a stable circuit. As indicated, the formula given provides the feedback capacitance for maximally flat bandwidth. Reduction in the value of the feedback capacitor can increase the signal bandwidth, but this occurs at the expense of peaking in the ac response.

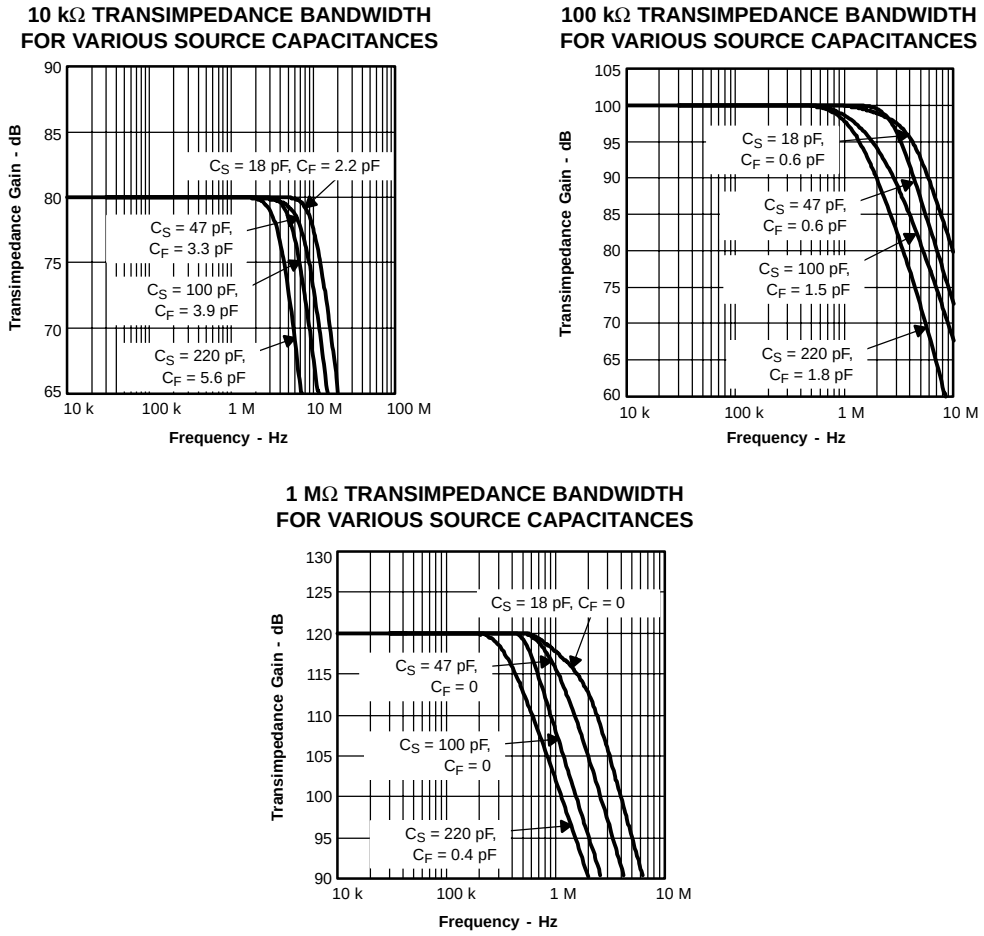
Figure 3-7. Transimpedance Circuit Bode Plot



The performance of the THS4601 has been measured for a variety of transimpedance gains with a variety of source capacitances. The achievable bandwidths of the various circuit configurations are summarized numerically in the data sheet, SLOS388.

Note that the feedback capacitances do not correspond exactly with the values predicted by the equation. They have been tuned to account for the parasitic capacitance of the feedback resistor (typically 0.2 pF for 0805 surface mount devices) as well as the additional capacitance associated with the PC board. The equation should be used as a starting point for the design, with final values for Z5 optimized in the laboratory. Figure 3-8 shows 10 kΩ, 100 kΩ, and 1 MΩ transimpedance gains for various values of feedback capacitors.

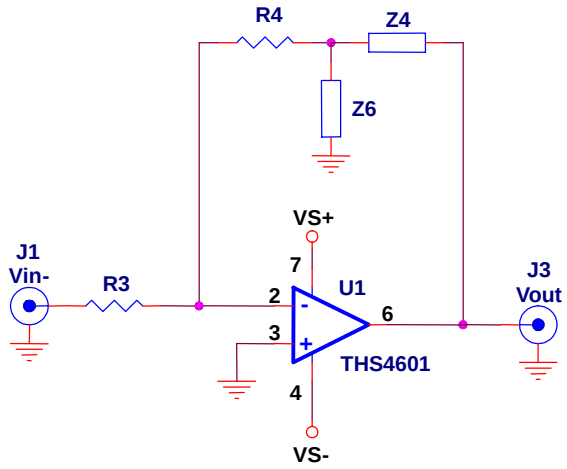
Figure 3-8. Transimpedance Gains



3.4 T-Network Gain Stages

To get higher transimpedance gains a T-Network is sometimes used. The components in the feedback path of the op amp that are shown in Figure 3-9 can be used to create either a purely resistive *T-Network* covered in this section, or a transimpedance network which is covered in the next section.

Figure 3-9. Simplified EVM Schematic for Inverting Gain



The following assumes that Z4 and Z6 are resistors.

Gain for the T-network stage is defined by the expression:

$$\frac{V_{out}}{V_{in}} = -\left(\frac{R4 + Z4}{R3} + \frac{Z4}{Z6} \times \frac{R4}{R3}\right)$$

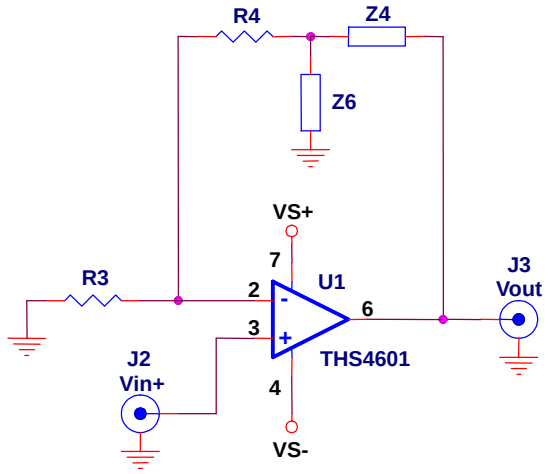
Looking at the expression above, the gain of the circuit is the standard inverting gain (the first term), modified by the second term. The second term is a voltage divider on the output voltage, multiplied by a gain term formed by R4 and R3.

When the T-network is used for noninverting gain, as shown in Figure 3-10, the gain for the T-network stage is defined by the expression:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R4 + Z4}{R3} + \frac{Z4}{Z6} \times \left(1 + \frac{R4}{R3}\right)$$

The noninverting gain expression is similar to that of the inverting gain; except that the first inverting gain term is replaced by a noninverting gain term. The second term is similarly modified—it is a voltage divider on the output voltage, multiplied by a noninverting gain term formed by R4 and R3.

Figure 3-10. Simplified EVM Schematic for Noninverting Gain



3.5 Transimpedance Networks

The components R4, and Z4 through Z6 can be used to form several transimpedance networks. Transimpedance networks are used to implement custom filter responses based on the location of poles and zeros. Pole / zero filter design is beyond the scope of this EVM manual. There are many excellent textbooks on the subject that the reader should consult. Figures 3-11 through 3-15 show some of the networks that can be implemented. Location of poles, as an *X* on an imaginary/real axis, and location of zeros as *O* are shown.

The output of the THS4601 is modeled as a ground because the ideal op amp model has zero-Ω output impedance.

Figure 3-11. Single Real Pole

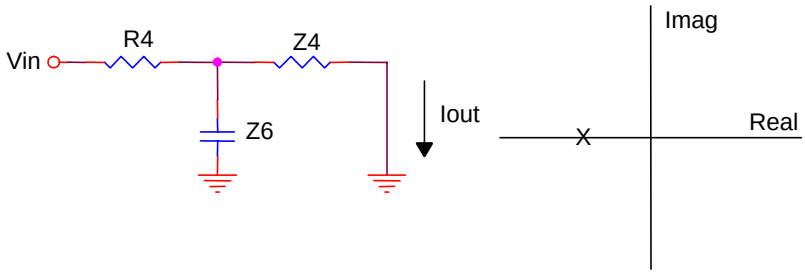


Figure 3-12. Single Real Zero

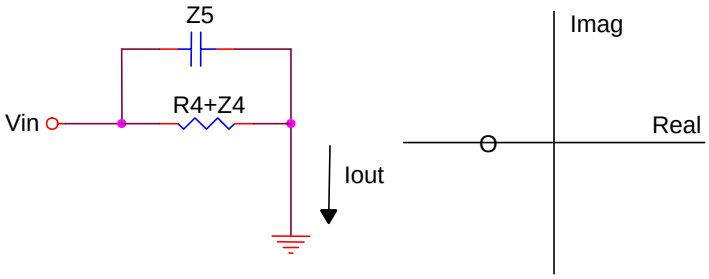


Figure 3-13. Single Real Pole and Single Real Zero (Second Configuration)

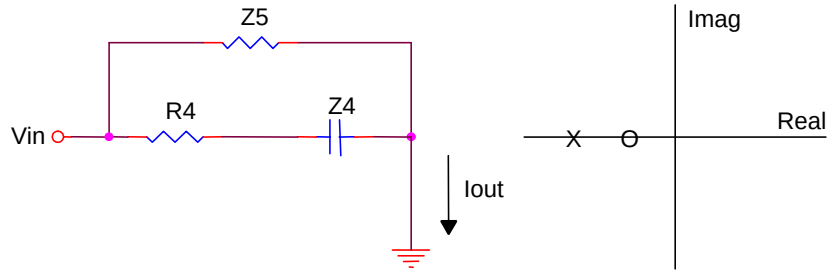


Figure 3-14. Two Real Poles, One Real Zero

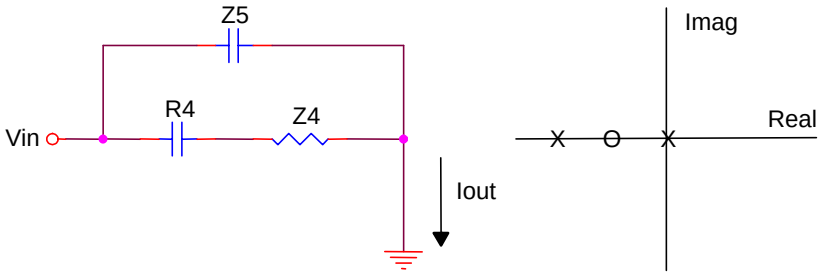
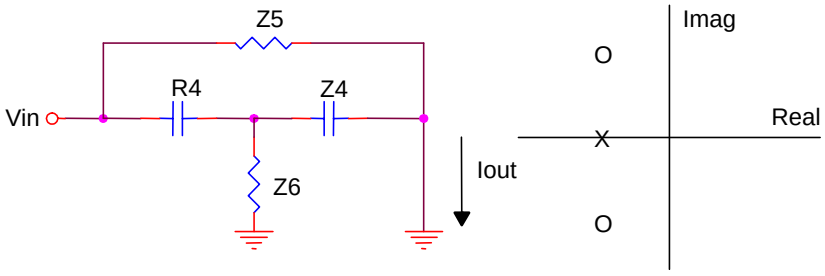


Figure 3-15. One Real Pole, Two Complex Zeros



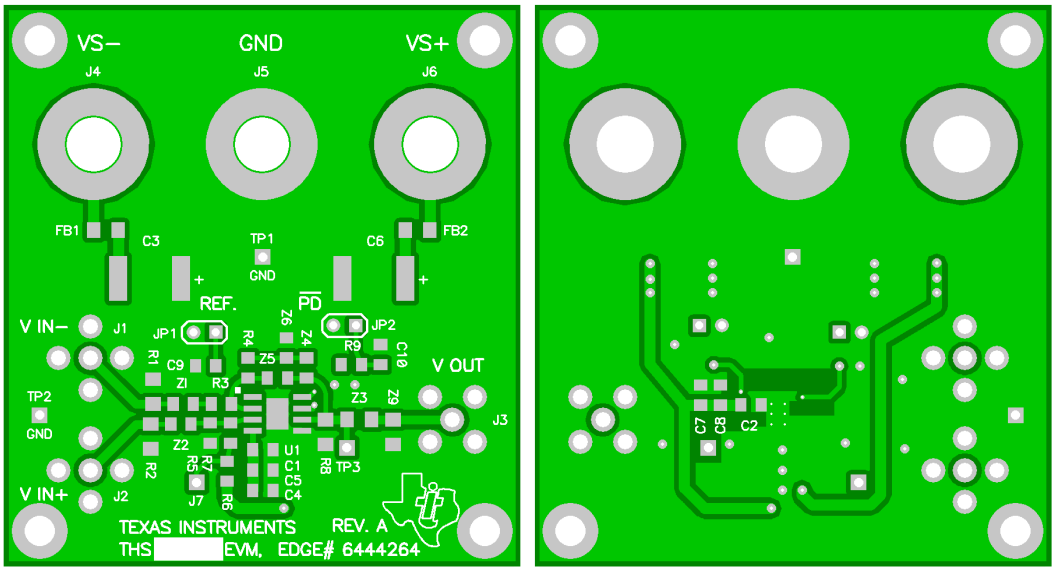
Chapter 4

EVM Hardware Description

Table 4-1. THS4601EVM Bill of Materials

Item	Description	SMD Size	Reference Desginator	PCB Qty.	Manfacturer's Part No.	Distributor's Part No.
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-010-1-ND
2	Capacitor, 22 µf, tantalum, 35 V, 10%	D	C3, C6	2	(AVX) TAJD226K035R	(Garrett) TAJD226K035R
3	Open	0805	C9, C10	2		
4	Capacitor, 0.1 µF, ceramic, x7r, 50 V	0805	C4, C7	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	Capacitor, 100 pF, ceramic	0805	C1, C2	2	(AVX) 08051A101JAT2A	(Garrett) 08051A101JAT2A
6	Capacitor, 1000 pF, ceramic	0805	C5, C8	2	(AVX) 08055A102JAT2A	(Garrett) 08055A102JAT2A
7	Open	0805	R4, R5, R6, R7, R9, Z4, Z6	7		
8	Resistor, 0 Ω, 1/8 W, 1%	0805	Z1, Z2	2	(Phycomp) 9C08052A0R00JLHFT	(Garrett) 9C08052A0R00JLHFT
9	Resistor, 100 Ω, 1/8 W, 1%	0805	R3, Z5	2	(Phycomp) 9C08052A1000FKHFT	(Garrett) 9C08052A1000FKHFT
10	Open	1206	Z9	1		
11	Resistor, 1 Ω, 1/4 W, 1%	1206	R8	1	(Phycomp) 9C12063A1001FKRFT	(Garrett) 9C12063A1001FKRFT
12	Resistor, 0 Ω, 1/4 W, 1%	1206	R1	1	(Phycomp) 9C1206A0R00JLHFT	(Garrett) 9C1206A0R00JLHFT
13	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R2, Z3	2	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
14	Open		JP1, JP2, J7	3		
15	Jack, banana receptacle, 0.25" diameter hole		J4, J5, J6	3	(SPC) 813	(Newark) 39N867
16	Test point, red		TP3	1	(Keystone) 5000	(Digi-Key) 5000K-ND
17	Test point, black		TP1, TP2	2	(Keystone) 5001	(Digi-Key) 5001K-ND
18	Connector, SMA PCB jack		J1, J2, J3	3	(Amphenol) 901-144-8RFX	(Newark) 01F2208
19	IC, THS4601		U1	1	(TI) THS4601DDA	
20	Board, printed circuit			1	(TI) EDGE # 6444264 Rev.A	

Figure 4-1. Board Layout Views



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