# NB3U23C

# 1.2 V Dual Channel CMOS Buffer / Translator

**ON Semiconductor®**

**http://onsemi.com**

### Description

The NB3U23C is a 2−input, 2−output buffer/voltage translator for UFS (Universal Flash Storage) in portable consumer applications such as mobile phones, tablets, cameras, etc. This dual channel CMOS buffer accepts 1.8 V CMOS input and translates it to 1.2 V CMOS output. The device is powered using single supply of 1.2 V ±5%.

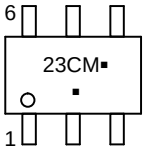
The NB3U23C is packaged in 2 ultra−small 6−pin packages: the 6 pin SC70 and a 6 pin thin UDFN package.

### Features

- Operating Frequency: 52 MHz (Max)
- Propagation Delay: 5 ns (Max)
- Low Standby Current: < 10 μA at 1.2 V $V_{DD}$
- Low Phase Noise Floor: −150 dBc/Hz (Typ)
- Rise/Fall Times (tr/tf): 2 ns (Max)
- ESD Protection Exceeds JEDEC Standards
  - 2000 V Human−Body Model (JS−001−2012)
  - 200 V Machine Model (JESD22−A115C)
  - 1000 V Charged−Device Model (JESDC101E)
- Operating Supply Voltage Range ($V_{DD}$): 1.2 V ±5%
- Operating Temperature Range (Industrial): −40°C to 85°C
- These are Pb−Free Devices

### MARKING DIAGRAMS


**SC−70**
**SQ SUFFIX**
**CASE 419B**




23C = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

**UDFN6**
**MN SUFFIX**
**CASE 517CW**


C = Device Code
M = Date Code

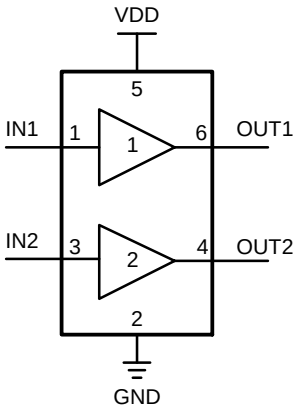



**Figure 1. Simplified Logic Diagram**

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

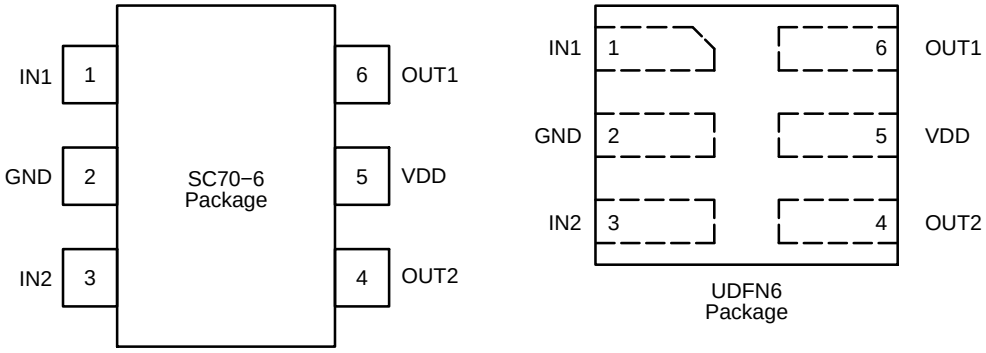



**Figure 2. Pinout Diagram** (Top Views)

**Table 1. PIN DESCRIPTION**

| Number | Name | Description |
|---|---|---|
| 1 | IN1 | Input Clock Signal − Channel 1 |
| 2 | GND | Power Supply Ground (0 V) |
| 3 | IN2 | Input Clock Signal − Channel 2 |
| 4 | OUT2 | Output − Channel 2 |
| 5 | VDD | Power Supply Voltage |
| 6 | OUT1 | Output − Channel 1 |

**Table 2. ATTRIBUTES**

| Characteristic | | Value |
|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model<br>Charge Device Model | 2 kV min<br>200 V min<br>1 kV min |
| Moisture Sensitivity (Note 1) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 120 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test II | | |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS** (Note 2)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | | 3.6 | V |
| $V_{in}$ | Input Voltage | | | $-0.5 \le V_I \le 2.5$ | V |
| $I_D$ | Output Current | | | 25 | mA |
| $T_A$ | Operating Temperature Range, Industrial | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm (Note 3)<br>0 lfpm<br>500 lfpm (Note 3) | SC70−6<br><br>UDFN−6 | 210<br>126<br>245<br>172 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | (Note 3) | SC70−6<br>UDFN−6 | 100<br>150 | °C/W |
| $T_{sol}$ | Wave Solder | | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

**Table 4. ELECTRICAL CHARACTERISTICS** (VDD = 1.2 ±5% V, GND = 0 V, $T_A$ = −40°C to +85°C)

| Symbol | Characteristic | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DIDD | Power Supply Current<br>(Single Channel Switching @ 52 MHz) | $C_L$ = 20 pF<br>$C_L$ = 5 pF<br>$C_L$ = 1 pF | | 2.5<br>1.5<br>1 | | mA |
| | Power Supply Current<br>(Both Channels Switching @ 52 MHz) | $C_L$ = 20 pF<br>$C_L$ = 5 pF<br>$C_L$ = 1 pF | | 5<br>3<br>2 | | mA |
| $I_{off}$ | Standby Current | Vi = $V_{IH}$ Max or GND;<br>$V_{DD}$ = 1.2 V, No Output Load | | | 10 | μA |
| $V_{IH}$ | Input High Voltage | | 0.65 * VDD | | 1.98 | V |
| $V_{IL}$ | Input Low Voltage | | 0 | | 0.35 * VDD | V |
| $V_{OH}$ | Output High Voltage | $C_L$ = 20 pF<br>$R_L$ = 100 kΩ | 0.75 * VDD | | VDD | V |
| $V_{OL}$ | Output Low Voltage | $C_L$ = 20 pF<br>$R_L$ = 100 kΩ | 0 | | 0.25 * VDD | V |
| $C_{in}$ | Input Capacitance | | | | 5 | pF |
| $F_{clk}$ | Operating Frequency Range | | 0 | | 52 | MHz |
| $t_{PD}$ | Propagation Delay | INx to OUTx<br>$C_L$ = 20 pF, $R_L$ = 100 kΩ | | | 5 | ns |
| | Phase Noise Floor Density<br>(Notes 4 and 5) | $C_L$ = 20 pF<br>$R_L$ = 100 kΩ | | −150 | | dBc/Hz |
| | Additive RMS Phase Jitter<br>(Notes 5 and 6) | $C_L$ = 20 pF<br>$R_L$ = 100 kΩ<br>Offset Frequency Range:<br>50 kHz to 10 MHz | | 0.15 | 0.25 | ps |
| DC | Output Duty Cycle (Note 7) | Input Duty Cycle = 50%,<br>Min Input Slew Rate = 1 V/ns | 45 | | 55 | % |
| tr/tf | Output Rise/Fall Times | 0.2 * $V_{DD}$ to 0.8 * VDD<br>$C_L$ = 20 pF<br>$R_L$ = 100 kΩ | | | 2 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. White noise floor.
5. This parameter refers to the random jitter only.
6. The output RMS phase jitter can be calculated using the following equation:
   (Output RMS Phase Jitter)$^2$ = (Input RMS Phase Jitter)$^2$ + (Additive RMS Phase Jitter)$^2$
7. Measured with input voltage swing from 0 V to 1.8 V.

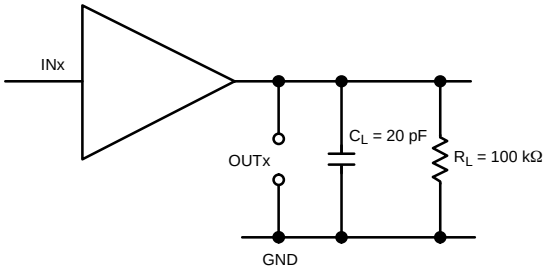



**Figure 3. Typical Test Setup for Evaluation**

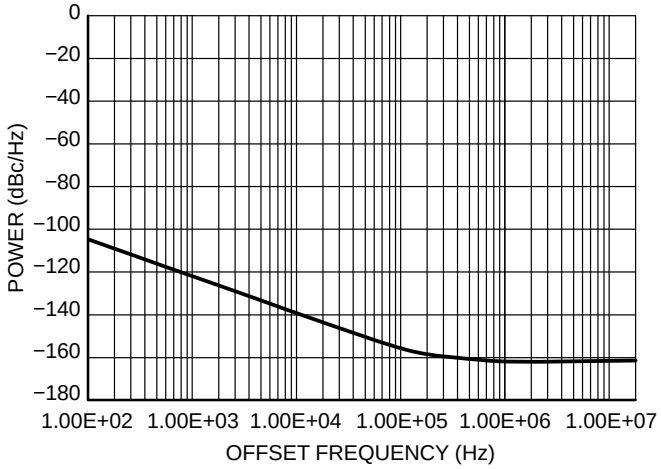



**Figure 4. Typical Phase Noise Plot at 50 MHz Carrier Frequency**

## ORDERING INFORMATION

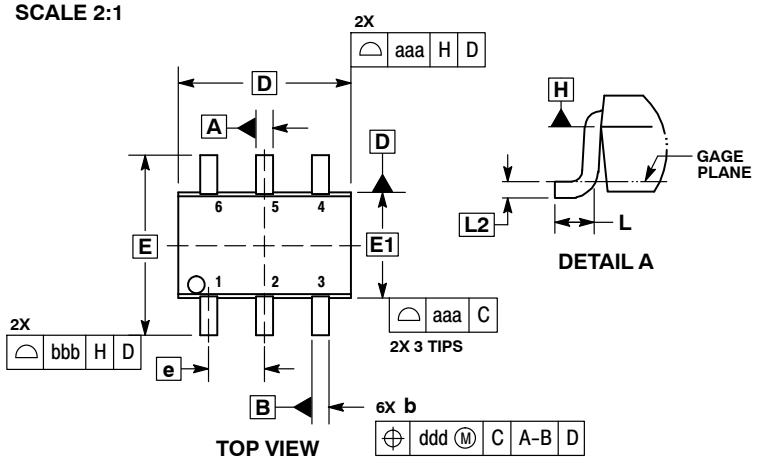
| Device | Package | Shipping† |
|---|---|---|
| NB3U23CSQTCG | SC−70−6<br>(Pb−Free) | 3000 / Tape & Reel |
| NB3U23CMNTAG | UDFN6<br>(Pb−Free) | 3000 / Tape & Reel |

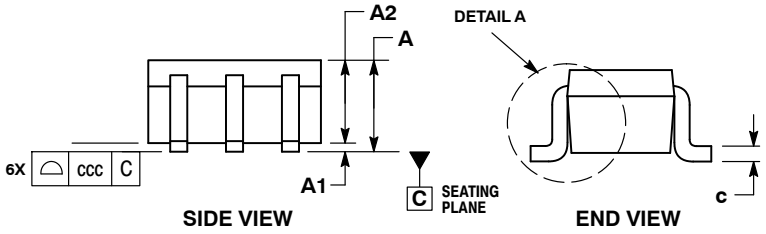
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SC−88/SC70−6/SOT−363**
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
**SCALE 2:1**

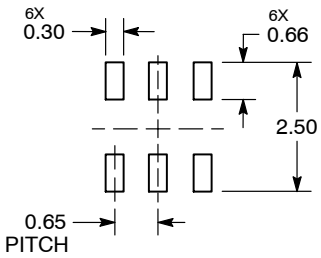



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| **A** | −−− | −−− | 1.10 | −−− | −−− | 0.043 |
| **A1** | 0.00 | −−− | 0.10 | 0.000 | −−− | 0.004 |
| **A2** | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| **b** | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| **C** | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| **D** | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| **E** | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| **E1** | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| **e** | 0.65 BSC | | | 0.026 BSC | | |
| **L** | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| **L2** | 0.15 BSC | | | 0.006 BSC | | |
| **aaa** | 0.15 | | | 0.006 | | |
| **bbb** | 0.30 | | | 0.012 | | |
| **ccc** | 0.10 | | | 0.004 | | |
| **ddd** | 0.10 | | | 0.004 | | |

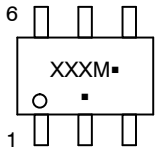
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.


**STYLES ON PAGE 2**

**SC−88/SC70−6/SOT−363**
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42985B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SC−88/SC70−6/SOT−363** | **PAGE 2 OF 2** |

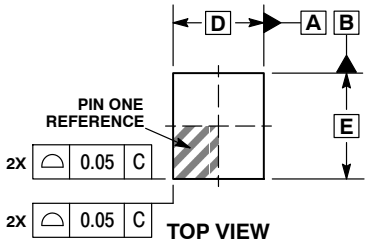
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

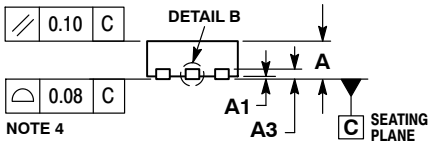
SCALE 4:1

**UDFN6 1.2x1.4, 0.4P**
CASE 517CW
ISSUE O

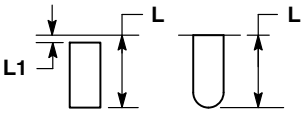
DATE 09 JAN 2014



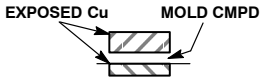

TOP VIEW



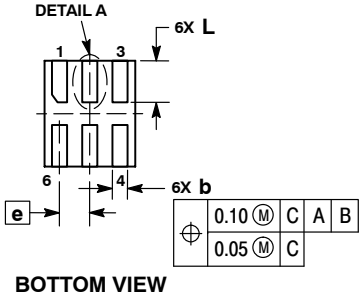

SIDE VIEW




**DETAIL A**
OPTIONAL TERMINAL CONSTRUCTIONS




**DETAIL B**
OPTIONAL CONSTRUCTION




BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.

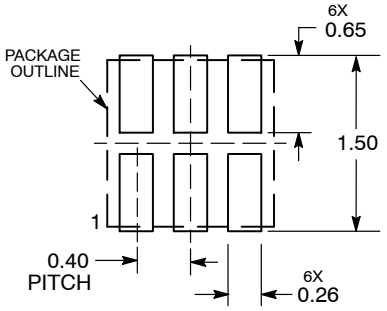
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| D | 1.20 BSC | |
| E | 1.40 BSC | |
| e | 0.40 BSC | |
| L | 0.50 | 0.60 |
| L1 | --- | 0.15 |

### GENERIC MARKING DIAGRAM*


X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON81510F** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **UDFN6 1.2X1.4, 0.4P** | **PAGE 1 OF 1** |

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊