Au5508: Quad PLL Frequency Translator / Jitter Attenuator / Network and Port Synchronizer / AAU Clock

General Description

Au5508 offers most integrated 5G clock solution: Combines BBU, Wireline, AAU, Serdes requirements in one part definition.

- Unique integration of Sync Features
  - Enables Systems with Low Constant Time Interval Error
  - IEEE1588/SyncE/1 PPS full support
- Lower jitter for higher data rate links
- Lower close in noise and JESD204B/C full support for AAU RF clocks
- Integrated feature rich single part offers unparalleled flexibility to the system designer

Features

- Ultra Performance PLLs
- Fully Integrated design with no external components
- 120 fs Typical RMS integrated jitter (12k-20M)
- 122.88M Output with excellent close in noise performance
- Fully Flexible Output and Input Mux: High level of flexibility in output allocation for PLLs
- JESD204B/C Support for data converter clocks
- 1 PPS Input / Output Support with sub 20s lock time
- External EEPROM Support
- TDC Mode available on all input clocks to measure input delays with < 10 ps accuracy: 10 TDC Channels available (independent of the PLLs)
- Frequency Control DCO: DCO Control on all outputs (down to 1/16 ppt)
- Phase Control DCO: Fine phase adjustment knob for phase of all outputs from a PLL (adjustment accuracy < 1ps) in both closed loop and open loop modes
- Internal modes to combine wander of OCXO with jitter of XO for holdover– Provides 24 hour holdover with programmable HO accuracy settings
- Best in class hitless switching performance: PBO with sub 25 ps hit, Phase Propagation & Frequency Ramp with programmable freq/phase slopes
- Fully integrated Jitter and wander attenuation options down to 0.09 mHz
- Repeatable input to output delays with output relative delay adjust
- Internal ZDB Mode with < 0.5 ns Input to Output delay independently available for each PLL
- Outputs can be phase aligned an independent sync pulse
- 72 QFN 10mm X 10mm Package

Product Family	Inputs / Outputs	Input Freq	Output Frequency	RMS Jitter	Packages
55xx	5 Diff / 10 SE Inputs Up to 12 Diff / 24 SE Outputs	0.5 Hz - 2.1 GHz	0.5 Hz- 2.94912 GHz	~ 120 fs typ	72 QFN

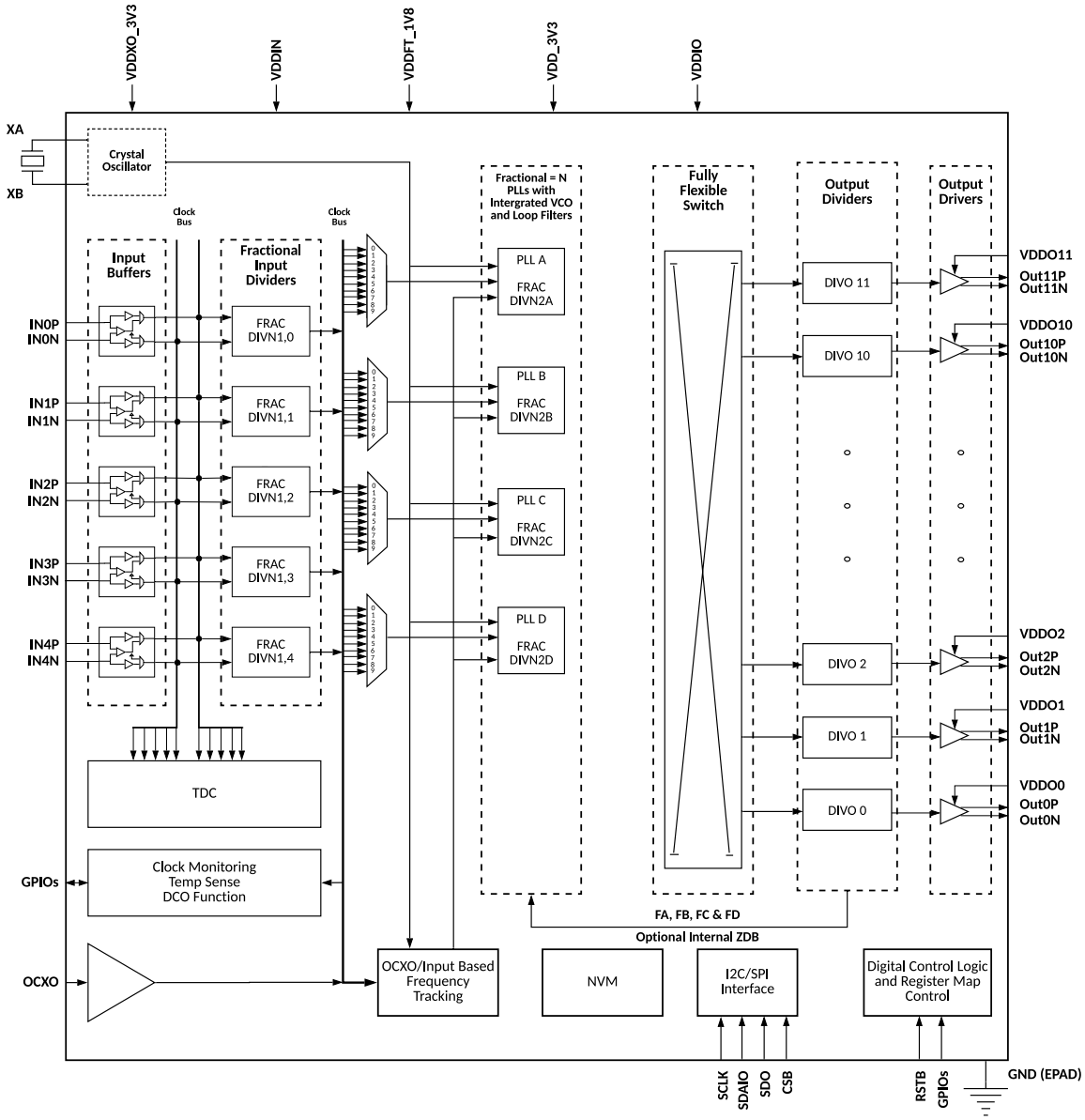

Figure 1 Functional Overview

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1 Pin Description

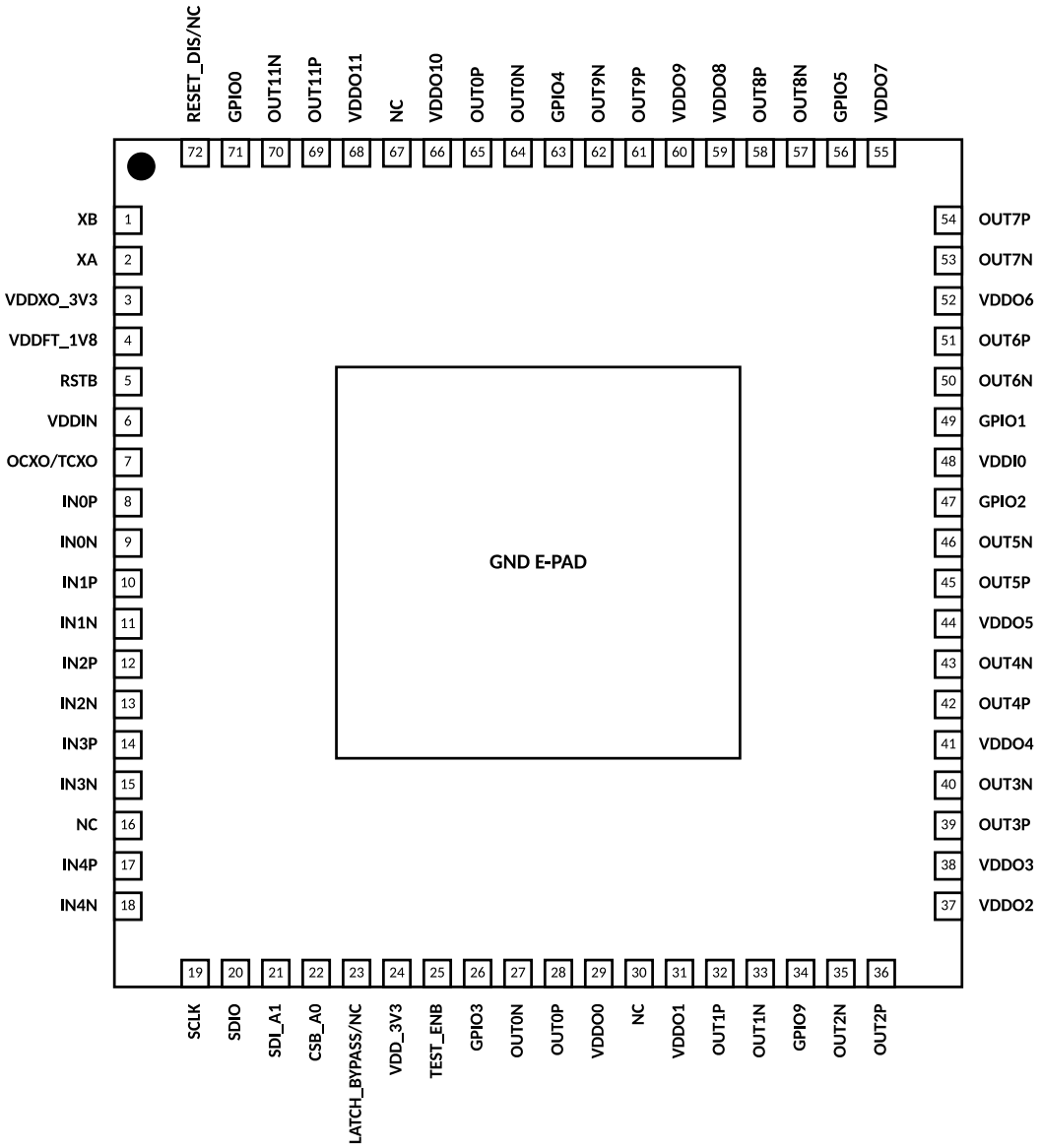


Figure 2 Au5508 Pin Configuration

Table 1 Pin Description

Pin No	Name	I/O Type	Voltage Level	Default Pull Up/ Down	Description
1	XB	Output			Crystal Output. Crystal connects to this pin. Leave unconnected if External oscillator is connected to XA.
2	XA	Input	< 1.4 V		Crystal Input. External reference clock input.
3	VDDXO_3V3	Power	2.5 V – 3.6 V		Analog Power supply for Crystal Oscillator
4	VDDFT_1V8	Power	1.71 V – 2 V		Analog Power Supply for Frequency tracking PLL, Input TDC and Clock Monitors.
5	RSTB	Reset	VDDIO (Pin 48)	Pull up	Reset Input
6	VDDIN	Power	1.71 V/2.5 V/ 3.6 V		Analog Power Supply for Input buffers and dividers.

Pin No	Name	I/O Type	Voltage Level	Default Pull Up/ Down	Description
7	OCXO/TCXO	Input	-0.5V – 3.6 V		Clock reference input. A low wander input such as an OCXO or TCXO clock can be applied on this input. Alternatively it can be used as an extra single ended CMOS input.
8	IN0P	Input	-0.5V – 3.6 V		Clock + for differential clock input. Single ended Input clock.
9	IN0N	Input	-0.5V – 3.6 V		Clock - for differential clock input. Single ended Input clock.
10	IN1P	Input	-0.5V – 3.6 V		Clock + for differential clock input. Single ended Input clock.
11	IN1N	Input	-0.5V – 3.6 V		Clock - for differential clock input. Single ended Input clock.
12	IN2P	Input	-0.5V – 3.6 V		Clock + for differential clock input. Single ended Input clock.
13	IN2N	Input	-0.5V – 3.6 V		Clock - for differential clock input. Single ended Input clock.
14	IN3P	Input	-0.5V – 3.6 V		Clock + for differential clock input. Single ended Input clock.
15	IN3N	Input	-0.5V – 3.6 V		Clock - for differential clock input. Single ended Input clock.
16	NC	No Connect			Pin not bonded.
17	IN4P	Input	-0.5V – 3.6 V		Clock + for differential clock input. Single ended Input clock.
18	IN4N	Input	-0.5V – 3.6 V		Clock - for differential clock input. Single ended Input clock.
19	SCLK	I/O	VDDIO (Pin 48)	Pull Up	Serial Clock for I2C/SPI Mode
20	SDIO	I/O	VDDIO (Pin 48)	Pull Up	I/O data port in I2C/3W SPI. Output port in 4W SPI mode.
21	SDI_A1	I/O	VDDIO (Pin 48)	Pull Up	Input data port in 4W SPI. Optional I2C Address bit.
22	CSB_A0	Input	VDDIO (Pin 48)	Pull Up	Input port as chip select in SPI mode. Optional I2C Address bit.
23	LATCH_BYPASS/ NC	Input	VDDIO (Pin 48)	Pull Down	Enable bypass Wake GPIO latching/ No Connect for parts where GPIO latching function is needed. There is a default internal pull down resistor of 25k.
24	VDD_3V3	Power	2.5 V – 3.6 V		Analog PLL Power Supply.
25	TEST_ENB	Input	VDDIO (Pin 48)	Pull Up	Enable DFT Test Mode.
26	GPIO3	I/O	VDDIO (Pin 48)	Pull Down	Configurable as per NVM bits.
27	OUT0N	Output	VDDO0		Clock – for differential Output. Single ended CMOS Output.
28	OUT0P	Output	VDDO0		Clock + for differential Output. Single ended CMOS Output.
29	VDDO0	Power	1.71 V – 3.6 V		Power supply for OUT0 drivers.
30	NC	No Connect			Pin not bonded.
31	VDDO1	Power	1.71 V– 3.6 V		Power supply for OUT1 drivers.
32	OUT1P	Output	VDDO1		Clock + for differential Output. Single ended CMOS Output.
33	OUT1N	Output	VDDO1		Clock - for differential Output. Single ended CMOS Output.
34	GPIO9	I/O	VDDIO (Pin 48)	Pull Up	Used I2C/SPI select during power up. Configurable as per NVM bits.

Pin No	Name	I/O Type	Voltage Level	Default Pull Up/ Down	Description
35	OUT2N	Output	VDDO2		Clock – for differential Output. Single ended CMOS Output.
36	OUT2P	Output	VDDO2		Clock + for differential Output. Single ended CMOS Output.
37	VDDO2	Power	1.71 V– 3.6 V		Power supply for OUT2 drivers.
38	VDDO3	Power	1.71 V – 3.6 V		Power supply for OUT3 drivers.
39	OUT3P	Output	VDDO3		Clock + for differential Output. Single ended CMOS Output.
40	OUT3N	Output	VDDO3		Clock - for differential Output. Single ended CMOS Output.
41	VDDO4	Power	1.71 V – 3.6V		Power supply for OUT4 drivers.
42	OUT4P	Output	VDDO4		Clock + for differential Output. Single ended CMOS Output.
43	OUT4N	Output	VDDO4		Clock - for differential Output. Single ended CMOS Output.
44	VDDO5	Power	1.71 V– 3.6 V		Power supply for OUT5 drivers.
45	OUT5P	Output	VDDO5		Clock + for differential Output. Single ended CMOS Output.
46	OUT5N	Output	VDDO5		Clock - for differential Output. Single ended CMOS Output.
47	GPIO2	I/O	VDDIO (Pin 48)	Pull Up	Configurable as per NVM bits.
48	VDDIO	Power	1.71 V– 3.6 V		GPIO/Serial Interface port Power Supply.
49	GPIO1	I/O	VDDIO (Pin 48)	Pull Up	Configurable as per NVM bits.
50	OUT6N	Output	VDDO6		Clock – for differential Output. Single ended CMOS Output.
51	OUT6P	Output	VDDO6		Clock + for differential Output. Single ended CMOS Output.
52	VDDO6	Power	1.71 V– 3.6 V		Power supply for OUT6 drivers.
53	OUT7N	Output	VDDO7		Clock – for differential Output. Single ended CMOS Output.
54	OUT7P	Output	VDDO7		Clock + for differential Output. Single ended CMOS Output.
55	VDDO7	Power	1.71 V– 3.6 V		Power supply for OUT7 drivers.
56	GPIO5	I/O	VDDIO (Pin 48)	Pull Up	Configurable as per NVM bits.
57	OUT8N	Output	VDDO8		Clock – for differential Output. Single ended CMOS Output.
58	OUT8P	Output	VDDO8		Clock + for differential Output. Single ended CMOS Output.
59	VDDO8	Power	1.71 V– 3.6 V		Power supply for OUT8 drivers.
60	VDDO9	Power	1.71 V– 3.6 V		Power supply for OUT9 drivers.
61	OUT9P	Output	VDDO9		Clock + for differential Output. Single ended CMOS Output.
62	OUT9N	Output	VDDO9		Clock - for differential Output. Single ended CMOS Output.
63	GPIO4	I/O	VDDIO (Pin 48)	Pull Up	Configurable as per NVM bits.
64	OUT10N	Output	VDDO10		Clock – for differential Output. Single ended CMOS Output.
65	OUT10P	Output	VDDO10		Clock + for differential Output. Single ended CMOS Output.
66	VDDO10	Power	1.71 V– 3.6 V		Power supply for OUT10 drivers.
67	NC	No Connect			Pin not bonded.

Pin No	Name	I/O Type	Voltage Level	Default Pull Up/ Down	Description
68	VDDO11	Power	1.71 V– 3.6 V		Power supply for OUT11 drivers.
69	OUT11P	Output	VDDO11		Clock + for differential Output. Single ended CMOS Output.
70	OUT11N	Output	VDDO11		Clock - for differential Output. Single ended CMOS Output.
71	GPIO0	I/O	VDDIO (Pin 48)	Pull Down	Configurable as per NVM bits.
72	RESET_DIS/NC	I/O	< 3.6 V	Pull Down	Disables Hard reset when pulled high.
ePad	Ground		0 V		Ground Pad

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings

Description	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltages	Reference XO Supply FTPLL Supply Input Supply PLL Supply GPIO Supply	V_{DDXO_3V3} V_{DDFT_1V8} V_{DDIN} V_{DD_3V3} V_{DDIO}	-0.5		+3.63	V
Output bank supply voltage	Output Driver Supply	V_{DDO}	-0.5		+3.63	V
Input voltage, All Inputs	Relative to GND Clock Inputs OCXO Input GPIO inputs	V_{IN}	-0.5		+3.63	V
XO Inputs	Relative to GND	V_{XO}	-0.5		+1.4	V
I2C Bus input voltage	SCLK SDIO	V_{INI2C}	-0.5		+3.63	V
SPI Bus input voltage	SDI_A1 CSB_A0	V_{INSPI}	-0.5		+3.63	V
Storage temperature	Non-functional, Non-Condensing	T_S	-55		+150	°C
Programming Temperature		T_{PROG}	+25		+85	°C
Maximum Junction Temperature in Operation		T_{JCT}			+125	°C
Programming Voltage (for Programming the OTP (Fuse Memory).		V_{PROG}	2.375	2.5	2.625	V
ESD (human body model)	JESD22A-114	ESD_{HBM}			2000	V
ESD (charge device model)		ESD_{CDM}			500	V
Latch Up	JEDEC JESD78D	LU			100	mA

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied.
- Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.
- Any pin category not covered here has a default minimum rating of -0.5 V and a default maximum rating of 3.63 V.

Table 3 Operating Temperature and Thermal Characteristics

Description	Conditions	Symbol	Min	Typ	Max	Units
Ambient temperature		TA	–40	–	+85	°C
Junction temperature		TJ			+125	°C
Au5508: 72-QFN package						
Thermal Resistance Junction to Ambient	Still Air	θ_{JA}		18.1		°C/W
	Air Flow :1m/s			15.3		
	Air Flow: 2m/s			14.3		
Thermal Resistance Junction to Case		θ_{JC}		6.7		°C/W
Thermal Resistance Junction to Board		θ_{JB}		6.46		°C/W

Description	Conditions	Symbol	Min	Typ	Max	Units
Au5508						
PLL Supply	3.3 V range: ± 10%	V_{DD_3V3}	2.97	3.3	3.63	V
XO Supply	3.3 V range: ±10%	V_{DDXO_3V3}	2.97	3.3	3.63	V
FTPLL/TDC Supply	1.8 V range: ±5%	V_{DDFT_1V8}	1.71	1.8	1.89	V
Input Buffer Supply	3.3 V range: ±10%	V_{DDIN}	2.97	3.3	3.63	V
GPIO Supply	1.8 V range: ±5%	V_{DDIO}	1.71	1.80	1.89	V
	2.5 V range: ±5%		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Output Driver Supply	1.8 V range: ±5%	V_{DDO}	1.71	1.80	1.89	V
	2.5 V range: ±5%		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Power Dissipation (VDD_3V3 = VDDXO_3V3=VDDO = 3.3 V, VDDFT_1V8=1.8)						
Total Power Dissipation (3.3V LVDS Outputs @ 156.25M)	4 PLLs, 12 Outputs 5 DE Inputs, OCXO PLL	Pd		2.2		W
	1 PLL, 2 Outputs 1 DE			500		mW
Supply Current						
VDDIN	All Five DE Inputs assumed to be enabled	I_{DDIN}		45		mA
VDD_3V3	All Four PLLs and All 12 Outputs enabled	I_{DD_3V3}		400		mA
VDDFT_1V8	FTPLL and All 10 Input TDC enabled	I_{DDFT_3V3}		30		mA
VDDXO_3V3	Crystal Oscillator	I_{DDXO_3V3}		10		mA
VDDO[4,7]	LVPECL, output pair terminated 50 Ω to V_{TT} (VDDO – 2 V).	I_{DDO} [1,2,3,5]		18		mA
	LVPECL2, output pair terminated 50 Ω to V_{TT} (VDDO – 2 V) or 0V without common mode current.			19		mA
	CML, output pair terminated 50 Ω to VDDO	I_{DDO} [1,5]		14		mA
	HCSL, output pair with HCSL termination	I_{DDO} [1,5]		19		mA
	LVDS output pair terminated with an AC or DC Coupled diff 100 Ω	I_{DDO} [1,5]		17		mA
	LVCMOS, 250 MHz, 2.5V output, 5-pF load	I_{DDO} [5,6]		22		mA

Notes:

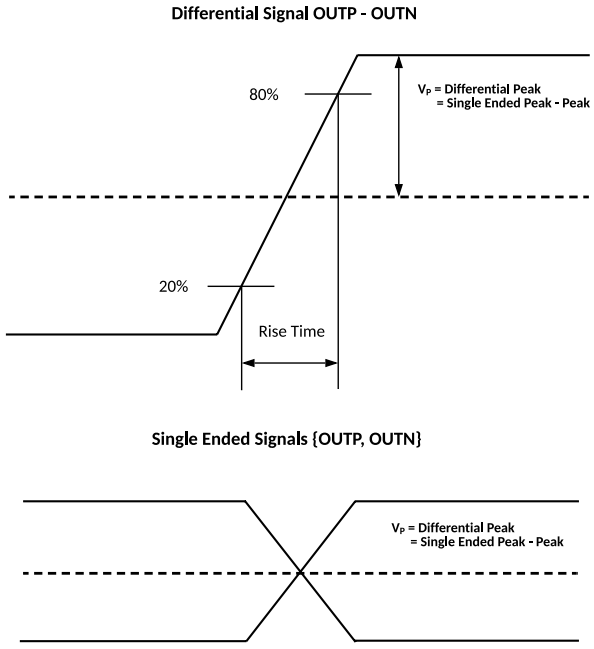
1. LVPECL standard is supported for V_{DDO} = {2.5 V, 3.3 V}. LVPECL2, HCSL, CML and LVDS standards are supported for V_{DDO} = {1.8 V, 2.5 V, 3.3 V}.
2. LVPECL mode provides 6 mA of common mode current on each output. LVPECL2 mode does not provide this common mode current.
3. A 50 Ω Termination resistor with a DC bias of V_{DDO} – 2 V for LVPECL standards is supported for V_{DDO} = {2.5 V, 3.3 V}.

4. IDDOx Output driver supply current specified for one output driver in the table. This includes current in each of the output module that includes output dividers, drivers and clock distributions.
5. Refer to the Output Termination Information in Section 9 in the full Datasheet for the description of the various terminations that are supported.
6. Both P and N terminal are active in LVCMOS mode.
7. Current consumption doesn't account for load current. LVCMOS current include load current also.

Table 4 Input Clock Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input Buffer with Differential DC or AC Coupled (See Input Slave Description for Termination information)						
Input Frequency Range	Differential	f_{IN}	0.5	—	2100M	Hz
	All Single-ended signals (including LVCMOS)		0.5	—	250M	Hz
PLL Input Frequency Range [1]	PLL Input Frequency	f_{IN_DPLL}	0.5	-	30M	Hz
Input Common Mode Voltage Range (for DC Coupled Differential Inputs)	Differential DC coupled inputs; Defined as cross point	V_{CMR}	0.25	-	VDDIN – 0.85	V
Single Ended Peak to Peak Voltage [2]	f_{IN} < 400 MHz	VP_{IN}	100	—	-	mV
	400 MHz < f_{IN} < 750 MHz		225	—	-	mV
	750 MHz < f_{IN} < 2100 MHz		350	—	-	mV
Single Ended AC Coupled input- — DC-coupled (IN0P/N, IN1P/N, IN2P/N, IN3P/N, IN4P/N, OCXO Input)						
Single Ended AC Coupled Inputs (Single Ended Peak to Peak Input) [3]	AC-Coupled f_{IN} < 250 MHz	f_{IN,SE_AC}	500	_	3600	mV
Slew Rate [4]		SR	400	—	—	V/µs
Duty Cycle		DC	40	—	60	%
Input Capacitance		C_{IN}	—	0.3	—	pF
Input Resistance	AC Coupled SE	R_{IN}	—	15	—	kΩ
Pulsed CMOS Input Buffer — DC-coupled (IN0P/N, IN1P/N, IN2P/N, IN3P/N, IN4P/N, OCXO Input)						
Input Frequency		$f_{IN\_PULSED\_CMOS}$	0.5	—	250M	Hz
Input Voltage		V_{IL}	–0.2	—	0.4	V
		V_{IH}	0.8	—	VDDIN	V
Slew Rate [4]		SR	400	—	—	V/µs
Duty Cycle		DC	40	—	60	%
Input Resistance		R_{IN}	—	30	—	kΩ
Reference Clock (Applied to XA), Can be external XO						
Reference Clock Frequency	Range for best jitter	F_{IN_REF}	48	-	160	MHz
	Overall supported range		25	-	160	MHz
Input Voltage Swing	Single Ended peak to peak	V_{IN_SE}	365	-	2000	mVpp_se
	Differential peak to peak	V_{IN_DIFF}	365	-	2500	mVpp_diff
Slew rate		SR	400	-	-	V/us
Duty Cycle		DC	40	-	60	%

Notes:
1. For proper device operation, the input frequency is internally divided down to 30 MHz or less (PLL Phase Detector maximum frequency = 30 MHz). This is achieved using internal dividers in the chip.
2. VP_{IN} is the single-ended peak-peak of the input signal which is equal to the differential peak. This is the swing requirement for both AC and DC coupled differential inputs where the swing is considered at the pin inputs.



3. AC Coupled input assumed with series capacitance for single ended AC Coupled inputs. Swing requirement at device pins for
4. Minimum slew rate specification is for best noise performance.

Table 5 Serial Data and Clock Input, GPIOs

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Voltage		V_{IL}	—	—	0.3 x V_{DDIO}[1]	V
		V_{IH}	0.7 x V_{DDIO}[1]	—	VDDIO	V
Input Capacitance		C_{IN}	—	1	—	pF
Input Resistance		R_{IN}	—	25	—	kΩ
Minimum Pulse Width	FINC, FDEC	PW	100	—	—	ns
Minimum RESET duration		T_{RES}	100			µs
Update Rate	FINC, FDEC	F_{UR}	—	—	1	µs

Notes:
1. VDDIO is the voltage used for all the status GPIOs and the serial interface. This is the voltage applied on Pin 48
2. FINC/FDEC are the increment and decrement for the DCO opertaion from the pins

Table 6 Output Serial and Status Pin

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
All VDDIO based GPIOs						
Output Voltage	I_{OH} = -2 mA	V_{OH}	V_{DDIO} x 0.75	—	—	V
	I_{OL} = 2 mA	V_{OL}	—	—	V_{DDIO} x 0.25	V

Notes:
1. VDDIO is the voltage used for all the status GPIOs and the serial interface. This is the voltage applied on Pin 48

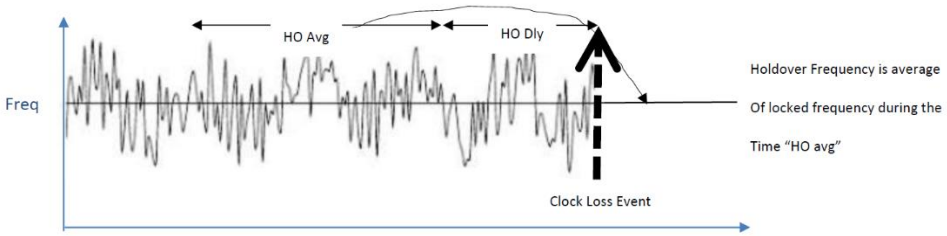
Table 7 Output Clock Characteristics

Description	Conditions	Symbol	Min	Typ	Max	Units
Differential output frequency continuous support [1],[2]	Differential output standards	$F_{OUT,DIFF}$ [1,3]	0.5		800M	Hz
Differential output frequency Selective Higher Frequency Support (For >800MHz outputs)[3]	Differential Output Standards		61.44M* {15, 20, 24, 30, 32, 40, 48} = 921.6M, 1228.8M, 1474.56M, 1843.2M, 1966.08M, 2457.6M, 2949.12M			Hz
Single ended output frequency	LVCMOS outputs	$F_{OUT,SE}$	1		250 M	Hz
PLL loop bandwidth	Programmable	F_{BW}	0.00009		4000	Hz
Jitter peaking[4]	Meets SONET Jitter Peaking requirements in closed loop (see footnote)	J_{PEAK}			0.1	dB
Time delay before the Historical average for output frequency is considered.	Programmable in register map	H_{DELAY} [5]	0.035	0.5	35	S
Length of time for which the Average of the frequency is considered	Programmable in register map	H_{AVG} [5]	0.07	1	70	S
Power Supply to I2C or SPI interface ready	No I2C or SPI transaction valid till 10ms after all power supplies are ramped to 90% of final value.	T_{START}			10	ms
Hold Time for GPIO Latching[6]	Hold time for GPIO latched inputs available on the GPIOs after the RSTB pin is driven from low to high	T_{HOLD} [6]	1			ms
DCO Mode Frequency Step Resolution[7]	Frequency Increment or Decrement resolution. This is controlled through the register map.	$F_{RES,DCO}$ [7]		0.0625		Ppt
Output Phase Shift [8]	Resolution for output delay between clocks from same PLL. Resolution Programmable per output clock with this resolution for a total delay range of ±T/2 where T is the time period of the output clock	T_{RESO} [8]		35		Ps
Output Skew[9]	Skew between outputs from the same PLL set up with same phase shift code	T_{SKEW} [9]	-50		50	Ps
Input Phase Shift Resolution[10]	Programmable delay resolution for all outputs that are locked to a particular input. Input phase shift is programmable per input clock with this resolution for a total delay of ±T/2 where T is the time period of the input clock	T_{RESI} [10]	10			Ps
PLL Lock Time[11]	Standard Mode	T_{LOCK}		300m		Sec

Description	Conditions	Symbol	Min	Typ	Max	Units
	1 PPS Mode, Frequency Lock to within 1ppb	$T_{LOCK\_FREQ\_1PPS}$			30	Sec
	1 PPS Mode, Input to Output Phase Error < +/- 30ns	$T_{LOCK\_PHASE\_1PPS}$			30	Sec
Maximum Phase Hit[12]	Default PBO Hitless Switching Mode (no phase propagation)	T_{MAX} [12]	-25		25	Ps
Input to Output Delay in external ZDB mode (external ZDB with feedback on the PCB)[13]	Any output to any input external feedback is possible. Supported for all PLLs. Multiple PLLs in external ZDB are supported concurrently	T_{ZDELAY}	-100		100	Ps
Temperature Variation of delay in external ZDB mode[13]		$T_{ZDELAY,TMP}$			1	ps/C
Internal ZDB Mode Input to Output Delay[14]	Supported for all PLLs. Multiple PLLs in internal ZDB are supported concurrently.	$T_{ZDELAY,INT}$	-500		500	Ps
Uncertainty in Input to Output Delay	Maximum variation in the static delay from input to output clock between repeated power ups of the chip	ΔT_{DELAY}	-175		175	Ps
PLL Pull Range		ω_P		500		Ppm

Notes:

1. The continuous frequency support implies that all output frequencies till 800 MHz are available with no gaps.
2. The VCOs support two ranges: A Low Band Range of 4843.75 MHz to 5898.24 MHz and a High Band Range of 6875 MHz to 8000 MHz. Along with the fully flexibly output multiplexer for the output clocks, this provides for customer use cases to be easily supported with several concurrent frequencies for application scenarios possible from a single PLL.
3. Specific multiples of 61.44 MHz are provided for Wireless applications. Please contact Aura Semiconductor for more frequency options and details.
4. Jitter peaking limit of < 0.1 dB can be enabled as an option for cases (such as SONET) where there is such a critical requirement. For other cases, the jitter peaking can be made slightly higher to enable faster transients and lock characteristics.
5. Hitless Switching enables PLL to switch between input clocks when the current clock is lost,
   a. Clock Loss can be defined as a specified number of consecutive missing pulses.
   b. Priority list for the input clocks can be set in the register map independently for each PLL.
   c. Output is truly hitless (no phase transient and 0 ppb relative error in frequency) for exactly same frequency input clocks that are switched in Phase Build Out Mode. Please refer to the relevant clock switching application notes for various switching modes/ options available in Au5508.
   d. Hitless switching support is both revertive and non-revertive
   e. Revertive / Non-revertive Support: Assume Clock Input 0 is lost and switch is made to Clock Input 1. Then, PLL reverts to Clock Input 0 when it becomes valid again in Revertive mode. It does not switch back to Clock Input 0 even when it becomes valid again in the non-Revertive mode.
   f. Entering hold over mode is supported with the frequency frozen at a historical average determined from the H_{DELAY} and H_{AVG} settings.



6. The Au5508 chip provides a GPIO latching function that allows for certain GPIOs to function as latched GPIOs that are latched along with the release of chip reset (using the RSTB pin) and can the same pin is released for other functions in steady state.
   a. This requires the RSTB pin to be held low and released from low to high ONLY when all supplies to the chip have crossed 90% of their final value.
   b. This further requires that the GPIOs whose inputs are used for GPIO latching should "Hold" the expected value for latching for at least 1ms of time after the RSTB pin has reached 90% of the VDDIO supply.
7. The 1/16 ppt specification is for the smallest frequency step resolution available. Larger frequency step resolutions up to 100 ppm can be used also. The frequency resolution for the DCO mode frequency step is independently programmable for each DCO step.

a. DCO steps are applicable on both XO referenced PLLs (free run) and input referenced PLL (sync mode)
b. DCO step size is programmed in the programmable interface (PIF) using the serial I2C or SPI interface
c. DCO is enacted in response to a trigger. This trigger can be provided either with a register based write through the serial interface or a pin-based trigger where a GPIO is programmed for the purpose of the increment and decrement DCO trigger.

8. The delay referred to here is delay between outputs from the same PLL. Such a delay can delay a clock by as much as 180 degrees which is half of a time period of the output clock with the resolution of 35 ps.
   a. All output clocks from one specific PLL are phase aligned by default. Relative delay adjustment is then possible on each clock individually as defined by the T_{RES} parameter for a total delay range of ±T/2 where T is the time period of the output clock.
9. This is the skew between outputs from the same PLL such that they are set up with the same relative output phase shift code.
10. The delay referred to here is from input to output hence it appears in the system as an input phase shift. All outputs from a PLL that is locked to a particular input can move by as much as 180 degrees of the input clock for the PLL (which is half the time period for the PLL input clock) and with a resolution of +/- 10ps.
11. For low PLL Loop Bandwidths, wake up time can be very large unless the speed up features are used. The speed up feature provides the user options to use a completely independent time constants for the wake-up transitioning to the regular bandwidth after frequency and phase are locked
    a. Fast Lock Bandwidth needs to be less than 100 times smaller than the input clock frequency (divided input at PLL phase detector) for stable and bounded (in time) lock trajectory of the PLL
    b. 1 PPS locking has extra features inbuilt especially with respect to facilitating the sub +/- 30ns phase lock in addition to the frequency lock within the 30 seconds specification
12. This test is for 2 inputs at 8M that are switched to get a 156.25M output.
13. Both input and feedback at 8MHz with the delays exactly matched and same slew for both for the chip
14. Internal ZDB mode is supported concurrently on any number of PLLs. The delay specification here is for delay between the input port and output port of the chip.
15. With PLL A and B configured in Internal ZDB mode, only internal feedback frequency can be brought out on OUT0 and with PLL C and D configured in Internal ZDB mode, only internal feedback frequency can be brought out on OUT11.

Table 8 Fault Monitoring Indicators

Description	Conditions	Symbol	Min	Typ	Max	Units
Clock Loss Indicator Thresholds	Clock Loss Indicators can be set on any of the four inputs. Loss of 2 / 4 / 8 / 16 consecutive pulses can be used to indicate a clock loss. Programmable in the register map.	CL_X [1,4]	2	4	16	Pulses
Fine Frequency Drift Indicator Thresholds: Step Size	Frequency drift threshold is programmable in the range with the step size resolution specified. Frequency drift hysteresis is programmable in the range with the step size resolution specified.	FD_X [2,3,4]		±2		Ppm
Fine Frequency Drift Indicator Thresholds: Hysteresis Range			±2		±500	Ppm
Fine Frequency Drift Indicator Thresholds: Range			±2		±500	Ppm
Coarse Frequency Drift Indicator Thresholds	Coarse Drift Indicators programmable from {Up to ±1600 ppm in steps of ± 100 ppm}		±100		±1600	Ppm
Phase Lock Loss Indicator	Provides phase locking indication for lock of the input and feedback clock phases with respect to each other for each PLL. This is particularly useful for 1 PPS lock	LLPH	1n		100u	Sec

Description	Conditions	Symbol	Min	Typ	Max	Units
Lock Loss Indicator Threshold	Lock Loss Indicator threshold is programmable in the range specified from the following choices for setting and clearing LL: {±0.2, ±0.4} ppm, {±2, ±4} ppm, {±20, ±40} ppm, {±200, ±400} ppm, {±2000, ±4000} ppm	LL	±0.2		±4000	Ppm

Notes:
1. Clock Loss Indicators are used for:
   a. Hitless Switching Triggers
   b. Update in Status Registers in the register map
2. Frequency Drift Indicators can use any one of the ten input clocks or the Crystal / Reference input clock as the golden reference with respect to which FDx for all other clocks can be recorded in the Status Registers. FDx thresholds for each clock input for each clock can be set independently.
3. Coarse and Fine Frequency Drift indicators can be concurrently enabled. This enables the user to detect fast drifting frequencies since detecting fine drifts will take longer measurements.
4. Clock loss and Lock loss indicators are available as alerts on GPIO pins as described in Section 7.1 in the full Datasheet
5. Clock Loss can be combined with either of the frequency drift monitors (coarse and fine) to trigger the hitless switching event in the PLLs. The trigger for a hitless switching event in the PLL can therefore be either the Clock Loss event or either of Clock Loss or Frequency Drift.

Table 9 Crystal Requirements

Description	Conditions	Symbol	Min	Typ	Max	Units
High Fundamental Frequency Crystal Reference (HFF)						
Crystal Frequency	Can be supported with a fundamental crystal of 100-160 MHz range.	$XTAL_{IN}$	100		160	MHz
C0 cap for crystal	Small range around CL only	$XTAL_{C0}$			2	pF
CL cap for crystal		$XTAL_{CL}$		5		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$			40	Ω
Rm1 for crystal		$XTAL_{Rm1}$			20	Ω
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW
Low Frequency Fundamental Crystal (LFF)						
Crystal Frequency	Can be supported with a fundamental crystal > 25 MHz range. For Best Performance use an LFF crystal > 48 MHz	$XTAL_{IN}$	25		54	MHz
C0 cap for crystal	Small range around CL only	$XTAL_{C0}$			2	pF
CL cap for crystal [2]		$XTAL_{CL}$		8		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$ [1]			40	Ω
Rm1 for crystal		$XTAL_{Rm1}$			40	Ω
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW

Notes:

1. ESR relates to the motional resistance Rm with the relationship $ESR = Rm\ (1 + C0/CL)2$
2. The table specifies the Ci, Ce and Cs for the 54MHz XTAL with different CL. Ci is the internal differential capacitance offered by the chip whereas Ce (Ce=Ce1=Ce2) and Cs(Cs=Cs1=Cs2) are the Single Ended external and the stray cap on the PCB.

XTAL	Ci	Ce	Cs	Unit
54MHz (CL = 8pF)	7.5	0	1	pF
54MHz (CL = 12pF)	8.1	7	1	pF

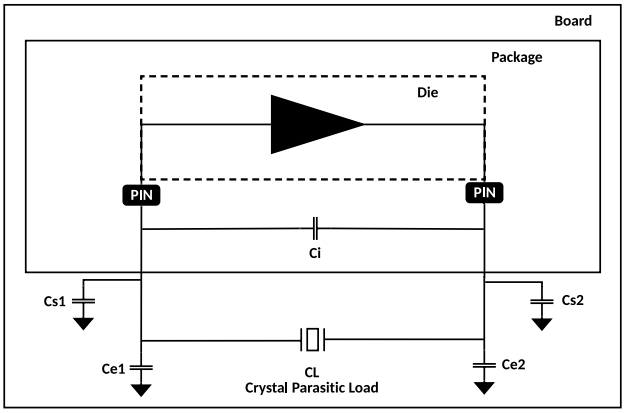


Table 10 Output RMS Jitter in Frequency Translation Modes

Description	Conditions	Symbol	Min	Typ	Max	Units
RMS Jitter for 12 kHz – 20 MHz Integration Bandwidth F_{IN} = 38.88 MHz, PLL BW = 100 Hz, Single PLL Profile	F_{OUT} = 156.25 MHz 54 MHz Crystal [3]	RMS_{JIT} [1,2]		120		fs rms
	F_{OUT} = 156.25 MHz 54 MHz External XO [4]			130		fs rms

Notes:
1. For best noise performance in jitter attenuation mode, use lowest usable loop bandwidth for the PLL.
2. Does not include noise from the input clocks to the PLL
3. Crystal is assumed to meet the specifications mentioned in this data sheet
4. External XO with a CMOS drive such as TXC 7X54000007 is assumed

Table 11 Close-In Offset Phase Noise

Description	Conditions	Symbol	Min	Typ	Max	Units
Phase Noise Skirt F_{IN} = 38.88 MHz F_{OUT} = 122.88 MHz, PLL BW = 100 Hz 54 MHz Crystal [2]	Offset Frequency = 100 Hz	PN[1]		-103		dBc/Hz
	Offset Frequency = 1 kHz			-123		
	Offset Frequency = 10 kHz			-138		
	Offset Frequency = 100 kHz			-143		
	Offset Frequency = 1 MHz			-154		
	Offset Frequency = 10 MHz			-160		
Phase Noise Skirt F_{IN} = 38.88 MHz F_{OUT} = 122.88 MHz, PLL BW = 100 Hz 54 MHz External XO[3]	Offset Frequency = 100 Hz	PN[1]		-114		dBc/Hz
	Offset Frequency = 1 kHz			-128		
	Offset Frequency = 10 kHz			-138		
	Offset Frequency = 100 kHz			-142		
	Offset Frequency = 1 MHz			-152		
	Offset Frequency = 10 MHz			-160		

Notes:
1. This is the noise contribution of the chip only without including the input and reference self-contributions.
2. Crystal is assumed to meet the specifications mentioned in this data sheet
3. External XO with a CMOS drive such as TXC 7X54000007 is assumed.

Table 12 Power Supply Rejection

Description	Conditions	Symbol	Min	Typ	Max	Units
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on PLL Supply	VDD_3V3 = 3.3 V	$PSRR_{VDD}$		-80		dBc
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on Input Supply	VDDIN = 3.3 V	$PSRR_{VDDIN}$		-80		dBc
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on Output Driver Supply	VDDO = 3.3 V	$PSRR_{VDDO}$		-80		dBc

Notes:
1. The PSRR is measured with a 50 mVpp sinusoid in series with the supply and checking the spurious level relative to the carrier on the output in terms of phase disturbance impact.
2. Output PSRR measured with LVDS standard which is the recommended standard for AC Coupled terminations

Table 13 Adjacent Output Cross Talk

Description	Conditions	Symbol	Min	Typ	Max	Units
156.25 M and 155.52 M on adjacent outputs	LVDS Output	X_{TALK}		-75		dBc

Notes:
1. Measured across adjacent outputs- All adjacent outputs are covered and the typical value for the worst-case output to output coupling is reported.
2. The adjacent output pairs are chosen at 155.52 MHz and 156.25 MHz frequencies.
3. This cross talk between outputs is mainly package dependent therefore terminated outputs are used for reporting these numbers ensuring that there is signal current in the bond wires.

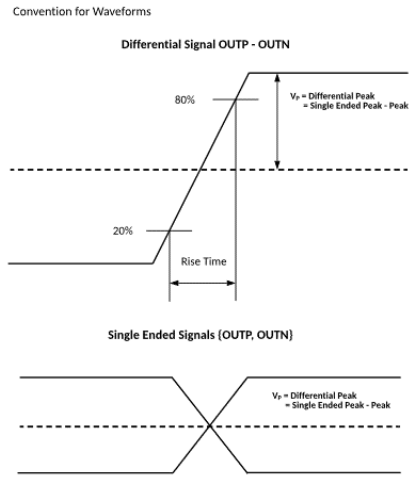
Table 14 Output Clock Specifications

Descriptions	Conditions	Symbol	Min	Typ	Max	Units
DC Electrical Specifications - LVCMOS output (Complementary Out of Phase Outputs or One CMOS Output per Output Driver)						
Output High Voltage	4 mA load, VDD = 3.3 V	V_{OH}	VDDO-0.3		-	V
Output High Voltage	4 mA load, VDD = 1.8V and 2.5 V	V_{OH}	VDDO-0.4		-	V
Output Low Voltage	4 mA load	V_{OL}			0.3	V
DC Electrical Specifications - LVCMOS output (In Phase Outputs)						
Output High Voltage	4 mA load, VDD = 3.3 V	V_{OH}	VDDO-0.35		-	V
Output High Voltage	4 mA load, VDD = 2.5 V	V_{OH}	VDDO-0.45		-	V
Output High Voltage	4 mA load, VDD = 1.8 V	V_{OH}	VDDO-0.5		-	V
DC Electrical Specifications – LVDS Outputs (VDDO = 1.8 V, 2.5 V or 3.3 V range)						
Output Common-Mode Voltage	VDDO = 2.5 V or 3.3 V range	V_{OCM}	1.125	1.2	1.375	V
Output Leakage Current	Output Off, VOUT = 0.75 V to 1.75 V	I_{OZ}	-20		20	µA
AC Electrical Specifications LVCMOS Output Load: 10 pF < 125 MHz, 7.5 pF < 150 MHz, 5 pF > 150 MHz > 200 MHz						
Output Frequency		f_{OUT}	0.5		250M	Hz
Output Duty cycle	Measured at 1/2 VDDO, loaded, fOUT < 125 MHz	t_{DC}	45		55	%
Output Duty cycle	Measured at 1/2 VDDO, loaded, fOUT > 125 MHz	t_{DC}	40		60	%
Rise/Fall time	VDDO = 1.8 V, 20-80%, Highest Drive setting	t_{RFCMOS}			2	Ns

Descriptions	Conditions	Symbol	Min	Typ	Max	Units
Rise/Fall time	VDDO = 2.5 V, 20-80%, Highest Drive setting	t_{RFCMOS}			1.5	Ns
Rise/Fall time	VDDO = 3.3 V, 20-80%, Highest Drive setting	t_{RFCMOS}			1.2	Ns
AC Electrical Specifications (LVPECL, LVDS, CML)						
Clock Output Frequency		f_{OUT}	0.5		2949.12 M	Hz
PECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for PECL outputs.	t_{RF}			350	Ps
CML Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for CML outputs	t_{RF}			350	Ps
LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	t_{RF}			350	Ps
HCSL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for HCSL outputs.	t_{RF}			350	Ps
Output Duty Cycle	Measured at differential 50% level, 156.25 MHz	t_{ODC}	45	50	55	%
Programmable Output differential peak LVDS DC Coupled Output [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned)	VP	100, 200, 300, 400, 500, 600, 700, 800			mV
Programmable Output differential peak LVDS AC Coupled Output [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned)	VP	100, 200, 300, 400, 500, 600, 700, 800			mV
Programmable Output differential peak LVDS DC Coupled Output with Internal Termination [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) No Far End Termination assumed	VP	100, 200, 300, 400, 500, 600, 700, 800			mV
Programmable Output differential peak LVDS AC Coupled Output with Internal Termination [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) No Far End Termination Assumed	VP	100, 200, 300, 400, 500, 600, 700, 800			mV
Programmable Output differential peak LVDS DC Coupled Output with Internal Termination [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) Differential 100 Ohm Far End Termination assumed	VP	100, 150, 200, 250, 300, 350, 400			mV
Programmable Output differential peak LVDS AC Coupled Output with Internal Termination [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) Differential 100 Ohm Equivalent Far End Termination Assumed	VP	100, 150, 200, 250, 300, 350, 400			mV
Programmable Output differential peak HCSL Coupled Output [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) DC Coupled True HCSL termination assumed. See foot note	VP	500,550,600,650,700,750,800			mV
Programmable Output differential peak CML Coupled Output [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) DC Coupled True CML termination assumed. See foot note	VP	50, 100, 150, 200, 250, 300, 350, 400			mV
Programmable Output differential peak LVPECL Coupled Output [1],[2]	Measured at 156.25M Output (Programmable Typical Levels mentioned) DC Coupled True LVPECL termination assumed. See foot note	VP	500,540,580,620,660,680,700,720			mV

Notes:

1.



2. Please see Section 9 in the full Datasheet related to the output slave to determine the output termination supported as per standard.
   a. LVDS standard is recommended for most AC Coupled termination cases OR DC coupled differential 100 Ohm loading
   b. LVPECL Standard mentioned here supports the true traditional standard with DC coupled 50 Ohm terminations to VDDO- 2V or its corresponding Thevenin equivalent network.
   c. CML Standard mentioned here supports the true traditional standard with DC coupled 50 Ohm terminations to VDDO supply.
   d. HCSL Standard mentioned here supports the true traditional standard with DC coupled 50 Ohm terminations to Ground which are then AC or DC coupled to a differential receiver

3 Functional Description

The Au5508 is a jitter attenuating frequency translation device that offers four independent PLLs. The fully integrated part offers IEEE1588/ SyncE / 1 PPS full support along with low integrated jitter for higher data rate links along with low close-in noise and full JESD204B/C support for AAU RF clocks. These features provide a unique feature rich definition in a highly integrated part.

The five unique differential (or 10 single ended) clocks can be routed to any of the four independent PLLs as well as a high precision independent input TDC (time to digital converter) that can be used to measure any relative phase delays between inputs. A fully flexible output RF multiplexer allows any PLL's output to be routed to any output. This offers a very flexible frequency translation arrangement with independent control of each PLL in terms of jitter attenuation, bandwidth control and input clock selection with redundancy. The hierarchy of the clocks, nomenclature of the various frequency dividers as well as the clock translation pathways available on the chip are shown in Figure 3, Figure 4, and Figure 5.

The digital architecture of the chip is partitioned into a master digital controller and nine slave controllers. The master controller and each of the nine controllers has an associated volatile programmable interface (PIF). The overall PIF structure is a register map that is divided into several pages according to function. Each controller (master and slaves) has an associated unique Page number. Each Page has an independent 8 bit addressable PIF memory. In all the pages, the last address, FF, holds the current page number and is reserved for changing the page. The current page to be communicated with, can be set by writing the page number in hexadecimal form {0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E} corresponding to pages {0, 1, 2, 3, 4, 5, 6, 7, A, B, C, D, E} in the address FF on any page.

- Page 0,1: Master System
- Page 2: Input System
- Page 3,4: Output System
- Page A: High Performance PLL A
- Page B: High Performance PLL B
- Page C: High Performance PLL C
- Page D: High Performance PLLD
- Page E: Frequency track PLL (FTPLL) for OCXO based tracking and auxiliary functionality
- Page 5: Input TDC System
- Page 6, 7: Clock Monitor System

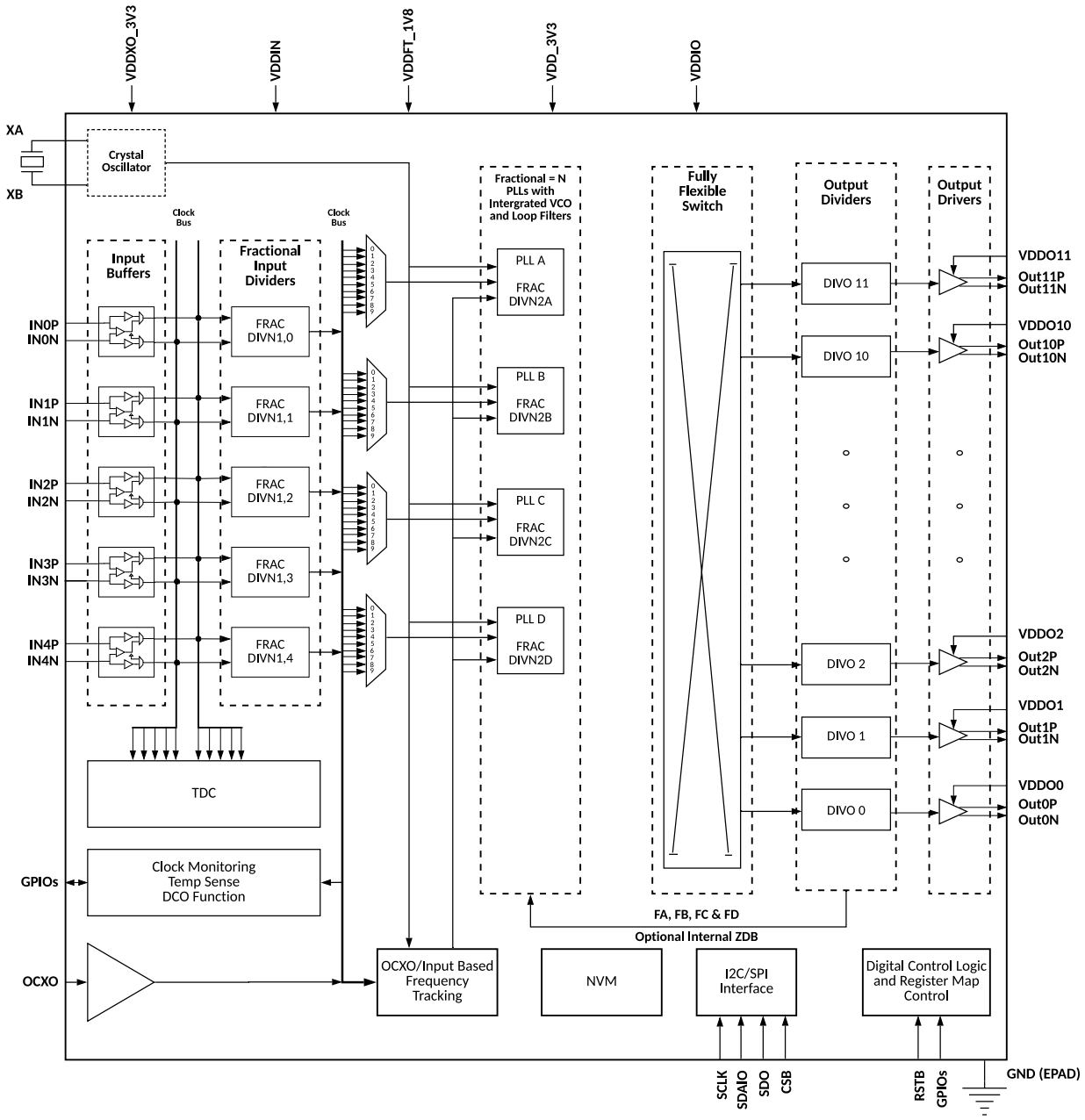


Figure 3 Au5508 Functional Block Diagram

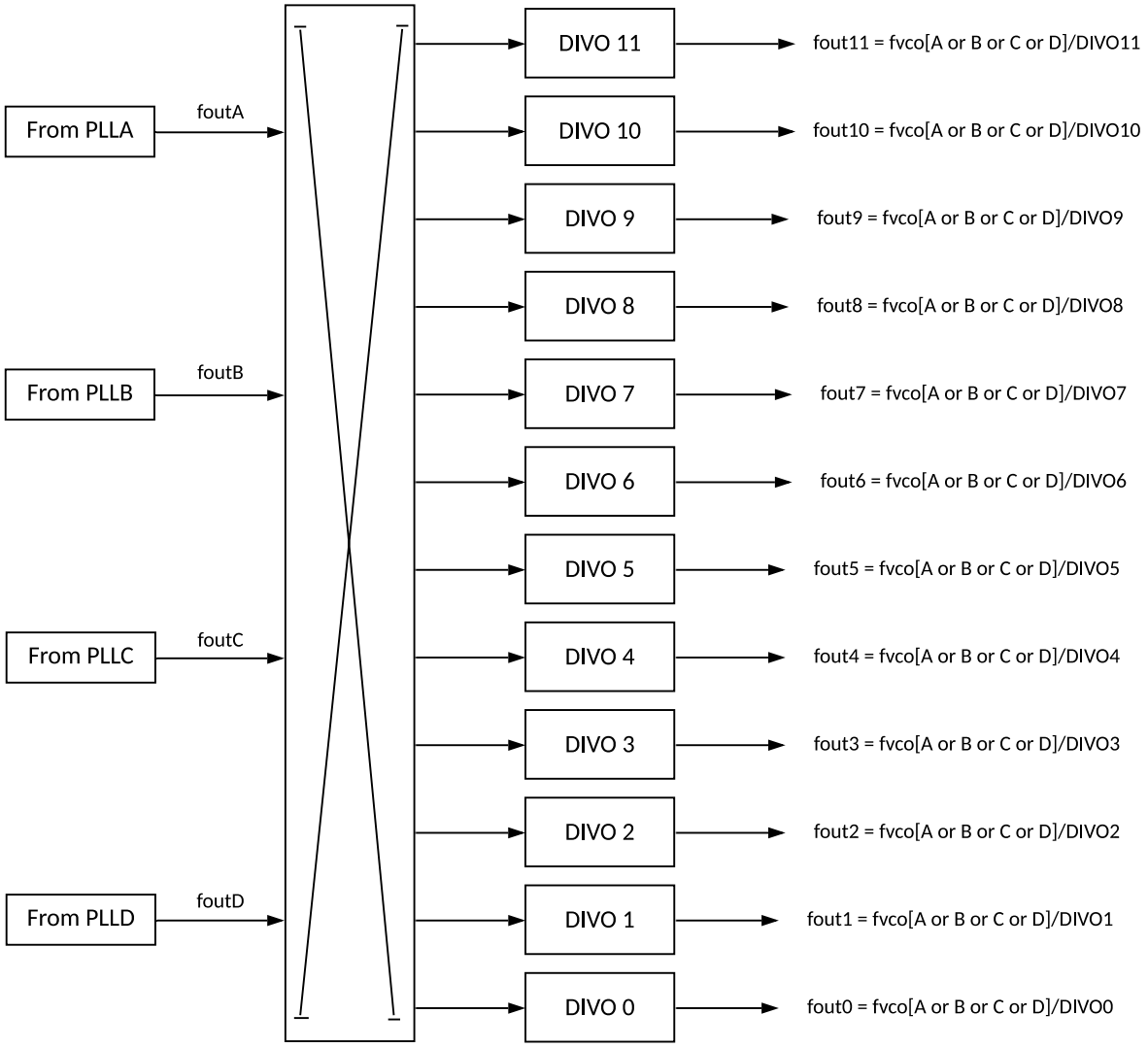


Figure 4 Output Clock Distribution

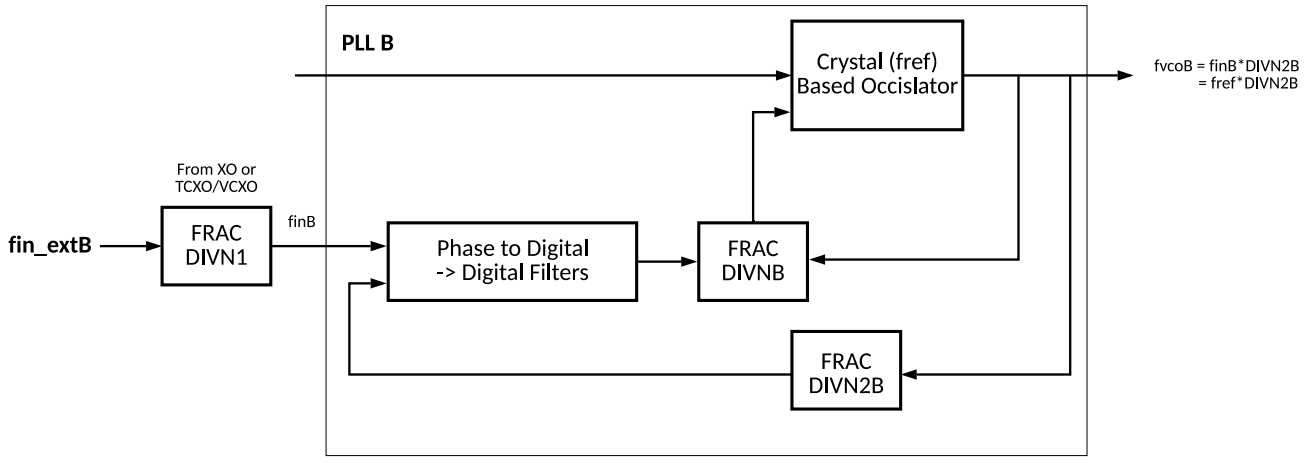


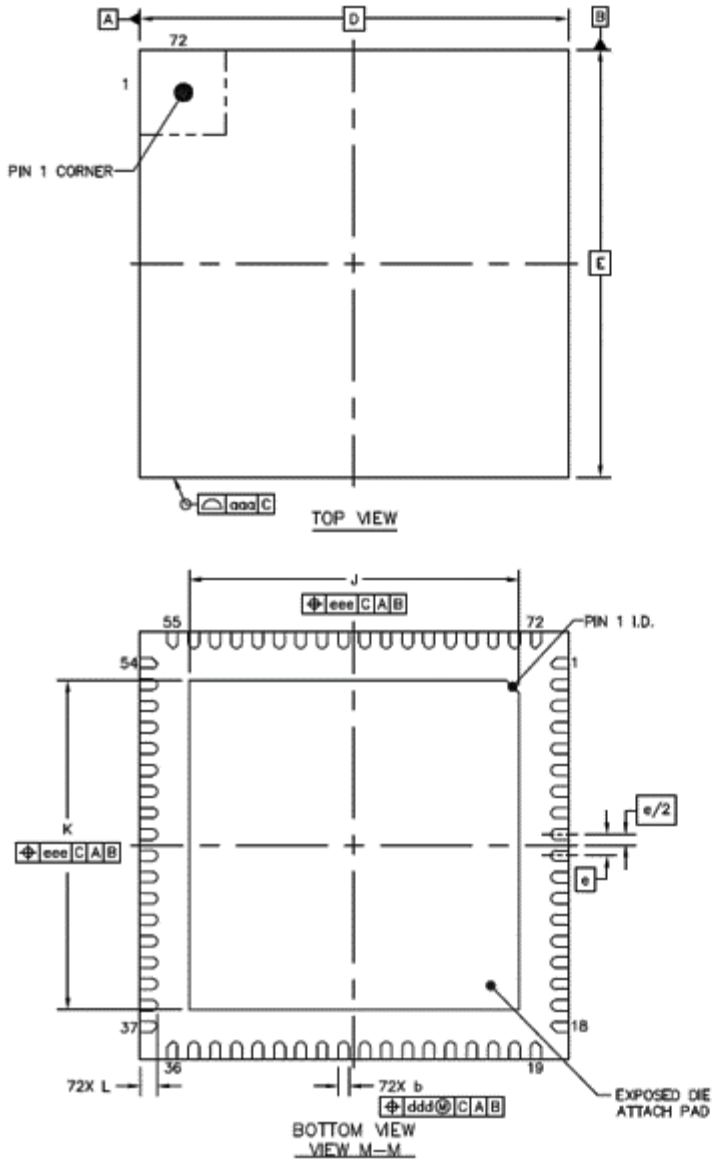
Figure 5 PLL Internals

Note: Similar for all PLLs, shown here for PLL B

Table 15 PIF Description

Page	Contents	Summary of contents
0	Master	All Generic Information related to the chip Chip Configuration details Control for the master sequencer FSM Crystal Reference Related Information
1		
2	Input Slave	Input 4P,4N,3P,3N,2P,2N,1P,1N,0P,0N,OCXO related information (Input type, DIVN1 divider configuration)
3	Output Slave	ODR 11,10,9,8,7,6,5,4,3,2,1,0. ODR Standards, DIVO, Programmable delay configurations for each
4		Fixed Outputs 0T / 0B (ODR Standards, DIVO, Programmable delay configurations for each)
5	Input TDC Slave	Phase delay detection for 10 Pairs up to 10 different clocks
6	ClkMon Slave	Clock Loss related Function. Frequency Drift related function
7		
A	PLL A Slave	All PLL related functionality
B	PLL B Slave	All PLL related functionality
C	PLL C Slave	All PLL related functionality
D	PLL D Slave	All PLL related functionality
E	FTPLL Slave	All FTPLL related functionality

4 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 6 Package Information

5 Revision History

Table 16 Revision History

Revision	Date	Description	Author
0.1	1st June 2021	Au5508 Short Data Sheet created	Aura Semi

6 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

7 Contact Information

For more information visit **www.aurasemi.com**

For the full Datasheet and other sales related information please contact your local Sales/FAE or send an email to **sales@aurasemi.com**

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