Data Sheet

ADCA5191

5 MHz to 1800 MHz Broadband CATV Amplifier

FEATURES

- Frequency range of 5 MHz to 1800 MHz
- High gain of 25.8 dB at 1800 MHz
- Excellent reverse isolation: −37 dB typical
- Excellent NPR (MER) performance: 51 dB at 67 dBmV TCP
- Excellent return losses:
  - −20 dB at 45 MHz to 1218 MHz
  - −18 dB at 1218 MHz to 1800 MHz
- V_{DD} operation: 5.0 V to 8.0 V
- Configurable dc current (total) from 250 mA to 530 mA
- 32-lead, 5 mm x 5 mm, LFCSP

APPLICATIONS

- 45 MHz to 1800 MHz CATV infrastructure amplifier systems
- 5 MHz to 700 MHz upstream
- Remote physical layer (PHY)
- DOCSIS® 3.1 and DOCSIS 4.0 compliant

FUNCTIONAL BLOCK DIAGRAM

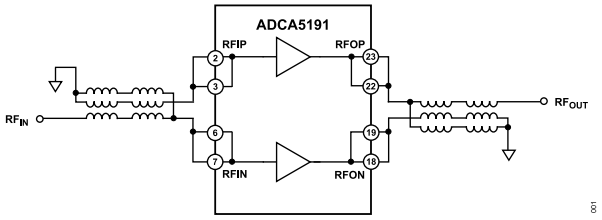

Figure 1.

GENERAL DESCRIPTION

The ADCA5191 is a medium power gain block amplifier that provides excellent linearity across a flexible bias range allowing power efficient design implementation for various applications.

The device provides 25.8 dB of flat gain up to 1800 MHz, making this ideal for Data Over Cable Service Interface Specification (DOCSIS) 4.0 downstream applications. The device is also well suited for upstream applications to 700 MHz as the output stage. It is conveniently packaged in an industry-standard, 5 mm × 5 mm, 32-lead, lead frame chip-scale package (LFCSP) with an exposed pad on the bottom of the package for improved thermal performance.

Rev. A

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REVISION HISTORY

8/2022—Rev. 0 to Rev. A

Changes to Figure 39 ... 19
Changes to Table 10 ... 20

5/2022—Revision 0: Initial Version

SPECIFICATIONS

GENERAL DOWNSTREAM PERFORMANCE

See the application circuit in Figure 39. Supply voltage (V_{DD}) = 8.0 V, supply current (I_{DD}) = 470 mA, paddle temperature (T_{PADDLE}) = 35 °C, and source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 1. Downstream Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BANDWIDTH		45		1800	MHz	
POWER GAIN	S21		25.7		dB	f = 45 MHz
			25.8		dB	f = 1218 MHz
			25.8		dB	f = 1800 MHz
SLOPE OF STRAIGHT LINE[1]			0.1		dB	f = 45 MHz to 1218 MHz
			0.1			f = 45 MHz to 1800 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.1		dB	f = 45 MHz to 1800 MHz
INPUT IMPEDANCE	Z_{IN}		37.5		Ω	RFIP and RFIP
REVERSE ISOLATION	S12		−37		dB	f = 45 MHz to 1800 MHz
OUTPUT INTERMODULATION DISTORTION						
Third-Order Intercept Point	OIP3		47		dBm	f_1 = 50 MHz to 1800 MHz, tone spacing = 6 MHz, 9 dBm per tone
Second-Order Inercept Point						
Low-Side	OIP2L		73		dBm	f_1 = 50 MHz to 1750 MHz, tone spacing = 50 MHz, 9 dBm per tone
High-Side	OIP2H		65		dBm	f_1 = 50 MHz to 850 MHz, tone spacing = 50 MHz, 9 dBm per tone
OUTPUT IMPEDANCE	Z_{OUT}		37.5		Ω	RFOP and RFON
RETURN LOSS						
Input	S11		−20		dB	f = 45 MHz to 1218 MHz
			−20		dB	f = 1218 MHz to 1800 MHz
Output	S22		−20		dB	f = 45 MHz to 1218 MHz
			−18		dB	f = 1218 MHz to 1800 MHz
NOISE FIGURE						Includes losses of baluns shown in Downstream Applications Circuit
			3.4		dB	f = 45 MHz
			3.8		dB	f = 1218 MHz
			5.2		dB	f = 1800 MHz
SUPPLY						
Operating Voltage	V_{DD}	5.0		8.0	V	Can be biased between 5.0 V and 8.0 V
DC Current (Total)	$I_{DD\ (TOTAL)}$		470		mA	Can be biased between 250 mA and 530 mA

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.

[2] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

SPECIFICATIONS

GENERAL UPSTREAM PERFORMANCE

See the application circuit in Figure 40. V_{DD} = 8.0 V, I_{DD} = 470 mA, T_{PADDLE} = 35 °C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 2. Upstream Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BANDWIDTH		5		700	MHz	
POWER GAIN	S21		24.7		dB	f = 5 MHz
			24.8		dB	f = 204 MHz
			24.7		dB	f = 684 MHz
FLATNESS OF FREQUENCY RESPONSE[1]	FL		0.1		dB	f = 5 MHz to 684 MHz
REVERSE ISOLATION	S12		−37		dB	f = 5 MHz to 684 MHz
RETURN LOSS						
Input	S11		−19		dB	f = 5 MHz to 204 MHz
			−22		dB	f = 204 MHz to 684 MHz
Output	S22		−24		dB	f = 5 MHz to 204 MHz
			−24		dB	f = 5 MHz to 684 MHz

[1] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

DISTORTION DATA

Downstream All Digital Channel Plan, 8× Orthogonal Frequency Division Multiplexing (OFDM) Channels, 258 MHz to 1794 MHz

See the application circuit in Figure 39. V_{DD} = 8.0 V, I_{DD} = 470 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 3. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			51		dB	10 dB tilt, 6 dB offset at 1026 MHz, total composite power (TCP) = 67 dBmV
			52		dB	10 dB tilt, no offset, TCP = 67 dBmV
			45		dB	0 dB tilt, 6 dB offset at 1026 MHz, TCP = 67 dBmV

[1] The noise power ratio gives an equivalent result to the standard modulation error rate (MER) testing but with improved dynamic range using an industry-accepted method.

SPECIFICATIONS

Downstream All Digital Channel Plan, 190×, ITU-T J.83B, Single-Channel Quadrature Amplitude Modulation (SCQAM) 6 MHz Channels, 54 MHz to 1218 MHz

See the application circuit in Figure 39. V_{DD} = 8.0 V, I_{DD} = 470 mA, T_{PADDLE} = 35 °C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 4. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			52		dB	10 dB tilt, TCP = 68 dBmV
			51		dB	0 dB tilt, TCP = 68 dBmV

[1] The noise power ratio gives an equivalent result to the standard MER testing but with improved dynamic range using an industry-accepted method.

Upstream All Digital Channel Plan, 105×, ITU-T J.83B, SCQAM 6 MHz Channels, 54 MHz to 684 MHz

See the application circuit in Figure 40. V_{DD} = 8.0 V, I_{DD} = 470 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 5. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			53		dB	10 dB tilt, TCP = 68 dBmV
			54		dB	0 dB tilt, TCP = 68 dBmV

[1] The noise power ratio gives an equivalent result to standard MER testing but with improved dynamic range using an industry-accepted method.

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	
DC Supply over Voltage (5 Minutes)	10 V
V_{DD} Bias Supply Current	550 mA
RF Input Power	75 dBmV
Temperature	
Operating Range, T_{PADDLE}	−40°C to +100°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)	260°C
Junction (T_J) to Maintain 1 Million Hour Mean Time to Failure (MTTF)	150°C
Nominal Junction (T_J)	
T_{PADDLE} = 100 °C, I_{DD} = 470 mA, V_{DD} = 8.0 V	132°C
Storage (T_S) Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the pseudomorphic, high electron mobility transistor (pHEMT) device to the outside surface of the package closest to the device mounting area (the exposed pad on the bottom of the case). See the Thermal Considerations section for additional information.

Table 7. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-32-13	8.5	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADCA5191

Table 8. ADCA5191, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	350	Class 1A, passed

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

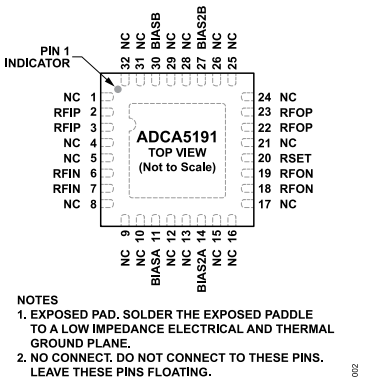

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 5, 8, 9, 10, 12, 13, 15, 16, 17, 21, 24, 25, 26, 28, 29, 31, 32	NC	No Connect. Do not connect to these pins. Leave these pins floating.
2, 3	RFIP	Positive RF Amplifier Input. RFIP and RFIN form a differential input.
6, 7	RFIN	Negative RF Amplifier Input. RFIP and RFIN form a differential input.
11	BIASA	BIASA (together with BIASB) supplies a portion (~10%) of the I_{DD} and controls the overall bias current of the amplifier. Configure the BIASA and BIASB pins as shown in Figure 41 with the bias resistor (R_{BIAS}) controlling I_{DD} as illustrated in Figure 42. Keep the network of passive components between BIASA and V_{DD} close to the device package to minimize parasitics.
14	BIAS2A	BIAS2A (together with BIAS2B) provides additional RF tuning or bias adjustment for special applications. However, BIAS2A and BIAS2B are normally left floating.
18, 19	RFON	Negative Amplifier RF Output. A choke inductor is required to provide dc current and RF isolation. A dc blocking capacitor is also required.
20	RSET	Bias Resistor. Place a 1% resistor between RSET and ground.
22 ,23	RFOP	Positive Amplifier RF Output. A choke inductor is required to provide dc current and RF isolation. A dc blocking capacitor is also required. See Figure 39, and Figure 40 for specific recommendations.
27	BIAS2B	BIAS2B (together with BIAS2A) provides additional RF tuning or bias adjustment for special applications. However, BIAS2B and BIAS2A are normally left floating.
30	BIASB	BIASB (together with BIASA) supplies a portion (~10%) of the I_{DD} and controls the overall bias current of the amplifier. Configure the BIASB and BIASA pins as shown in Figure 41 with R_{BIAS} controlling I_{DD} as illustrated in Figure 42. Keep the network of passive components between BIASB and V_{DD} close to the device package to minimize parasitic.
	EPAD	Exposed Pad. Solder the exposed paddle to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 8.0 V, I_{DD} = 470 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

S-PARAMETERS FOR DOWNSTREAM APPLICATION (SEE FIGURE 39)

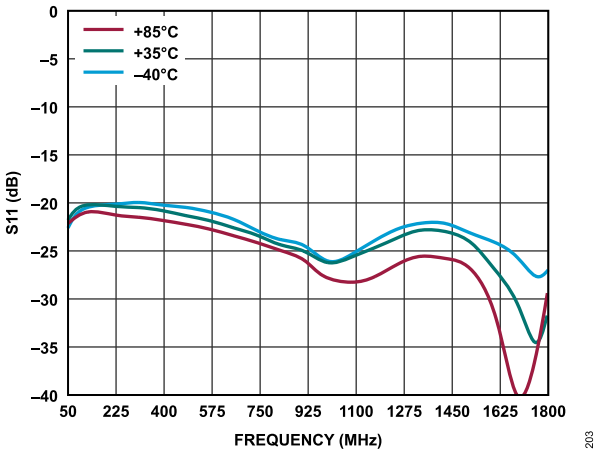

Figure 3. Downstream S11 vs. Frequency Over Temperature, V_{DD} = 8.0 V

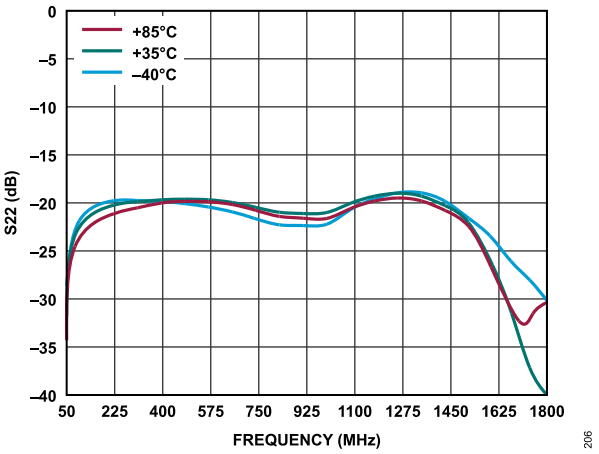

Figure 6. Downstream S22 vs. Frequency Over Temperature, V_{DD} = 8.0 V

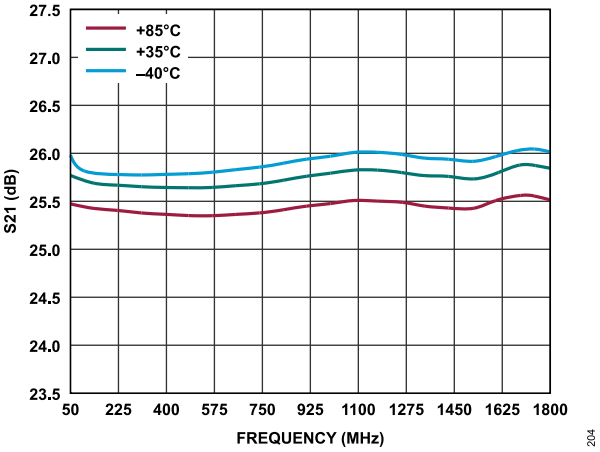

Figure 4. Downstream S21 vs. Frequency Over Temperature, V_{DD} = 8.0 V

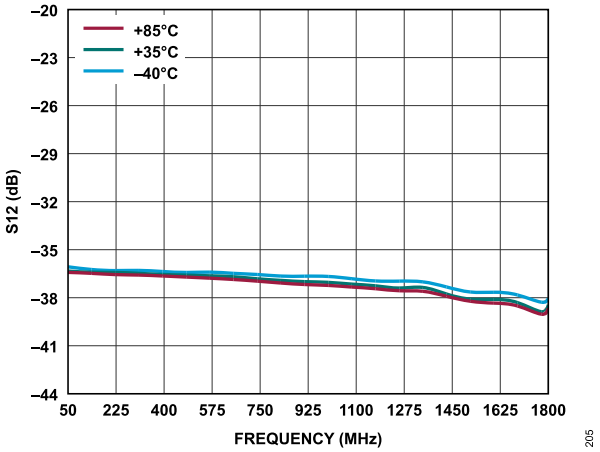

Figure 5. Downstream S12 vs. Frequency Over Temperature, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

S-PARAMETERS FOR UPSTREAM APPLICATION (SEE FIGURE 40)

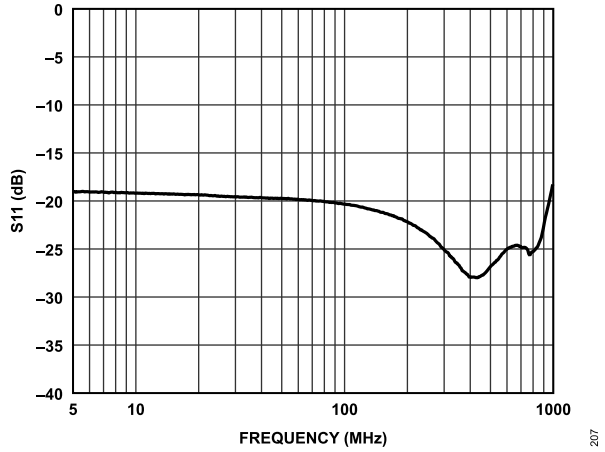

Figure 7. Upstream S11 vs. Frequency Over Temperature

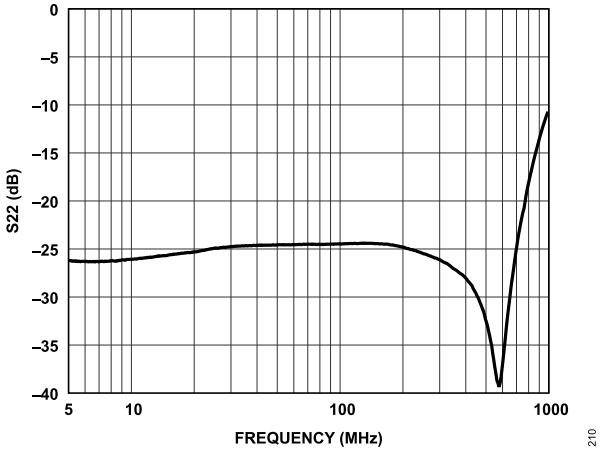

Figure 10. Upstream S22 vs. Frequency Over Temperature

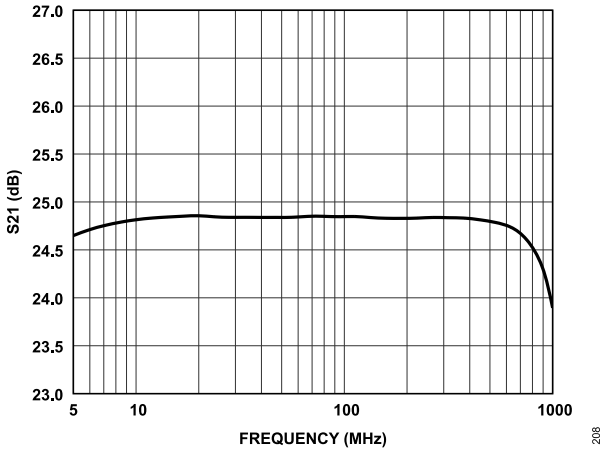

Figure 8. Upstream S21 vs. Frequency Over Temperature

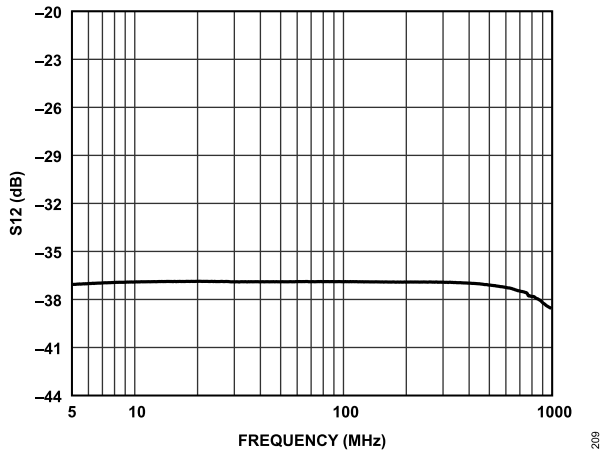

Figure 9. Upstream S12 vs. Frequency Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 4.0 DOWNSTREAM PERFORMANCE (SEE FIGURE 39)

8x OFDM Channels, 258 MHz to 1794 MHz, and 6 dB offset at 1026 MHz, unless otherwise noted. In Figure 11 to Figure 21, the performance at the lower output power is limited by the test equipment and is not indicative of the noise performance of the device.

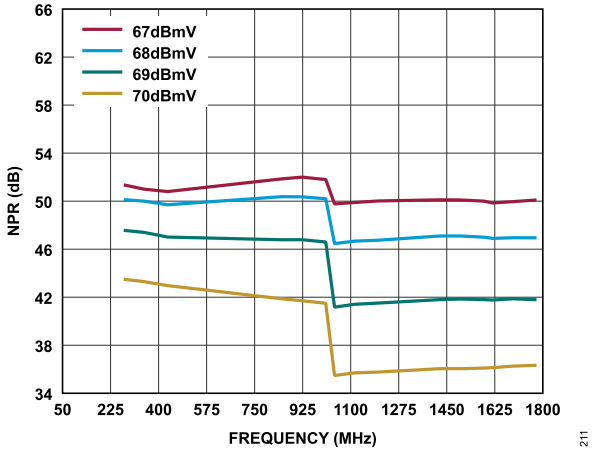

Figure 11. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 8.0 V

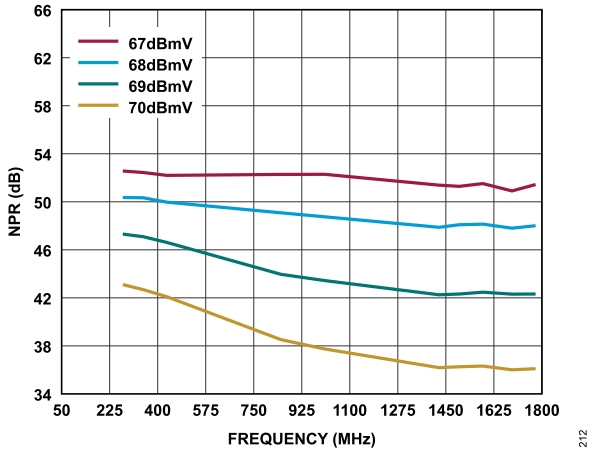

Figure 12. NPR vs. Frequency Over TCP, 10 dB Tilt, No Offset at 1026 MHz, V_{DD} = 8.0 V

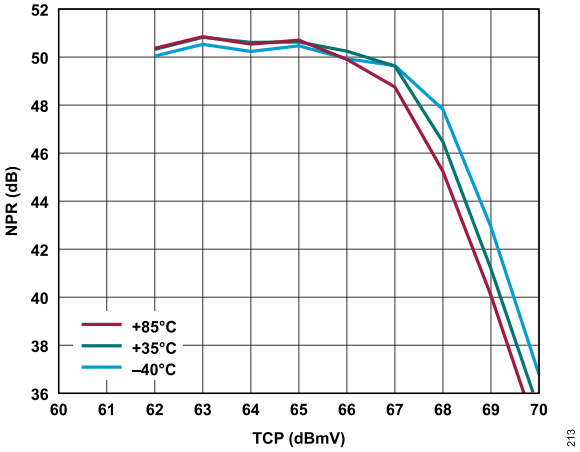

Figure 13. NPR vs. TCP Over Temperature, Worst Case Frequency, 10 dB Tilt, V_{DD} = 8.0 V

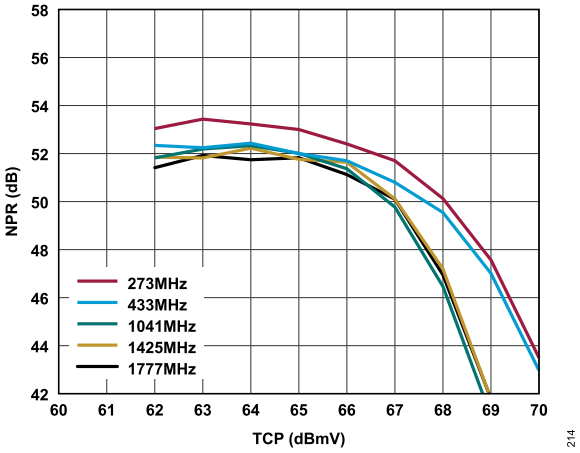

Figure 14. NPR vs. TCP Over Frequency, 10 dB Tilt, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

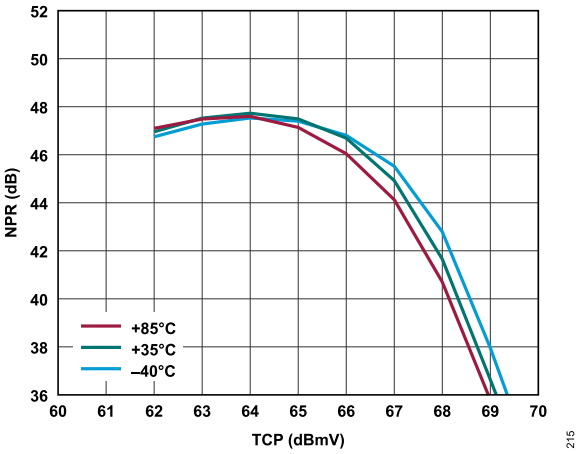

Figure 15. NPR vs. TCP Over Temperature, Worst Case Frequency, 0 dB Tilt, V_{DD} = 8.0 V

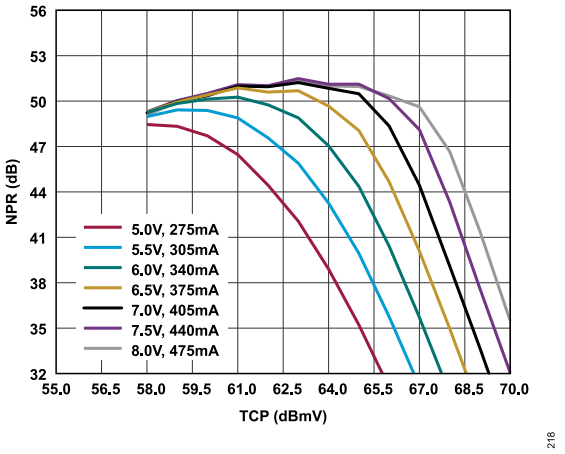

Figure 18. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 33 Ω

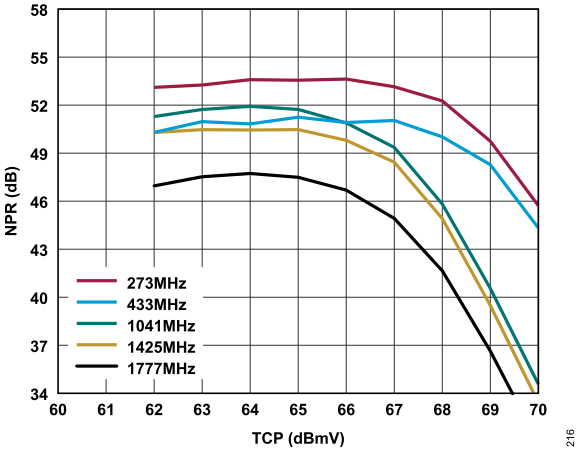

Figure 16. NPR vs. TCP Over Frequency, 0 dB Tilt, V_{DD} = 8 .0 V

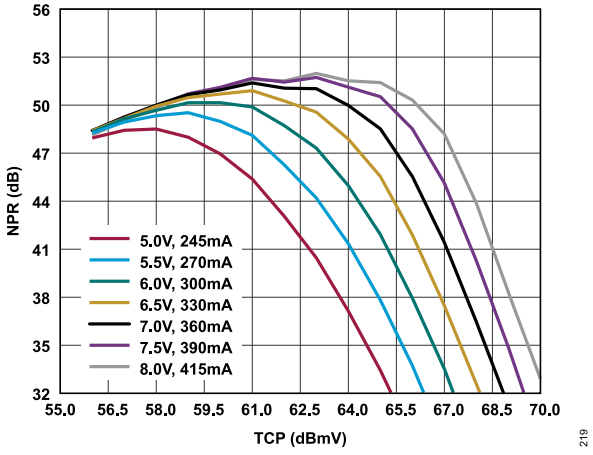

Figure 19. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 50 Ω

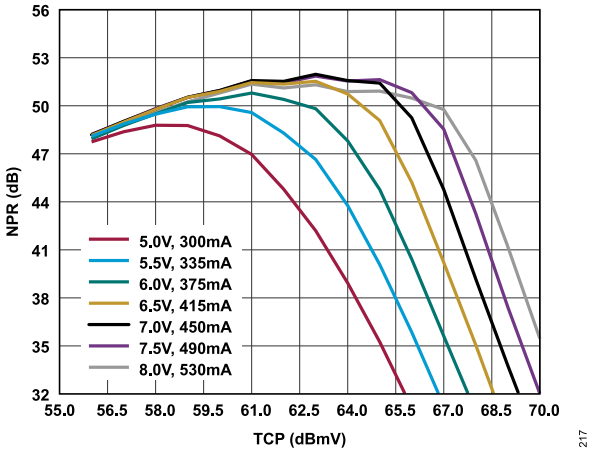

Figure 17. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 16 Ω

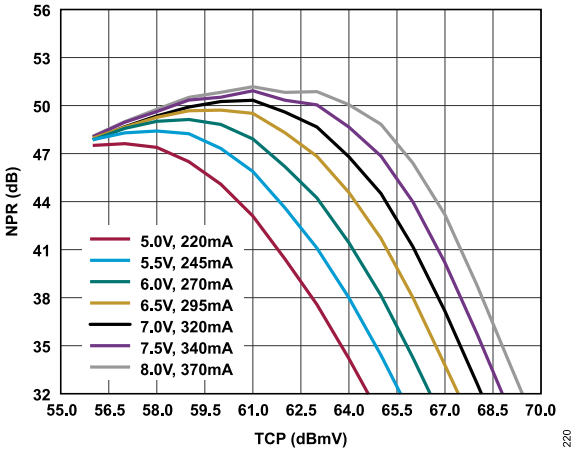

Figure 20. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 75 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

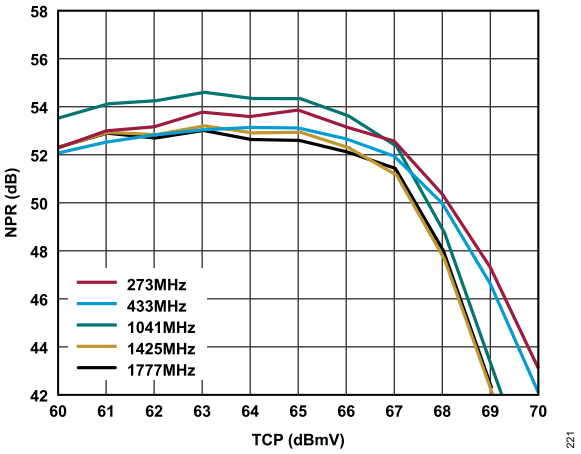

Figure 21. NPR vs. TCP Over Frequency, 10 dB Tilt, No Offset at 1026 MHz, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 3.1 DOWNSTREAM PERFORMANCE (SEE FIGURE 39)

190×, ITU-T J.83B, SCQAM 6 MHz Channels, and 54 MHz to 1218 MHz, unless otherwise noted. In Figure 22 to Figure 30, the performance at the lower output power is limited by the test equipment and is not indicative of the noise performance of the device.

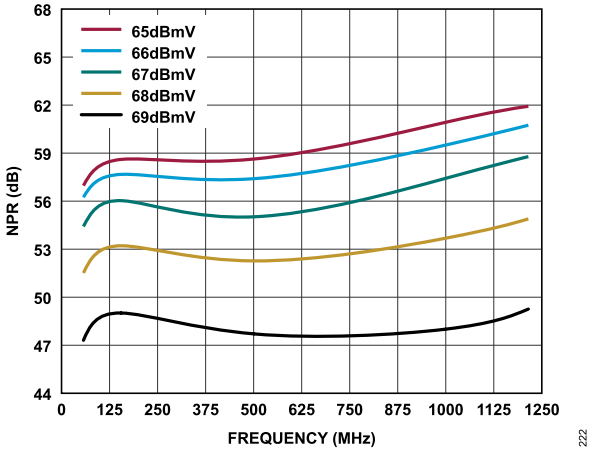

Figure 22. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 8.0 V

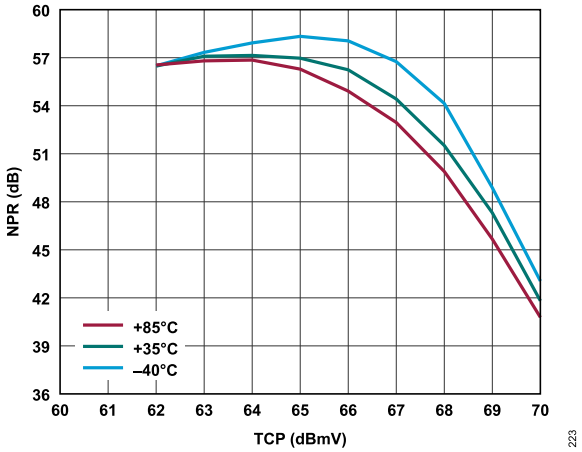

Figure 23. NPR vs. TCP Over Temperature, Worst Case Frequency, 10 dB Tilt, V_{DD} = 8.0 V

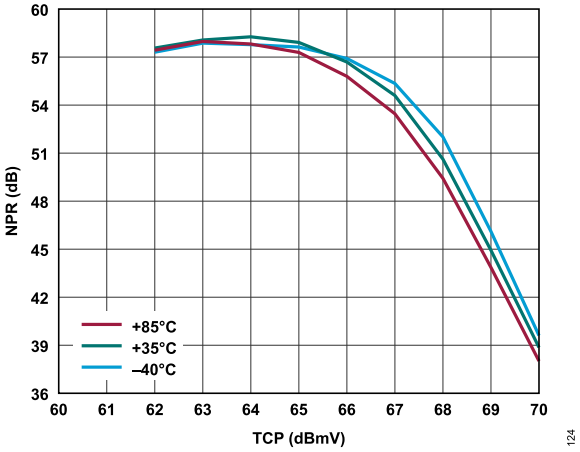

Figure 24. NPR vs. TCP Over Temperature, Worst Case Frequency, 0 dB Tilt, V_{DD} = 8.0 V

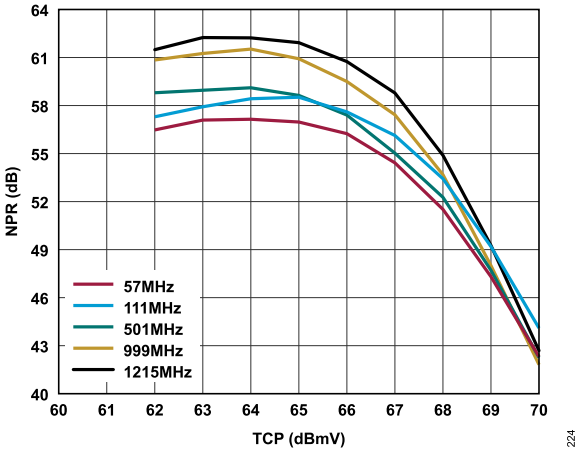

Figure 25. NPR vs. TCP Over Frequency, 10 dB Tilt, V_{DD} = 8.0 V

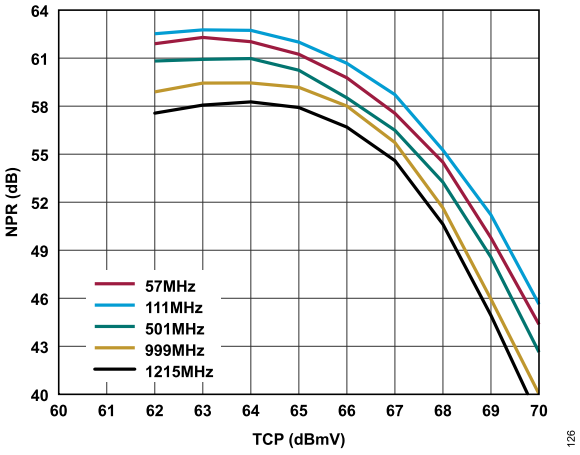

Figure 26. NPR vs. TCP Over Frequency, 0 dB Tilt, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

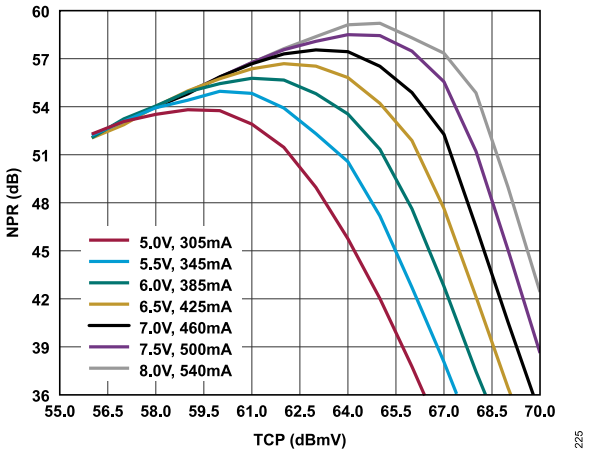

Figure 27. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 16 Ω

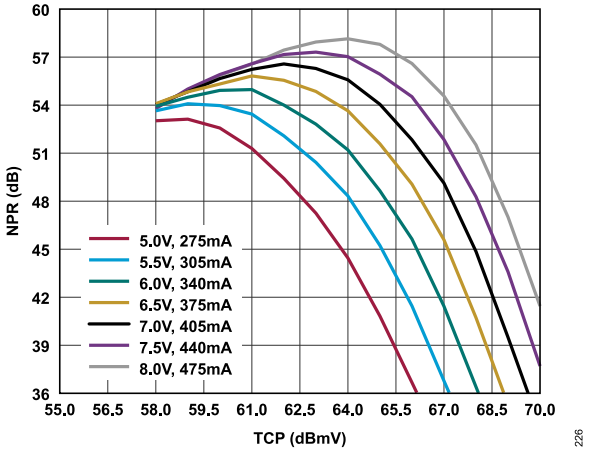

Figure 28. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 33 Ω

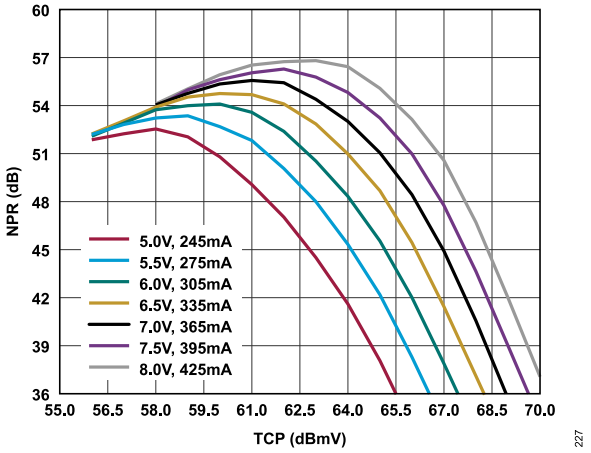

Figure 29. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 50 Ω

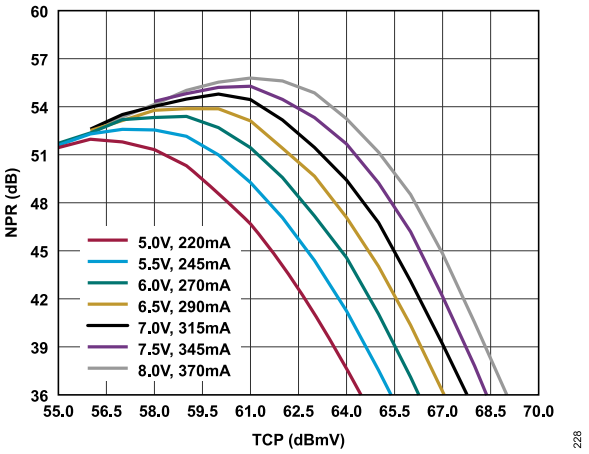

Figure 30. NPR vs. TCP Over V_{DD} and I_{DD}, Worst Case Frequency, 10 dB Tilt, R_{BIAS} = 75 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

DISTORTION AND NOISE PERFORMANCE

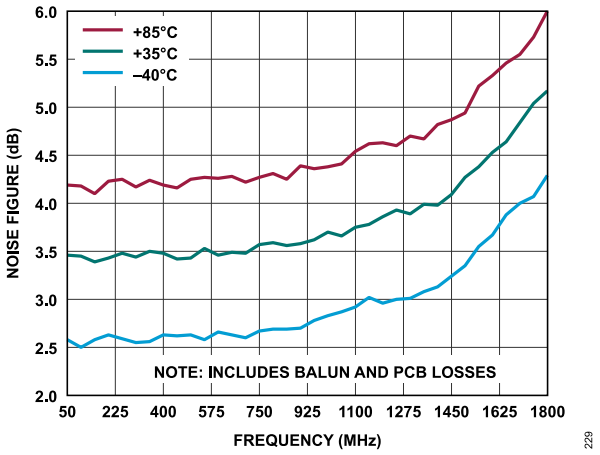

Figure 31. Noise Figure vs. Frequency Over Temperature, V_{DD} = 8 .0 V

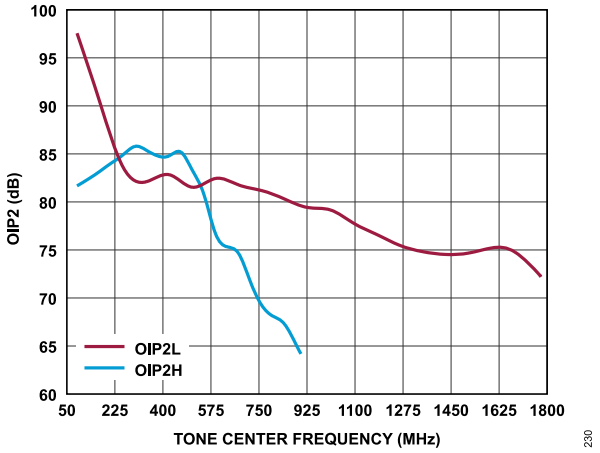

Figure 32. OIP2 vs. Tone Center Frequency, Tone Spacing 50 MHz, V_{DD} = 8 .0 V

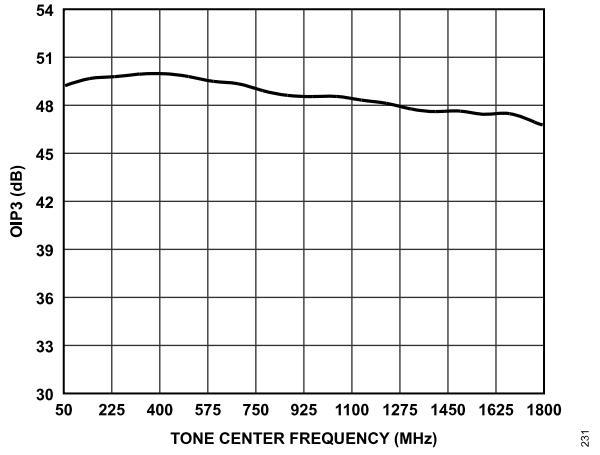

Figure 33. OIP3 vs. Tone Center Frequency, Tone Spacing 6 MHz, V_{DD} = 8 .0 V

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS UPSTREAM PERFORMANCE (SEE FIGURE 40)

105×, ITU-T J.83B, SCQAM 6 MHz Channels, and 54 MHz to 684 MHz, unless otherwise noted. In Figure 34 to Figure 37, the performance at the lower output power is limited by the test equipment and is not indicative of the noise performance of the device.

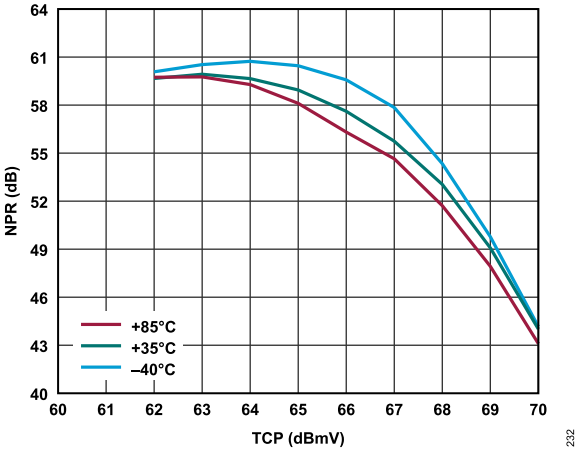

Figure 34. NPR vs. TCP Over Temperature, Worst Case Frequency, 10 dB Tilt, V_{DD} = 8.0 V

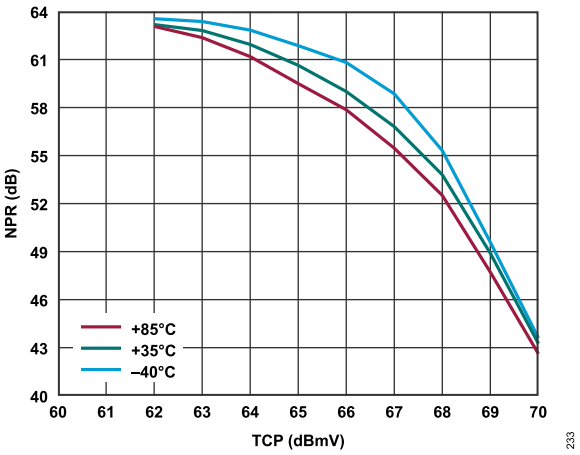

Figure 35. NPR vs. TCP Over Temperature, Worst Case Frequency, 0 dB Tilt, V_{DD} = 8.0 V

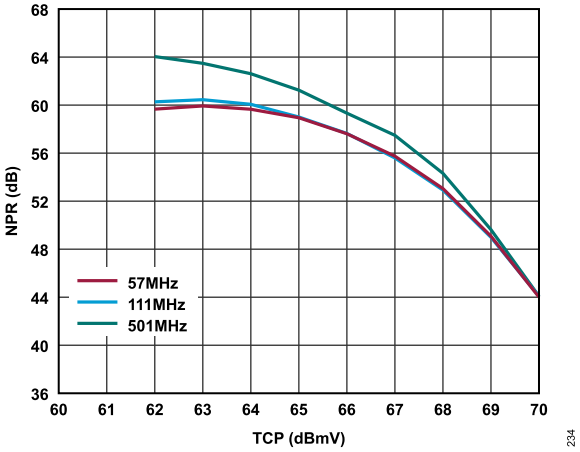

Figure 36. NPR vs. TCP Over Frequency, 10 dB Tilt, V_{DD} = 8.0 V

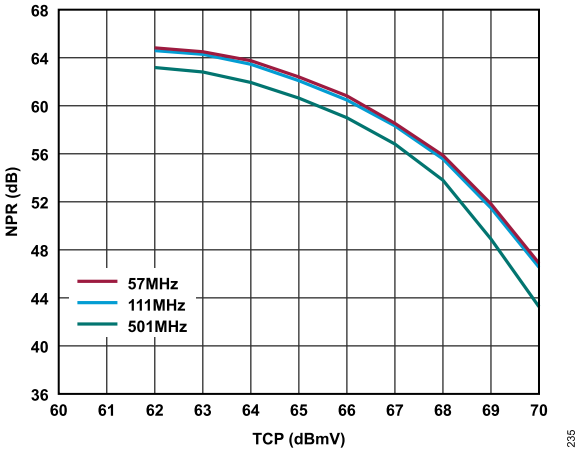

Figure 37. NPR vs. TCP Over Frequency, 0 dB Tilt, V_{DD} = 8.0 V

THEORY OF OPERATION

The ADCA5191 is a single-die, 1800 MHz differential cascode amplifier fabricated on a linear gallium arsenide (GaAs), pHEMT process. The device provides general-purpose linear gain suitable for a wide range of applications.

When used with a recommended balun, the ADCA5191 can achieve a 5.2 dB noise figure at 1800 MHz (3.8 dB noise figure at 1218 MHz) while holding excellent linearity for extended spectrum line extender input stage applications.

The device has suitable drive capability to overcome nominal insertion losses introduced from automatic gain control and tilt functions.

The ADCA5191 can also serve as an output stage for the upstream path at any DOCSIS 4.0 frequency split.

Depending on the application, the ADCA5191 can be biased from 5.0 V through 8.0 V with currents from 250 mA to 530 mA. Optimized biasing for 5.0 V applications can be achieved with additional bill of material (BOM) changes.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

The ADCA5191 is packaged in a thermally efficient, 32-lead LFCSP. The thermal resistance from junction to case, θ_{JC}, is 8.5°C/W, where the case is defined by the exposed pad on the bottom of the package. For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP and to fill these vias with a paste that has high thermal conductivity. It is also recommended that the array of vias under the ADCA5191 interface to an external heat sink such as a pedestal on the system chassis.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 38 shows the recommended land pattern for the ADCA5191. To minimize thermal impedance, the exposed pad on the 5 mm × 5 mm LFCSP is soldered to a ground plane. To improve thermal dissipation, 45 thermal vias are arranged in an array under the exposed pad. The array consists of alternating rows of six vias and seven vias, maximizing the number of vias within the area. The area under the pad is also tied to ground on the bottom layer of the PCB. If multiple ground layers exist, tie these layers together by the vias. The external layer of the PCB must be a minimum of 1 oz. copper. The minimum average plated hole wall thickness of the vias must not be less than 0.001 inches, and it is recommended that the vias be filled with a conductive paste, such as Tatsuta AE3030, and plated over.

For further information on optimizing the thermal performance while using the ADCA5191, refer to the AN-1604 Application Note, Thermal Management Calculations for RF Amplifiers in LFCSP and Flange Packages.

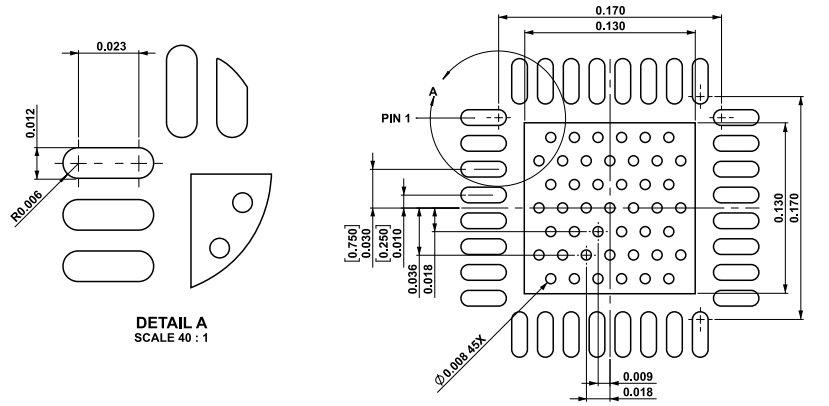

Figure 38. Recommended PCB Layout (Dimensions Shown in Inches)

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATIONS CIRCUIT

The schematic in Figure 39 is recommended for downstream cable system applications from 45 MHz to 1800 MHz. Recommended values for all components are in the BOM listed in Table 10. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5191 (RFIN and RFIP). The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. This voltage is connected through a series of components (R6, R4, and E1) and supplies the dc reference on the RF input side of T1. C6 stabilizes this reference and serves as the ac ground for the RF input signal.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C2, C3, C5, C7, C8, C13, C14, C21, L8, L9, L10, and L11 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. Capacitor C4 blocks the dc voltage of the RF input source. Capacitor C27 and Capacitor C28 are for blocking the dc voltage at the RFOP (Pin 22 and Pin 23) and RFON (Pin 18 and Pin 19) output pins. Inductors L2 and L3 are RF chokes connected to the filtered VDD supply voltage. The passive networks connected to the BIASA and BIASB pins (Pin 11 and Pin 30) are also part of the supply and biasing required for the ADCA5191 and are discussed in detail in the Supply Voltage and Bias Current section.

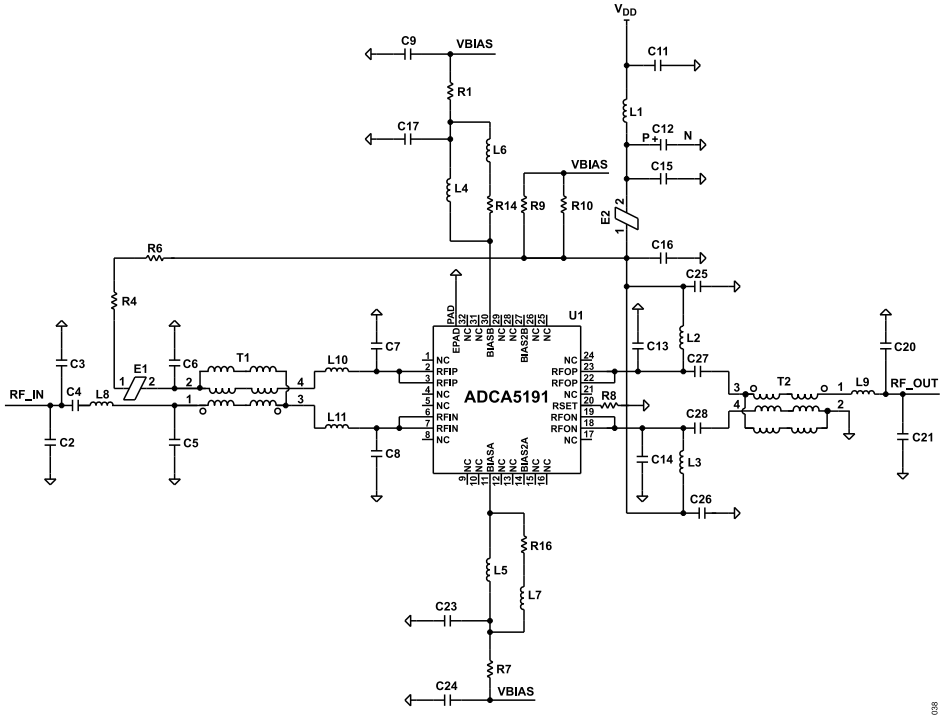

Figure 39. Suggested Downstream Cable TV (CATV) Application Circuit

APPLICATIONS INFORMATION

DOWNSTREAM CABLE APPLICATION CIRCUIT BILL OF MATERIALS

Table 10. Downstream Bill of Materials

Reference Designator	Value	Tolerance[1]	Min Rating[1]	Footprint	Suggested Vendor[1]	Suggested Part Number
C3	0.4 pF	±0.1 pF	50 V	0402	Murata	GRM1555C2AR40BA1D
C5	0.6 pF	±0.1 pF	100 V	0201	Murata	GRM0335C2AR60BA01D
C6	0.01 µF	10%	50 V	0201	Taiyo Yuden	UMK063BJ103KP-F
C7, C8	0.5 pF	±0.1 pF	100 V	0402	Murata	GRM1555C2AR50BA01D
C11	0.01 µF	20%	100 V	0603	TDK	C1608X7R2A103M080AA
C12	2.2 µF	10%	50 V	1210	Kyocera AVX	TAJB225K050RNJ
C13, C14	0.6 pF	±0.1 pF	100 V	0402	Murata	GRM1555C2AR60BA01D
C15	0.047 µF	10%	50 V	0603	TDK	06035C473KAT4A
C27, C28	160 pF	1%	50 V	0402	Murata	GRT1555C1H161FA02D
C4, C9, C16, C17, C23, C24, C25, C26	0.01 µF	10%	100 V	0402	TDK	810-C1005X7S2A103K
E1	1000 Ω ferrite	25%	170 mA	0201	Murata	BLM03BX102SN1D
E2	220 Ω ferrite	25%	1.8 A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	20%	1.6 A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	270 nH	5%	590 mA	0402	Coilcraft	0402DF-271XJRW
L4, L5	470 nH	5%	610 mA	0603	Coilcraft	0603AF-471XJEW
L6, L7	10 nH	3%	250 mA	0201	Murata	LQP03TN10NH02D
L8	5.6 nH	0.2 nH	800 mA	0402	Murata	LQW15AN5N6C10D
L9, L10, L11	0 Ω	N/A	0.1 W	0402	Panasonic	ERJ-2GE0R00X
R1, R7	10 Ω	1%	0.1 W	0402	Panasonic	ERJ-2RKF10R0X
R4, R6	365 Ω	1%	62.5 mW	0402	Yageo	RC0402FR-07365RL
R8	2 kΩ	1%	50 mW	0201	Panasonic	ERJ-1GNF2001C
R9, R10	33 Ω	1%	200 mW	0402	Vishay	CRCW040233R0FKEDHP
R14, R16	120 Ω	1%	50 mW	0201	Panasonic	ERJ-1GNF1200C
T1, T2	1:1 transformer	N/A	N/A	99-01-1618-2	Mini-Circuits	TRS1-182-75-3+
U1	CATV amplifier	N/A	N/A	5 mm × 5 mm, 32-lead LFSCP	Analog Devices, Inc.	ADCA5191
C2, C20, C21	Do not install	N/A	N/A	0402	N/A	Do not install

[1] N/A means not applicable.

APPLICATIONS INFORMATION

UPSTREAM APPLICATION CIRCUIT

The schematic in Figure 40 is recommended for upstream cable system applications from 5 MHz to 700 MHz. Recommended values for all components are in the BOM listed in Table 11. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5191 (RFIN and RFIP). The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. This voltage is connected through a series of components (R6, R4, and E1) and supplies the dc reference at Pin 4 of T1. C6 stabilizes this reference and serves as the ac ground for the RF input signal.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFIN and RFIP) to a single-ended 75 Ω RF output.

The C2, C3, C5, C7, C8, C13, C14, C20, C21, L8, L9, L10, and L11 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. Capacitor C4 blocks the dc voltage of the RF input source. Capacitor C33 is for blocking the dc voltage from T2 to RF_OUT. The V_{DD} supply is connected through T2. The passive networks connected to the BIASA and BIAS2A and the BIASB and BIAS2B pins (Pin 11, Pin 14, Pin 27, and Pin 30) are also part of the supply and biasing required for the ADCA5191 and are discussed in additional detail in the Supply Voltage and Bias Current section.

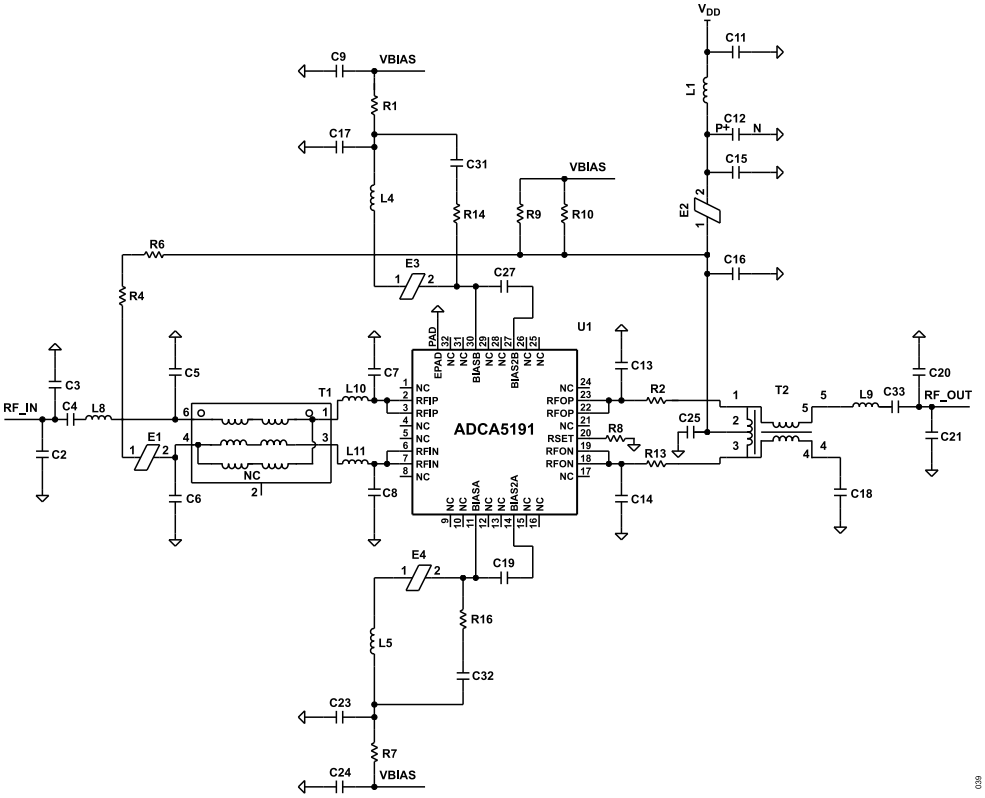

Figure 40. Suggested Upstream CATV Application Circuit

APPLICATIONS INFORMATION

UPSTREAM CABLE APPLICATIONS CIRCUIT BILL OF MATERIALS

Table 11. Upstream Bill of Materials

Reference Designator	Value	Tolerance[1]	Min Rating[1]	Footprint	Suggested Vendor[1]	Suggested Part Number[1]
C4, C6, C16, C18, C25, C33	1 µF	10%	50 V	0402	Murata	GRM155R61H105KE05D
C7, C8	2 pF	0.1 pF	50 V	0201	Murata	GRM0335C1H2R0BA01D
C9, C24	0.01 µF	10%	100 V	0402	TDK	C1005X7S2A103K050BB
C11	0.01 µF	20%	100 V	0603	TDK	C1608X7R2A103M080AA
C12	2.2 µF	10%	50 V	1210	Kyocera AVX	TAJB225K050RNJ
C15	1 µF	10%	50 V	0603	Murata	GRT188R61H105KE13D
C19, C27	1000 pF	1%	50 V	0402	Murata	GCM155R71H102KA37D
E1	1000 Ω ferrite	25%	170 mA	0201	Murata	BLM03BX102SN1D
E2	220 Ω ferrite	25%	1.8 A	0603	Taiyo Yuden	FBMH1608HM221-T
E3, E4	1500 Ω ferrite	40%	230 mA	0402	TDK	MMZ1005A152ET000
L1	2.2 µH	20%	1.6A	1210	Taiyo Yuden	BRL3225T2R2M
L8	5 Ω	1%	62.5 mW	0402	Vishay	CRCW04024R99FNED
L4, L5	4.7 µH	20%	80 mA	0603	Murata	LQM18FN4R7M00D
L9	3.3 nH	0.2 nH	900 mA	0402	Murata	LQW15AN3N3C10D
R1, R7	10 Ω	1%	100 mW	0402	Panasonic	ERJ-2RKF10R0X
R6	1470 Ω	1%	62.5 mW	0402	Yageo	RC0402FR-071K47L
R8	1470 Ω	1%	50 mW	0201	Panasonic	ERJ-1GNF1471C
R9, R10	33 Ω	1%	200 mW	0402	Vishay	CRCW040233R0FKEDHP
R14, R16	150 Ω	1%	62.5 mW	0402	Yageo	RC0402FR-07150RL
T1	1:1 transformer	N/A	N/A	AT224-3	Mini-Circuits	TC1-33-75G2+
T2	1:1 transformer	N/A	N/A	S20	MiniRF	MRFXF5R17
U1	CATV amplifier	N/A	N/A	5 mm × 5 mm, 32-lead LFSCP	Analog Devices	ADCA5191
C31, C32, L10, L11, R2, R4, R13	0 Ω	N/A	N/A	0402	Panasonic	ERJ-2GE0R00X
C2, C3, C13, C14, C17, C20, C21, C23	Do not install	N/A	N/A	0402	N/A	N/A
C5	Do not install	N/A	N/A	0201	N/A	N/A

[1] N/A means not applicable.

APPLICATIONS INFORMATION

SUPPLY VOLTAGE AND BIAS CURRENT

The ADCA5191 employs a versatile circuit design, allowing system designers to configure the supply voltage at the RFON connection (Pin 18 and Pin 19) and the RFOP connection (Pin 22 and Pin 23), as well as the overall bias current of the device through the BIASA and BIASB pins (Pin 11 and Pin 30).

Connect the BIASA and BIASB pins as shown in Figure 41. Keep the network of passive components between the BIASA and BIASB pins and V_{DD} close to the device package to minimize parasitics.

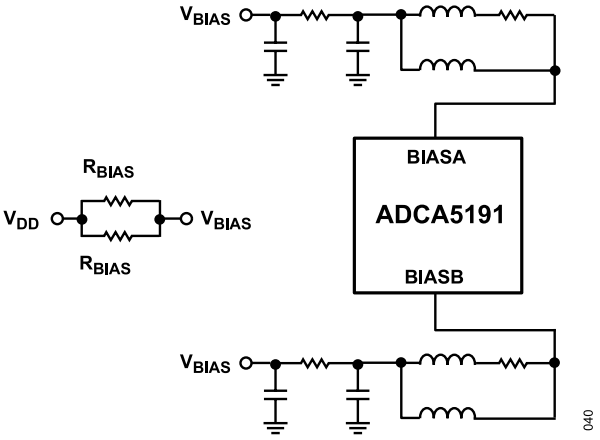

Figure 41. Suggested BIASA and BIASB Application Circuit

Figure 42 provides the typical transfer function of I_{DD} to R_{BIAS}, which allows the user to adjust I_{DD} from 250 mA to 530 mA.

See the Typical Performance Characteristics for performance under different bias conditions.

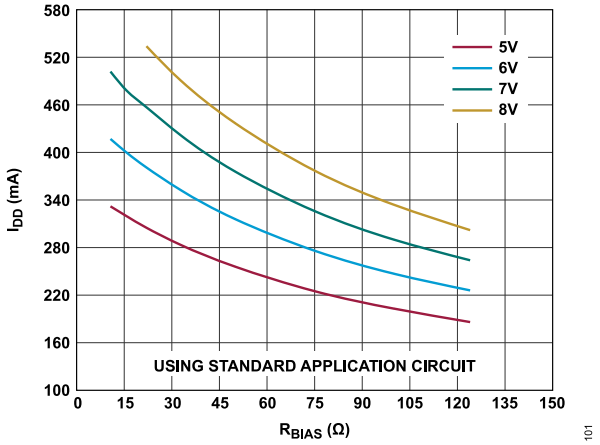

Figure 42. I_{DD} vs. R_{BIAS} over V_{DD}

OUTLINE DIMENSIONS

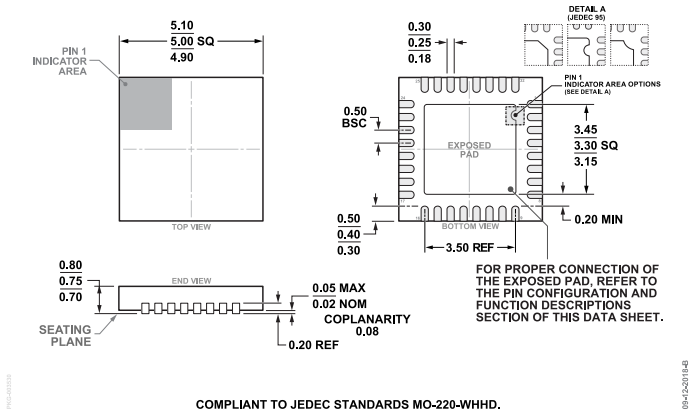

Figure 43. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-13)
Dimensions shown in millimeters

Updated: August 24, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADCA5191ACPZ	-40°C to +100°C	32-Lead LFCSP (5mm x 5mm x 0.75mm w/ EP)		CP-32-13
ADCA5191ACPZ-R7	-40°C to +100°C	32-Lead LFCSP (5mm x 5mm x 0.75mm w/ EP)	Reel, 1500	CP-32-13

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADCA5191-EVALZ	Evaluation Board for the Downstream Cable System Application

[1] Z = RoHS Compliant Part.