Digitally Programmable Dual Full-Bridge MOSFET Driver

FEATURES AND BENEFITS

- Serial interface for full digital control
- Dual full-bridge gate drive for N-channel MOSFETs
- Dual 6-bit DAC current reference
- Operation over 12 to 50 V supply voltage range
- Synchronous rectification
- Cross-conduction protection
- Adjustable mixed decay
- Fixed off-time PWM current control
- Low-current idle mode

PACKAGE: 38-pin TSSOP (suffix LD)

Not to scale

DESCRIPTION

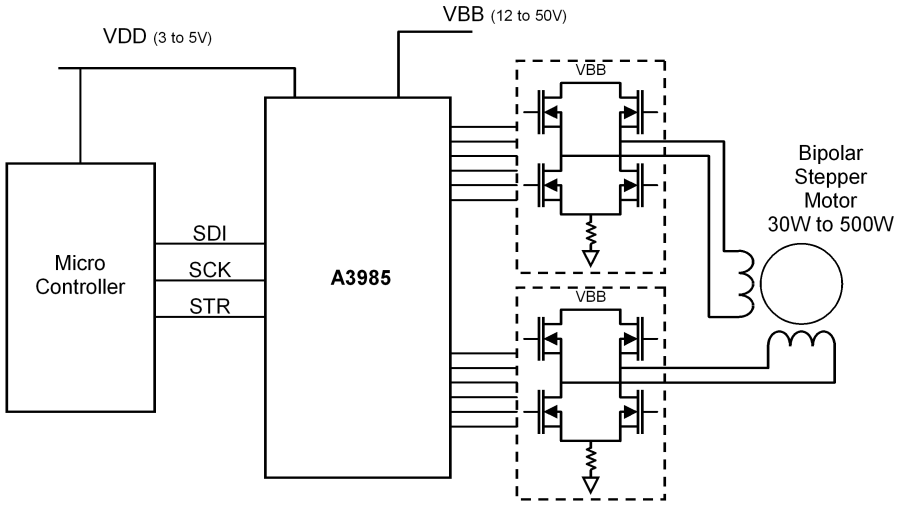
The A3985 is a flexible dual full-bridge gate driver suitable for driving a wide range of higher power industrial bipolar 2-phase stepper motors or 2-phase brushless dc motors. It can also be used to drive two individual torque motors or solenoid actuators. Motor power is provided by external N-channel power MOSFETs at supply voltages from 12 to 50 V.

Full digital control is provided by two serially accessible registers that allow programming of off-time, blank-time, dead-time, mixed decay ratios, synchronous rectification, master clock source selection, and division ratio and idle mode. All internal timings are derived from a master clock that can be generated on-chip or provided by an external clock such as the system clock of the master controller. A programmable divider allows for a wide range of external system clock frequencies.

The internal fixed off-time PWM current-control timing is programmed via the serial interface to operate in slow, fast, and mixed current-decay modes. The desired load-current level and direction is set via the serial port with a direction bit and two 6-bit linear DACs in conjunction with a reference voltage. The seven bits of control allow maximum flexibility in torque control for a variety of step methods, from microstepping to

Continued on the next page…

Typical Application



DESCRIPTION (continued)

full-step drive. Load current in the external power MOSFET full bridges is set in 1.56% increments of the maximum value.

The above-supply voltage required for the high-side N-channel MOSFETs is provided by a bootstrap capacitor. Efficiency is enhanced by using synchronous rectification and the power FETs are protected from shoot-through by integrated crossover-control and programmable dead time.

In addition to crossover current control, internal circuit protection provides thermal shutdown with hysteresis and undervoltage lockout. Special power-up sequencing is not required. This component is supplied in a 38-pin TSSOP (package LD) with 100% matte tin leadframe plating.

SELECTION GUIDE

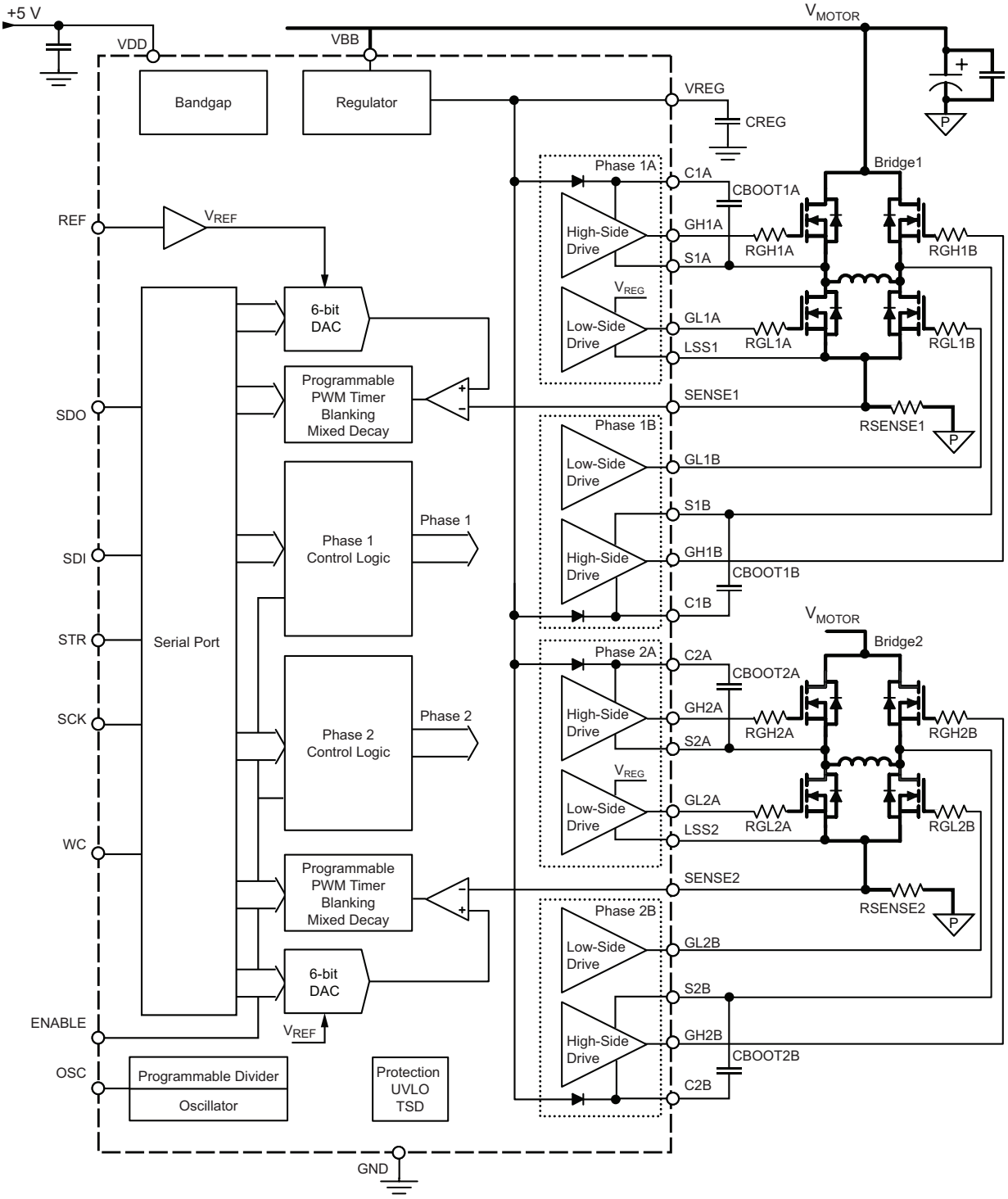
Part Number	Packing
A3985SLDTR-T	Tape and reel, 4000 pieces per reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 7	V
Logic Inputs and Outputs			–0.3 to 7	V
SENSE*x* pins			–1 to 1	V
S*xx* pins			–2 to 55	V
LSS*x* pins			–2 to 5	V
GH*xx* pins			S*xx* to S*xx*+15	V
GL*xx* pins			–2 to 16 V	V
C*xx* pins			–0.3 to S*xx*+15	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL BLOCK DIAGRAM



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 12 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY AND REFERENCE						
Load Supply Voltage Range	V_{BB}		12	–	50	V
Load Supply Current	I_{BB}	f_{MCK} = 4 MHz, C_{LOAD} = 1000 pF	–	–	10	mA
		ENABLE = High, outputs disabled	–	–	6	mA
Load Supply Idle Current	I_{BBQ}	Word1:Bit D18 = 0	–	–	100	µA
Logic Supply Voltage Range	V_{DD}		3.0	–	5.5	V
Logic Supply Current	I_{DD}		–	–	10	mA
Logic Supply Idle Current	I_{DDQ}	Word1:Bit D18 = 0	–	–	300	µA
Regulator Output	V_{REG}	I_{REGInt} = 30 mA	11.25	–	13	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_{fBOOT} = 10 mA	0.6	0.8	1	V
GATE OUTPUT DRIVE						
Turn-On Rise Time	t_r	C_{LOAD} = 1000 pF, 20% to 80%	80	120	160	ns
Turn-Off Fall Time	t_f	C_{LOAD} = 1000 pF, 80% to 20%	40	60	80	ns
Turn-On Propagation Delay	$t_{p(on)}$	ENABLE low to gate drive on	–	120	–	ns
Turn-Off Propagation Delay	$t_{p(off)}$	ENABLE high to gate drive off	–	120	–	ns
Crossover Dead Time	t_{DEAD}	f_{MCK} = 4 MHz, Word1:Bits D1 and D2 = 00	0.5	–	0.75	µs
Pull-Up On Resistance	$R_{DS(on)UP}$	I_{GH} = –25 mA	30	40	55	Ω
Pull-Down On Resistance	$R_{DS(on)DN}$	I_{GL} = 25 mA	14	19	24	Ω
Short-Circuit Current – Source [1]	$I_{SC(source)}$		–140	–110	–80	mA
Short-Circuit Current – Sink	$I_{SC(sink)}$		160	200	250	mA
GH*x* Output Voltage	V_{GHx}	CBOOT*x* fully charged	V_C – 0.2	–	–	V
GL*x* Output Voltage	V_{GLx}		V_{REG} – 0.2	–	–	V
LOGIC INPUTS						
Input Low Voltage	V_{IL}		–	–	0.3 V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}	–	–	V
Input Hysteresis	V_{IHys}		150	300	–	mV
Input Current[1]	I_{IN}		–1	–	1	µA
Output Low Voltage	V_{OL}	SDO, I_{OL} = 0.5 mA			0.5	V
Output High Voltage	V_{OH}	SDO, I_{OH} = –0.3 mA	V_{DD} – 0.5			V
Output Leakage Current [1]	I_{Oleak}	SDO, STR = 1, 0 V< V_O< V_{DD}	–1		1	µA

Continued on the next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 12 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
CURRENT CONTROL						
Blank Time	t_{BLANK}	f_{MCK} = 4 MHz; Word1:Bits D1 and D2 = 00	–	1	–	µs
Fixed Off-Time	t_{OFF}	f_{MCK} = 4 MHz, Word1:Bits D3 to D7 = 01010, and D15 = 0	21.75	–	22	µs
Reference Input Voltage	V_{REF}		0.8	–	2	V
Internal Reference Voltage	V_{REFInt}	20 kΩ to V_{DD}	1.9	2.0	2.1	V
Current Trip Point Error [2]	E_{ITrip}	V_{REF} = 2 V	–	–	±5	%
Reference Input Current [1]	I_{REF}		–3	0	3	µA
Internal Oscillator Frequency	f_{OSC}	R_{OSC} = 10 kΩ	3.2	4	4.8	MHz
Maximum Clock Input Frequency	f_{EXTmax}	External clock selected	–	10	–	MHz
Master Clock Frequency	f_{MCK}		0.5	4	5	MHz
PROTECTION						
VREG Undervoltage Lockout	V_{REGUV}	Decreasing V_{REG}	7.5	8	8.5	V
VREG Undervoltage Lockout Hysteresis	$V_{REGUVHys}$		100	200	–	mV
VDD Undervoltage Lockout	V_{DDUV}	Decreasing V_{DD}	2.45	2.7	2.95	V
VDD Undervoltage Lockout Hysteresis	$V_{DDUVHys}$		50	100	–	mV
Overtemperature Shut Down	T_{TSD}	Temperature increasing	–	165	–	°C
Overtemperature Shut Down Hysteresis	T_{TSDHys}	Recovery = T_{TSD} – T_{TSDHys}	–	15	–	°C

Continued on the next page...

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB, based on JEDEC standard	51	°C/W
		1-layer PCB with copper limited to solder pads	127	°C/W

*Additional thermal information available on Allegro Web site.

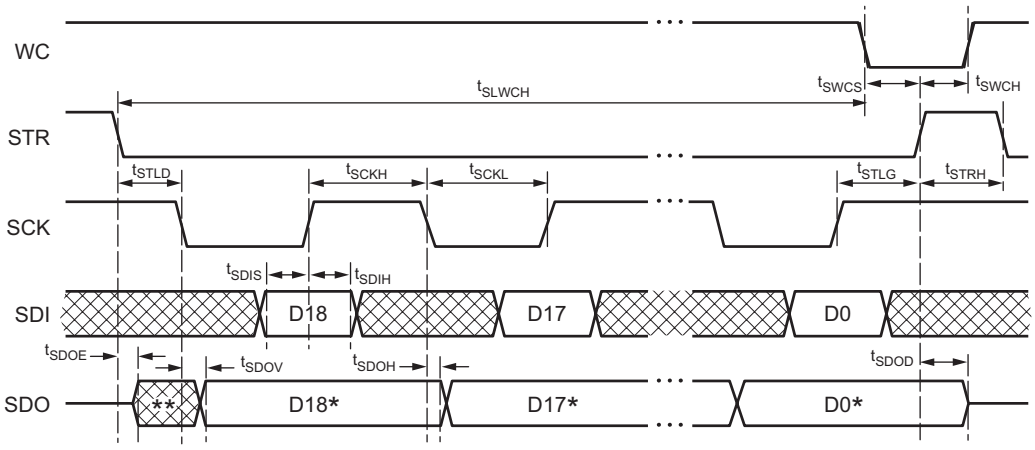
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 12 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SERIAL DATA TIMING						
Serial Clock High Time	t_{SCKH}		50	—	—	ns
Serial Clock Low Time	t_{SCKL}		50	—	—	ns
Strobe Lead Time	t_{STLD}		30	—	—	ns
Strobe Lag Time	t_{STLG}		30	—	—	ns
Strobe High Time	t_{STRH}		150	—	—	ns
Data Out Enable Time	t_{SDOE}		—	—	40	ns
Data Out Disable Time	t_{SDOD}		—	—	30	ns
Data Out Valid Time from SCK Falling	t_{SDOV}		—	—	40	ns
Data Out Hold Time from SCK Falling	t_{SDOH}		5	—	—	ns
Data In Set-up Time to SCK Rising	t_{SDIS}		15	—	—	ns
Data In Hold Time from SCK Rising	t_{SDIH}		10	—	—	ns
WC Set-up Time to STR Rising	t_{SWCS}		15	—	—	ns
WC Hold Time from STR Rising	t_{SWCH}		50	—	—	ns
WC Hold Time from STR Falling	t_{SLWCH}		30	—	—	ns

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] Current Trip Point Error is the difference between actual current trip point and the target current trip point, referred to full scale (100%) current: $E_{ITrip} = 100 \times (I_{TripActual} - I_{TripTarget}) / I_{FullScale}$ %

Serial Data Timing Diagram



Dx = Current data transfer block
Dx* = Previous data transfer block
** = Undefined, usually LSB from previous transfer

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Basic Operation

The A3985 is a highly configurable dual full-bridge FET driver with built-in digital current control. All features are accessed through a simple SPI (Serial Peripheral Interface) compatible serial port, allowing multiple motors to be controlled with as few as three wires.

Because the full-bridge control circuits are independently controlled, the A3985 can be used to drive 2-phase bipolar stepper motors and 2-phase brushless dc (BLDC) motors. The current in each of the two external power full-bridges (which are all N-channel MOSFETs) is regulated by a fixed off-time PWM control circuit. The full-bridge current at each step is set by the value of an external current sense resistor, R_{SENSEx}, in the ground connection to the bridge, a reference voltage, V_{REF}, and the output of the DAC controlled by the serial data.

The use of PWM with N-channel MOSFETs provides the most cost-effective solution for a high efficiency motor drive. The A3985 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are above 10 V, and that there is no cross-conduction (shoot through) in the external bridge. Specific functions are described more fully in the following sections.

Power Supplies

Two power connections are required. The motor power supply should be connected to VBB to provide the gate drive levels. Power for internal logic is provided by the VDD input. Internal logic is designed to operate from 3 to 5.5 V, allowing the use of 3.3 or 5 V external logic interface circuits.

GND The ground pin is a reference voltage for internal logic and analog circuits. There is no large current flow through this pin. To avoid any noise from switching circuits, this should have an independent trace to the supply ground star point.

VREG The voltage at this pin is generated by a low-drop-out linear regulator from the VBB supply. It is used to operate the low-side gate drive outputs, GL*xx*, and to provide the charging current for the bootstrap capacitors, CBOOT*x*. To limit the voltage drop when the charge current is provided, this pin should be decoupled with a ceramic capacitor, CREG, to ground. The value C_{REG} should typically be 40 times the value of the bootstrap capacitor for PWM frequencies up to 14 kHz. Above 14 kHz, the minimum recommended value can be determined from the following formula:

$$C_{REG} > C_{BOOT} \times 3 \times f_{PWM} ,$$

where C_{REG} and C_{BOOT} are in nF, and f_{PWM} is the maximum PWM frequency, in kHz. V_{REG} is monitored, and if the voltage becomes too low, the outputs will be disabled.

REF The reference voltage, V_{REF}, at this pin sets the maximum (100%) peak current. The REF input is internally limited to 2 V when a 20 kΩ pull-up resistor is connected between VREF and VDD. This allows the maximum reference voltage to be set without the need for an externally-generated voltage. An external reference voltage below the maximum can also be input on this pin. The voltage at VREF is divided by the range select ratio G_m to produce the DAC reference voltage level.

OSC The PWM timing is based on a master clock, typically running at 4 MHz. The master clock period is used to derive the PWM off-time, dead time, and blanking time.

The master clock frequency can be set by an internal oscillator or by one of three division ratios of an external clock. These four options are selected by bits D12 and D13 of the Control register word.

When the A3985 is configured to use an external clock, this is input on the OSC pin and will usually provide more precision than using the internal oscillator. The three internal divider alternatives provide flexibility in setting the master clock frequency based on available external system clocks. If internal timing is selected, f_{OSC} is configured by using an external resistor, ROSC, connected from the OSC pin to GND. This sets the frequency (in MHz) to approximately:

$$f_{OSC} \approx 100 / (6 + 1.9 \times R_{OSC}) ,$$

where R_{OSC}, in kΩ, is typically between 50 kΩ and 10 kΩ.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SDI, SCK, STR, SDO These are the serial port interface pins. Data is clocked into SDI by a clock signal on SCK. The data is then latched by a signal on STR. Note, however, that SCK must be high for one setup time interval, t_{STLG}, before STR goes high and SCK must remain high for one hold time interval, t_{STRH}, after STR has gone high (see Serial Data Timing Diagram). If required, the serial data out pin, SDO, can be used to read back the previously latched serial data or to form a daisy chain for multiple controllers using a single STR connection. (For bit assignment details, see the Bit Assignments table.)

WC This input provides a lockout capability for writing to the Control register. When set to logic high, no changes can be made to the Control register through the serial port. When at logic low, the data on the serial port will update the Control register (if selected by D0 = 1) while STR is high. This provides a mechanism to avoid inadvertently changing the Control register settings by erroneous or corrupt serial data signals.

Gate Drive

The A3985 is designed to drive external power N-channel MOSFETs. It supplies the transient currents necessary to quickly charge and discharge the external FET gate capacitance in order to reduce dissipation in the external FET during switching. The charge and discharge rate can be controlled using an external resistor, RGx, in series with the connection to the gate of the FET. Cross-conduction is prevented by the gate drive circuits which introduce a dead time, t_{DEAD}, between switching one FET off and the complementary FET on. t_{DEAD} is at least 2, 3, 4, or 6 periods of the master clock, depending on the corresponding value set in the Control register (Word 1: bits D1 and D2). t_{DEAD} can be up to 1 cycle longer than the programmed value, to allow synchronization with the master clock.

ENABLE This input simply turns off all of the power MOSFETs. Set to logic high to disable outputs. When at logic low, the internal control enables the outputs as required. Inputs to the registers and the internal sequencing logic are all active independent of the ENABLE input state.

C1A, C1B, C2A, and C2B High-side connections for the bootstrap capacitors, CBOOT*x*, and positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately V_{REG} when the associated output S*xx* terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs. The bootstrap capacitor should be ceramic and have a value of 10 to 20 times the total MOSFET gate capacitance.

GH1A, GH1B, GH2A, and GH2B High-side gate drive outputs for external N-channel MOSFETs. External series gate resistors can be used to control the slew rate seen at the gate, thereby controlling the *di*/*dt* and *dv*/*dt* at the motor terminals. GH*xx* = 1 (high) means that the upper half of the driver is turned on and will source current to the gate of the high-side MOSFET in the external motor-driving bridge. GH*xx* = 0 (low) means that the lower half of the driver is turned on and will sink current from the external MOSFET gate circuit to the respective S*xx* pin.

S1A, S1B, S2A, and S2B Directly connected to the motor, these terminals sense the voltages switched across the load and define the negative supply for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low impedance traces to the MOSFET bridge.

GL1A, GL1B, GL2A, and GL2B Low-side gate drive outputs for external N-channel MOSFETs. External series gate resistors (as close as possible to the MOSFET gate) can be used to reduce the slew rate seen at the gate, thereby controlling the *di*/*dt* and *dv*/*dt* at the motor terminals. GL*xx* = 1 (high) means that the upper half of the driver is turned on and will source current to the gate of the low-side MOSFET in the external motor-driving bridge. GL*xx* = 0 (low) means that the lower half of the driver is turned on and will sink current from the gate of the external MOSFET to the LSS*x* pin.

LSS1 and LSS2 Low-side return path for discharge of the gate capacitors, connected to the common sources of the low-side external FETs through low-impedance traces.

Internal PWM Current Control

Each full-bridge is independently controlled by a fixed off-time PWM current control circuit that limits the load current in the phase to a desired value, I_{Trip}. Initially, a diagonal pair of source and sink MOSFETs are enabled and current flows through the motor winding and the current sense resistor, RSENSE*x*. When the voltage across RSENSE*x* equals the

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DAC output voltage, the current sense comparator resets the PWM latch, which turns off the source MOSFET (slow decay mode) or the sink and source MOSFETs (fast decay mode). The maximum value of current limiting is set by the selection of R_{SENSE} and the voltage at the REF input, with a transconductance function approximated by:

$$I_{Trip(max)} = V_{REF}/(G_m \times R_{SENSE}) ,$$

where G_m is the range factor defined by in the Data register (Word0: Bits D17 and D18).

The DAC output reduces the VREF output to the current sense comparator, V_{DAC}, in precise steps:

$$V_{DAC} = [(1 + DAC) \times V_{REF}] / 64 ,$$

where DAC is the decimal equivalent value of the Bridge DAC bits in the Data register (Word0: Bits D1 through D6 for Bridge 1, Bits 9 through 14 for Bridge 2). (Active codes are represented by the values 1 through 63. Programming a DAC input code to 0 disables the corresponding bridge, and results in minimum load current.)

The current trip level for each DAC value then becomes:

$$I_{TripDAC} = V_{DAC}/(G_m \times R_{SENSE}) .$$

PWM Timer Function All bridge control timing is based on the master clock. The PWM timer is programmed via the serial port to provide fixed off-time PWM signals to the control block. The off-time, t_{OFF}, is selected by programming the Off-Time bits in the Control register (Word1, Bits D3 through D7) using the serial port. t_{OFF} may be up to 1 cycle longer than the programmed value, to synchronize with the master clock.

Blanking When a source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent false overcurrent detection due to this current spike, the output from the current sense comparator is ignored (blanked) for a duration of time called the blank time. The blank timer runs, when a source power MOSFET is turned on, to provide the programmable blanking function The blank timer is reset when PHASE is changed.

The blank time can be set to 4, 6, 8, or 12 periods of the master clock by programming the blank time bits in the Control register (Word1, Bits D1 and D2) using the serial port.

Dead Time To prevent cross-conduction (shoot through) in the power full-bridge, a dead time, t_{DEAD}, is introduced between switching one MOSFET off and switching the complementary MOSFET on. The dead time, t_{DEAD}, is nominally half of t_{BLANK}, but may be up to 1 cycle longer to synchronize with the master clock.

Mixed Decay Operation

Mixed decay is a technique that provides greater control of phase currents while the current is decreasing. When a stepper motor is driven at high speed, the back EMF from the motor will lag behind the driving current. If a passive current decay mode, such as slow decay, is used in the current control scheme, then the motor back EMF can cause the phase current to rise out of control. Mixed decay eliminates this effect by putting the full-bridge initially into fast decay, and then switching to slow decay after some time. Because fast decay is an active (driven) decay mode, this portion of the current decay cycle will ensure that the current remains in control. Using fast decay for the full current decay time (off-time, t_{OFF}) would result in a large ripple current, but switching to slow decay once the current is in control will reduce the ripple current value. The portion of the off-time that the full-bridge has to remain in fast decay will depend on the characteristics and the speed of the motor.

When the phase current is rising, the motor back EMF does not affect the current control, and slow decay may be used to minimize the phase current ripple. The A3985 must be programmed to switch between slow decay, when the current is rising, and mixed decay, when the current is falling. To simplify this programming sequence the decay mode is included in the data word (Word0) with the phase current trip level and the phase current direction.

When mixed decay is used, the portion of the off-time that the full-bridge remains in fast decay, t_{FD}, is selected by programming the Fast Decay Time bits in the Control register (Word1, Bits D8 through D11). If t_{FD} is set longer than t_{OFF}, the device effectively operates in full fast decay mode.

Selecting between slow decay and mixed decay is done by programming the Mode bits in the Data register (Word0, Bits D8 and D16) using the serial port.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Synchronous Rectification When a PWM off-cycle is triggered, load current recirculates according to the decay mode selected by the control logic. The synchronous rectification feature turns on the appropriate MOSFETs during the current decay and effectively shorts out the body diodes with the low $R_{DS(ON)}$ of the MOSFET. This lowers power dissipation significantly and eliminates the need for additional Schottky diodes.

Synchronous rectification can be set to one of three distinct modes by programming the Synchronous Rectification bits in the Control register (Word1, Bits D14 through D15) using the serial port. The modes are:

- **Active** This mode prevents reversal of the load current by turning off synchronous rectification when a zero current level is detected. This prevents the motor winding from conducting in the reverse direction.
- **Passive** This mode allows reversal of current but will turn of the synchronous rectifier circuit if the load current inversion ramps up to the current limit, $I_{TripDAC}$.
- **Disabled** During this mode, MOSFET switching does not occur during load recirculation. Usually, this setting would only be used with 4 additional external clamp diodes per bridge.

Shutdown Operation In the event of an overtemperature fault, or an undervoltage fault on VREG, the gate drive outputs are disabled until the fault condition is removed. At power-up, and in the event of low voltage at VDD, the undervoltage lockout (UVLO) circuit disables the gate drive outputs until the voltage at VDD reaches the minimum level. Once VDD is above the minimum level, the data in the serial port is reset to all 0s, ensuring a safe power-up condition.

Serial Interface

The A3985 is controlled by a 3-wire serial port using data, clock and strobe inputs on the SDI, SCK and STR pins respectively. An additional serial data output on SDO can be used to connect several A3985s in a serial daisy chain. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is written as two 19-bit words: 18 bits of data plus 1 bit to select the destination register.

Serial Port Write Timing Operation The serial port timing requirements are specified in the electrical characteristics table and illustrated in the Serial Data Timing diagram.

Data is received on the SDI pin and clocked through a shift register on the rising edge of the clock signal received on the SCK pin. STR is normally held high, and is only brought low to initiate a write cycle. No data is clocked through the shift register when STR is high.

The 18 data bits for a register are input MSB first, followed by the register select bit, D0. After D0 is clocked into the shift register, STR goes high to latch the data into the selected register. When this occurs, the internal control circuits immediately act on the new data.

The Control register can only be written if the WC pin is at logic low. If WC is high and D0 = 1 (indicating the Control register), the data will be ignored on the rising edge of STR. The state of the WC pin does not affect writing to the Data register, and the pin can be tied to GND when Control register protection is not required.

Note that the number of bits clocked through the shift register is irrelevant and only the last 19 bits before STR goes high will be latched. This allows several A3985 devices to be daisy-chained and updated together with a single STR rising edge.

Data Register (Word 0) Bit Assignments

This section describes the function of the individual bit values in the Data register, one of the two registers accessed through the serial port. The assignments are summarized in the Bit Assignments table.

D0 – Register Select Indicates which register should receive the data. For the Data register, this is set to 0.

D1 through D6 – Bridge 1 Linear DAC These six bits set the desired current level for Bridge 1. Setting all six bits

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

to 0 disables Bridge 1, with all drivers off (see Internal PWM Current Control, in the Functional Description section).

D7 – Bridge 1 Phase Controls the direction of output current for Bridge (load) 1.

D7	S1A	S1B
0	L	H
1	H	L

D8 – Bridge 1 Mode Determines whether slow decay is forced or mixed decay, according to Word 1 Bits D3 to D11, is allowed.

D8	Mode
0	Mixed-decay
1	Slow-decay

D9 – D14 Bridge 2 Linear DAC These six bits set the desired current level for Bridge 2. Setting all six bits to 0 disables Bridge 2, with all drivers off (see Internal PWM Current Control, in the Functional Description section).

D15 – Bridge 2 Phase Controls the direction of output current for Bridge (load) 2.

D15	S2A	S2B
0	L	H
1	H	L

D16 – Bridge 2 Mode Determines whether slow decay is forced or mixed decay, according to Word 1 Bits D3 to D11, is allowed.

D16	Mode
0	Mixed-decay
1	Slow-decay

D17 and D18 – G_m Range Select These bits determine the range scaling factor, G_m, used in PWM current control, according to the following formula:

$$I_{TripDAC} = V_{DAC} / (G_m \times R_{SENSEx})$$

D18	D17	G_m
0	0	8
0	1	12
1	0	16
1	1	20

Control Register (Word 1) Bit Assignments

This section describes the function of the individual bit values in the Control register, one of the two registers accessed through the serial port. The assignments are summarized in the Bit Assignments table.

Note that the Control register can only be updated when the WC pin is logic low.

D0 – Register Select Indicates which register should receive the data. For the Control register, this is set to 1.

D1 and D2 – Blank Time These two bits set the value of the scaling factor, α / f_{MCK}, used for determining t_{BLANK} for the current-sense comparator. The factor for t_{DEAD} also is set, because $t_{DEAD} = t_{BLANK} / 2$.

D2	D1	t_{BLANK}	t_{DEAD} ($t_{BLANK}/2$)
0	0	$4/f_{MCK}$	$2/f_{MCK}$
0	1	$6/f_{MCK}$	$3/f_{MCK}$
1	0	$8/f_{MCK}$	$4/f_{MCK}$
1	1	$12/f_{MCK}$	$6/f_{MCK}$

D3 through D7 – Fixed Off Time These five bits set the fixed off-time for the internal PWM control circuitry. Fixed off-time is defined by:

$$t_{OFF} = [(1 + n) \times (8/f_{MCK})] - 1/f_{MCK},$$

where $n = 0$ to 31.

For example, with a master clock frequency of 4 MHz, the fixed off-time time would be adjustable within the range 1.75 to 63.75 µs, in increments of 2 µs.

D8 through D11 – Fast Decay Time These four bits set the fast decay portion of fixed off-time for the internal PWM control circuitry. The fast-decay portion is defined by:

$$t_{FD} = [(1 + n) \times 8/f_{MCK})] - 1/f_{MCK},$$

where $n = 0$ to 15.

For example, with a master clock frequency of 4 MHz, the fast decay time would be adjustable within the range 1.75 to 32.75 µs, in increments of 2 µs.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Note that, for $t_{FD} > t_{OFF}$, the device effectively operates in full fast-decay mode.

D12 and D13 – Master Clock Control An internal oscillator can be used for the timing functions, and if more precise control is required, an external clock can be input to the OSC terminal (for configuration information, refer to the Functional Description section). To accommodate a wider range of external system clocks, an internal divider is provided to generate the desired master clock frequency, f_{MCK}, according to the following table:

D13	D12	Master Clock Source and f_{MCK}
0	0	Internal oscillator*
0	1	External clock rate
1	0	External clock rate/2
1	1	External clock rate/4

*4 MHz typical, configurable with external resistor, ROSC.

D14 and D15 – Synchronous Rectification Two bits are used to set the mode for synchronous rectification. The modes are described in the synchronous rectification section of the Functional Description section.

D15	D14	Synchronous Rectification Mode
0	0	Disabled
0	1	Disabled
1	0	Active
1	1	Passive

D16 and D17 – Reserved These bits are reserved for testing and should be programmed to 0 during normal operation.

D18 – Idle Mode The device can be placed in a low power mode by writing a 0 to D18. This disables the VREG regulator (to 0 V) and the outputs, and the device draws a lower load supply current. The undervoltage monitor circuit remains active. When leaving idle mode, D18 should be set to 1 for at least 1 ms to allow the regulator to return VREG to its normal operating voltage (≈12 V) before attempting to enable any output driver.

Bit Assignments Table

Data Register			Control Register		
Word	**Bit**	**Function**	**Word**	**Bit**	**Function**
0	D0	Register Select = 0	1	D0	Register Select = 1
	D1	Bridge 1, DAC bit 0 (LSB)		D1	Blank-time bit 0 (LSB)
	D2	Bridge 1, DAC bit 1		D2	Blank-time bit 1 (MSB)
	D3	Bridge 1, DAC bit 2		D3	Off-time bit 0 (LSB)
	D4	Bridge 1, DAC bit 3		D4	Off-time bit 1
	D5	Bridge 1, DAC bit 4		D5	Off-time bit 2
	D6	Bridge 1, DAC bit 5 (MSB)		D6	Off-time bit 3
	D7	Bridge 1, Phase		D7	Off-time bit 4 (MSB)
	D8	Bridge 1, Mode		D8	Fast-decay time bit 0 (LSB)
	D9	Bridge 2, DAC bit 0 (LSB)		D9	Fast-decay time bit 1
	D10	Bridge 2, DAC bit 1		D10	Fast-decay time bit 2
	D11	Bridge 2, DAC bit 2		D11	Fast-decay time bit 3 (MSB)
	D12	Bridge 2, DAC bit 3		D12	Master Clock Control bit 0 (LSB)
	D13	Bridge 2, DAC bit 4		D13	Master Clock Control bit 1 (MSB)
	D14	Bridge 2, DAC bit 5 (MSB)		D14	Synchronous Rectification Control bit 0 (LSB)
	D15	Bridge 2, Phase		D15	Synchronous Rectification Control bit 1 (MSB)
	D16	Bridge 2, Mode		D16	Reserved
	D17	Range Select bit 0		D17	Reserved
	D18	Range Select bit 1		D18	Idle Mode

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATIONS INFORMATION

Current Sensing

To minimize inaccuracies in sensing the I_{PEAK} current level caused by ground-trace IR drops, the sense resistor, RSENSE*x*, should have an independent return to the supply ground star point. For low-value sense resistors, the IR drops in the sense resistor PCB traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in $RENSE_{Sx}$ due to their contact resistance.

Thermal Protection

All drivers are turned off when the junction temperature reaches 165°C typical. This is intended only to protect the A3985 from failures due to excessive junction temperatures. Thermal protection will not protect the A3985 from continuous short circuits. Thermal shutdown has a hysteresis of approximately 15°C.

Circuit Layout

Since this is a switch-mode application, where rapid current changes are present, care must be taken during layout of the application PCB. The following points are provided as guidance for layout. Following all guidelines will not always be possible. However, each point should be carefully considered as part of any layout procedure.

Ground Connection Layout Recommendations:

1. Decoupling capacitors for the supply pins VBB, VREG, and VDD should be connected independently, close to the GND pin, and not to any ground plane. The decoupling capacitors should also be connected as close as possible to the corresponding supply pin.
2. If used, the oscillator timing resistor ROSC should be connected to the GND pin. It should not be connected to any ground plane, supply common, or the power ground.
3. The GND pin should be connected by an independent low-impedance trace to the supply common at a single point.
4. Check the peak voltage excursion of the transients on the LSS pin with reference to the GND pin using a close grounded (tip and barrel) probe. If the voltage at LSS exceeds the specified absolute maximum add additional clamping, capacitance, or both, between the LSS pin and the AGND pin.

Other layout recommendations:

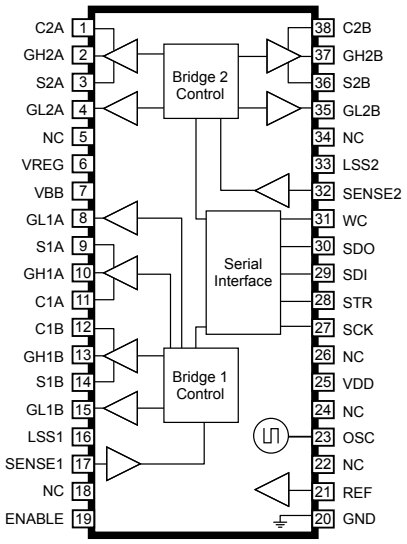
1. Gate charge drive paths and gate discharge return paths may carry transient current pulses. Therefore, the traces from GH*xx*, GL*xx*, S*xx*, and LSS*x* should be as short as possible to reduce the inductance of the circuit trace.
2. Provide an independent connection from each LSS pin to the common point of each power bridge. It is not recommended to connect LSS directly to the GND pin. The LSS connection should not be used for the SENSE connection.
3. Minimize stray inductance by using short, wide copper runs at the drain and source terminals of all power FETs. This includes motor lead connections, the input power bus, and the common source of the low-side power FETs. This will minimize voltages induced by fast switching of large load currents.
4. Consider the use of small (100nF) ceramic decoupling capacitors across the source and drain of the power FETs to limit fast transient voltage spikes caused by trace inductance.

The above are only recommendations. Each application is different and may encounter different sensitivities. Each design should be tested at the maximum current, to ensure any parasitic effects are eliminated.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST

PINOUT DIAGRAM



TERMINAL LIST TABLE

Number	Name	Description
1	C2A	Phase 2 bootstrap capacitor drive A connection
2	GH2A	Phase 2 high-side gate drive A
3	S2A	Phase 2 motor connection A
4	GL2A	Phase 2 low-side gate drive A
5	NC	No internal connection
6	VREG	Regulator decoupling capacitor connection
7	VBB	Motor supply voltage
8	GL1A	Phase 1 low-side gate drive A
9	S1A	Phase 1 motor connection A
10	GH1A	Phase 1 high-side gate drive A
11	C1A	Phase 1 bootstrap capacitor drive A connection
12	C1B	Phase 1 bootstrap capacitor drive B connection
13	GH1B	Phase 1 high-side gate drive B
14	S1B	Phase 1 motor connection B
15	GL1B	Phase 1 low-side gate drive B
16	LSS1	Phase 1 low-side source connection
17	SENSE1	Phase 1 bridge current sense input
18	NC	No internal connection
19	ENABLE	Output enable
20	GND	Ground
21	REF	Reference voltage
22	NC	No internal connection
23	OSC	External clock input, ROSC resistor connection
24	NC	No internal connection
25	VDD	Logic supply voltage
26	NC	No internal connection
27	SCK	Serial Data Clock
28	STR	Serial Data Strobe
29	SDI	Serial Data Input
30	SDO	Serial Data Output
31	WC	Write Configuration Enable
32	SENSE2	Phase 2 bridge current sense input
33	LSS2	Phase 2 low-side source connection
34	NC	No internal connection
35	GL2B	Phase 2 low-side gate drive B
36	S2B	Phase 2 motor connection B
37	GH2B	Phase 2 high-side gate drive B
38	C2B	Phase 2 bootstrap capacitor drive B connection

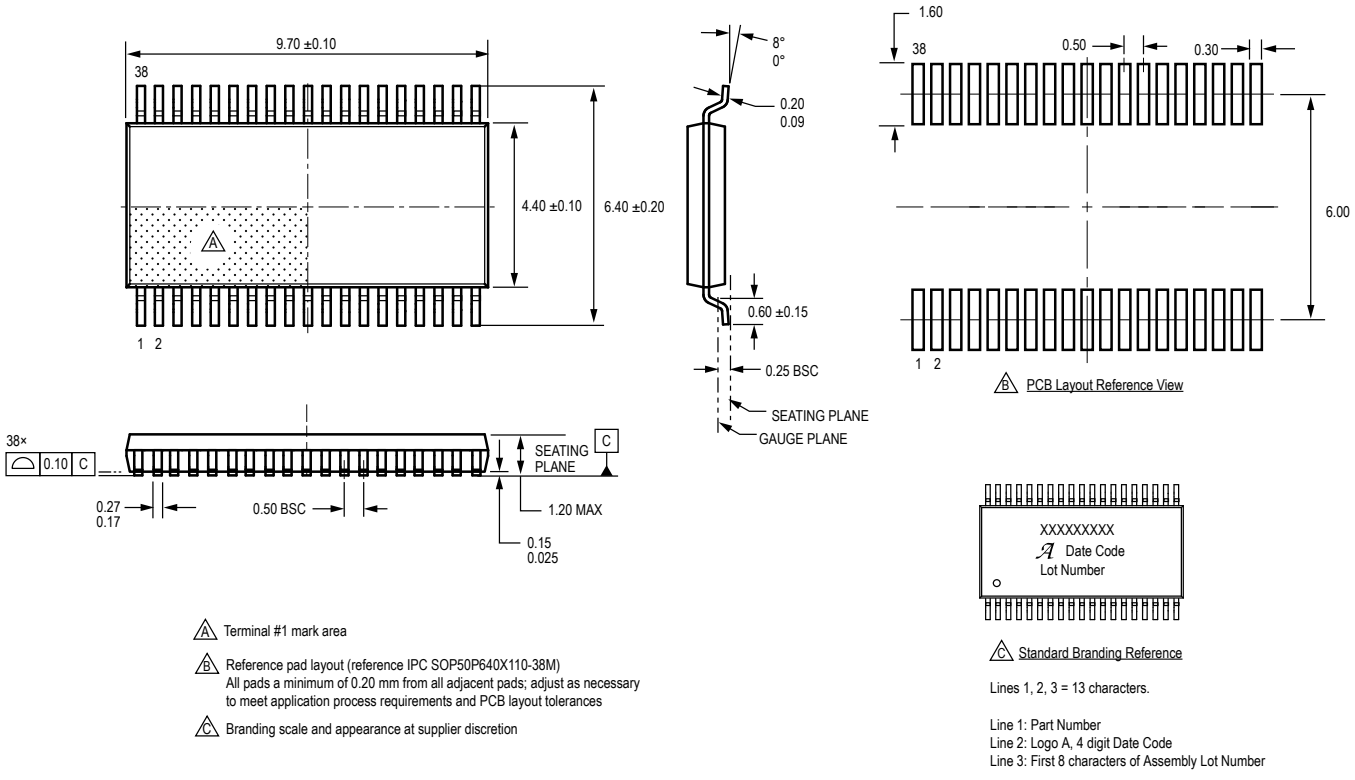
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

LD Package, 38-Pin TSSOP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 BD-1)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference pad layout (reference IPC SOP50P640X110-38M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

C Standard Branding Reference

Lines 1, 2, 3 = 13 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: First 8 characters of Assembly Lot Number

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
5	November 22, 2019	Minor editorial updates
6	December 13, 2021	Updated package drawing (page 15) and minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com