MP6910

Fast Turn-off Intelligent Rectifier

The Future of Analog IC Technology

DESCRIPTION

The MP6910 is a fast turn-off intelligent rectifier for Flyback converters that combines a 100V power switch that replaces diode rectifiers for high efficiency. The chip regulates the forward voltage drop of the internal power switch to about 70mV and turns it off before the voltage goes negative.

FEATURES

- Supports DCM and Quasi-Resonant Flyback converter
- Integrated 10mΩ 100V Power Switch
- Compatible with Energy Star, 1W Standby Requirements
- V_{DD} Range From 8V to 24V
- 70mV V_{DS} Regulation Function (1)
- Max 400kHz Switching Frequency
- Light Load Mode Function (1) with <300uA Quiescent Current
- Supports High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

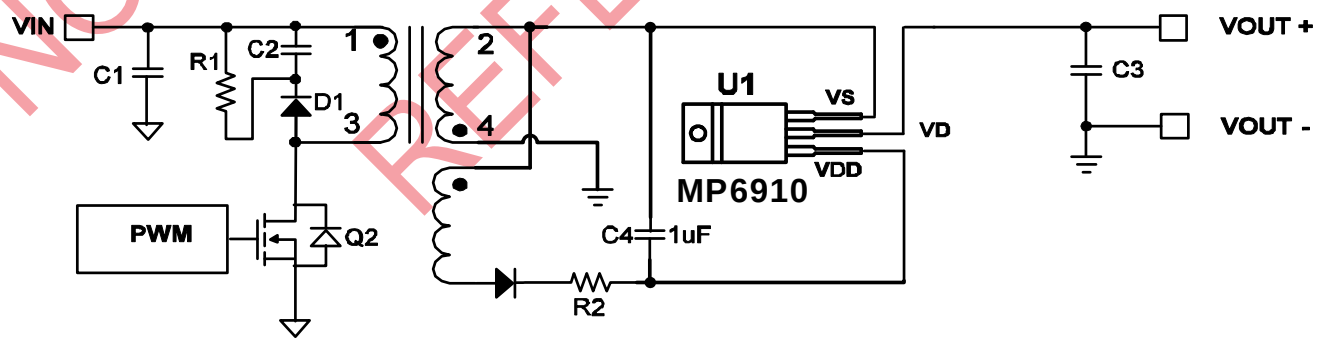
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

Notes:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending

TYPICAL APPLICATION

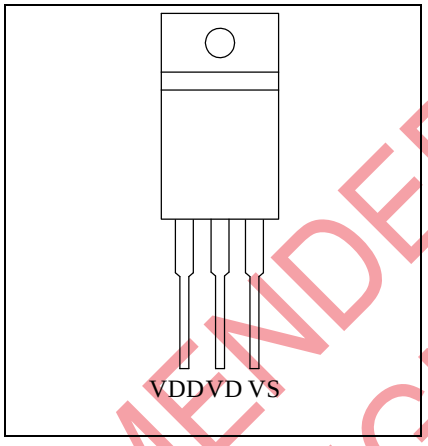


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6910DZ	TO220-3	MP6910DZ

* For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6910DZ–LF)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (2)

V_{DD} to V_S .....-0.3V to +27V
V_D to V_S .....-0.7V to +100V
Maximum Operating Frequency..... 400kHz
Continuous Drain Current (T_C=25°C) 40A
Continuous Drain Current (T_C=100°C) 15A
Maximum Power Dissipation (3) 2.7W
Junction Temperature .....150°C
Lead Temperature (Solder).....260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operation Conditions (4)

V_{DD} to V_S .....8V to 24V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TO220-3	45	3	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) T_A=+25℃. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_A= +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$		100	110		V
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Rising			5.0	6.0	7.0	V
V_{DD} UVLO Hysteresis			0.8	1.2	1.5	V
Operating Current	I_{CC}	F_{SW}=100kHz		4.5	8	mA
Light-Load Mode Current				260	360	µA
CONTROL CIRCUITRY SECTION						
V_{SS} –V_D Forward Voltage	V_{fwd}		55	70	85	mV
Turn-on Delay[6]	T_{Don}			200		ns
Turn off Threshold (V_{SS}-V_D)[6]				30		mV
Turn-off Delay[6]	T_{Doff}	V_D =V_{SS}		30	45	ns
Minimum On-time[6]	T_{MIN}			1.6		µs
Light-load-enter Delay	$T_{LL-Delay}$			120		µs
Light-load-enter Pulse Width	T_{LL}			2.2		µs
Light-load-enter Pulse Width Hysteresis	T_{LL-H}			0.2		µs
Light-load Mode Exit Pulse Width Threshold (V_{DS})	V_{LL-DS}		-400	-250	-150	mV
POWER SWITCH SECTION						
Single Pulse Avalanche Current [7]	I_{AS}			66		A
Single Pulse Avalanche Energy [7]	E_{AS}			597		mJ
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		10.2		mΩ
Input Capacitance	C_{iss}	V_{DS}=40V, f=1MHz		5110		pF
Output Capacitance	C_{oss}			334		pF
Reverse Transfer Capacitance	C_{rss}			150		pF
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{rr}			81		ns
Diode Reverse Change	Q_{rr}			190		nC

Notes:

6) Guaranteed by Design and Characterization.

7) Starting T_J=25°C, L=0.3mH

PIN FUNCTIONS

Pin #	Name	Description
1	VDD	Supply Voltage
2	VD	FET Drain
3	VS	FET Source, also used as reference for VDD

BLOCK DIAGRAM

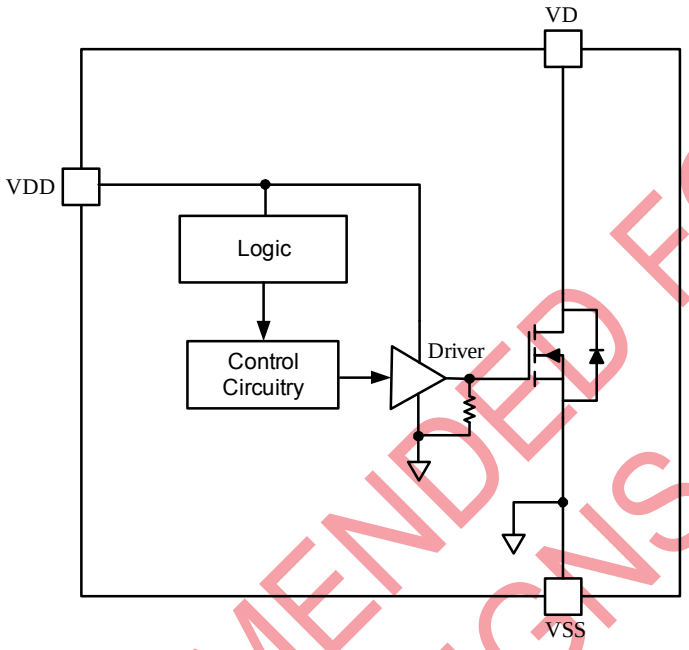


Figure 1—Function Block Diagram

OPERATION

The MP6910 supports operation in DCM and Quasi-Resonant Flyback converters. The control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When it pulls the integrate Mosfet on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is ~1.6us, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold voltage to ~+50mV (instead of -30mV). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower)

Under-Voltage Lockout (UVLO)

When the VDD is below UVLO threshold, the part is in sleep mode and the integrated Mosfet is never turned on.

Basic Operation

The basic operations of flyback converter with MP6910 are:

- **Turn On Phase**

  The switch current will first flow through the body diode of the integrate Mosfet, which generates a negative Vds across it (<-500mV). The voltage is much smaller than the turn on threshold of the control circuitry (-70mV), which turns on the integrate Mosfet after 200ns turn on delay (defined in Fig.2).

- **Conducting Phase**

  When the integrated Mosfet is turned on, Vds becomes to rise according to its on resistance, as soon as Vds rises above the turn on threshold (-70mV), the control circuitry stops pulling up the gate driver, which leads the driver voltage of the integrate Mosfet dropped to larger the on resistance to ease the rise of Vds. By doing that, Vds is adjusted to be around -70mV even when the current through the switch is

fairly small, this function can make the internal driver voltage fairly low when the mosfet is turned off to fast the turn off speed (this function is still active during turn on blanking period which means the integrate mosfet could still be turned off even with very small duty).

Fig.3 shows synchronous rectification operation at heavy load condition. Due to the high current, the internal driver voltage will be saturated at first. After Vds goes to above -70mV, driver voltage decreases to adjust the Vds to typical -70mV.

Fig.4 shows synchronous rectification operation at light load condition. Due to the low current, the driver voltage never saturates but begins to decrease as soon as the integrated mosfet is turned on and adjust the Vds.

- **Turn Off Phase**
  When Vds rises to trigger the turn off threshold (-30mV), the driver voltage of the switch is pulled to low after about 20ns turn off delay (defined in Fig.2) by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the switch is turned off to avoid error trigger.

Light-load Latch-off Function

The gate driver of integrate Mosfet in MP6910 is latched to save the driver loss at light-load condition to improve efficiency. The light-load-enter pulse width T_{LL} is internal fixed (~2.2μs). When synchronous power switch conducting period keeps lower than T_{LL} for longer than the light-load-enter delay ($T_{LL\text{-}Delay}$), MP6910 enters light-load mode and latches off the integrate Mosfet (Fig.5 for detail).

During light-load mode, MP6910 monitors the integrate Mosfet body diode conducting period by sensing V_{DS} (when V_{DS} exceeds the light-load mode exit pulse width threshold $V_{LL\text{-}DS}$, MP6910 considers the integrate Mosfet body diode conducting time finishes). If the Mosfet body diode conduction time is longer than $T_{LL}+T_{LL\text{-}H}$ ($T_{LL\text{-}H}$, light-load-enter pulse width hysteresis), the light-load mode is finished and the integrate Mosfet of MP6910 is unlatched to restart the synchronous rectification (Fig.6 for detail).

Typical System Implementations

Fig.7 shows the typical system implementation for the IC supply derived from output voltage, which is available in low-side rectification and the output voltage is recommended to be in the VDD range of MP6910 (from 8V to 24V).

If output voltage is out of the V_{DD} range of MP6910 or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply, which is shown in Fig.8 and Fig.9.

There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding. See fig.10 and fig.11, compared with using auxiliary winding for IC supply, this solution has a bit higher power loss which is dissipate on the LDO circuit especially when the secondary winding voltage is high.

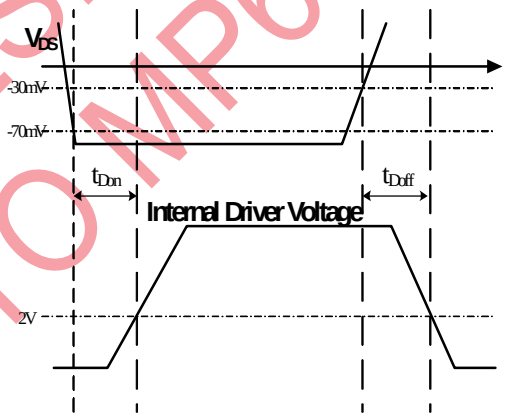


Figure 2—Turn on and Turn off delay

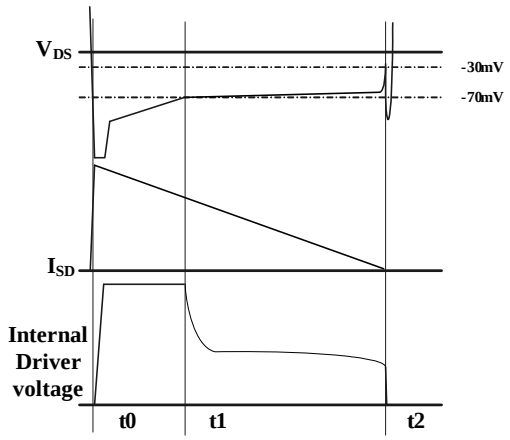


Figure 3—Synchronous Rectification Operation at heavy load

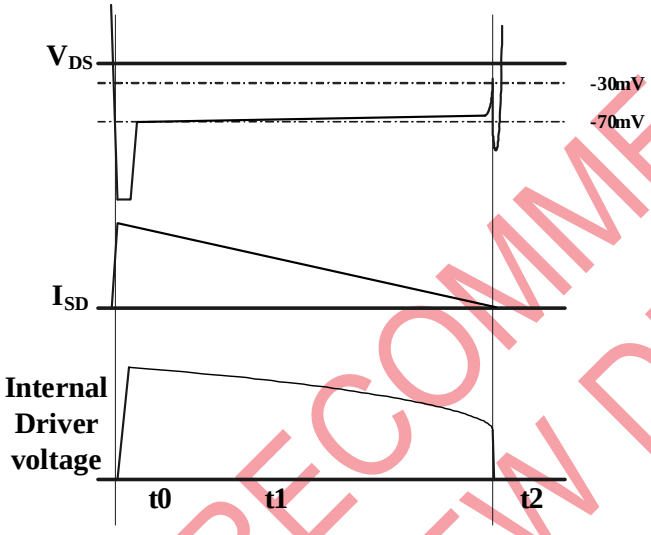


Figure 4—Synchronous Rectification Operation at light load

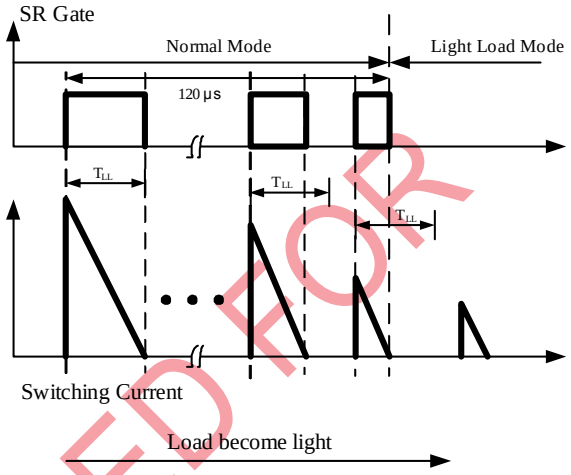


Figure 5—Enter Light Load Mode

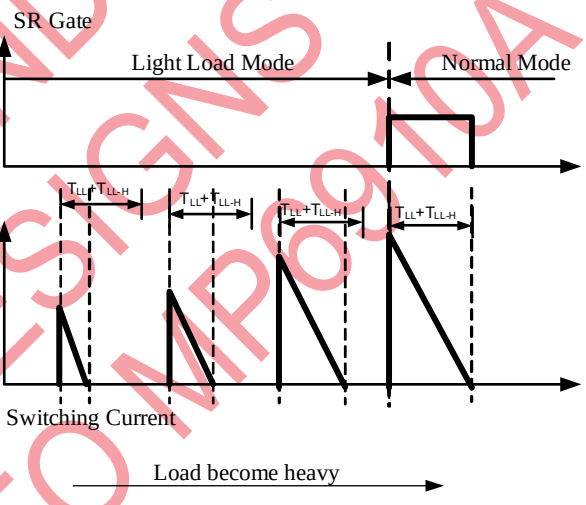


Figure 6—Exit Light Load Mode

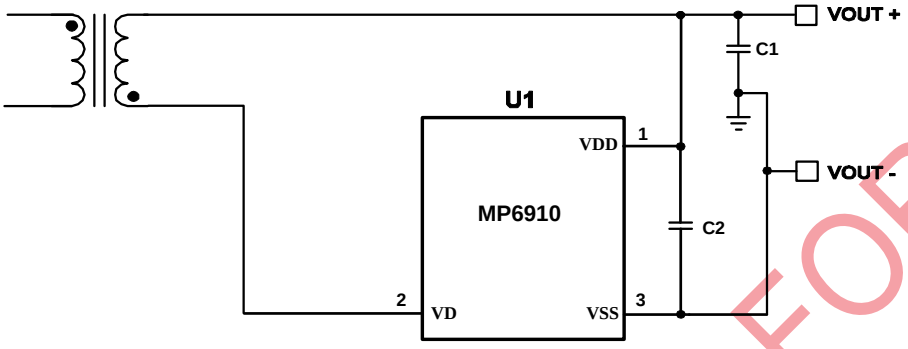


Figure 7—IC supply derived directly from output voltage

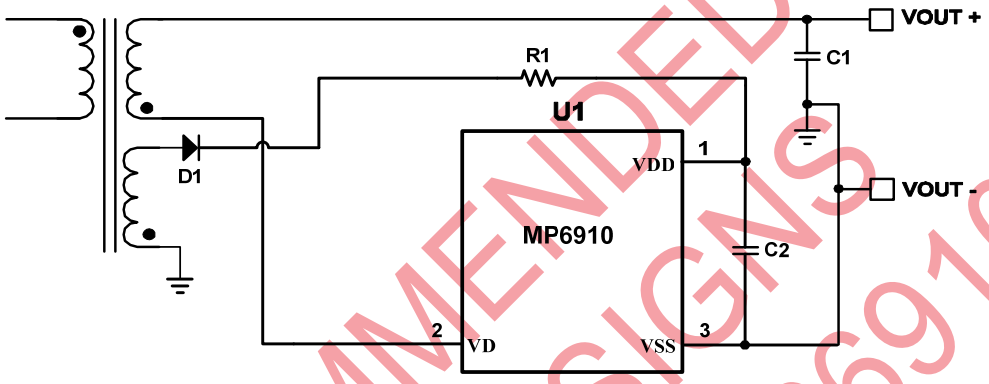


Figure 8—IC supply derived from auxiliary winding in low-side rectification

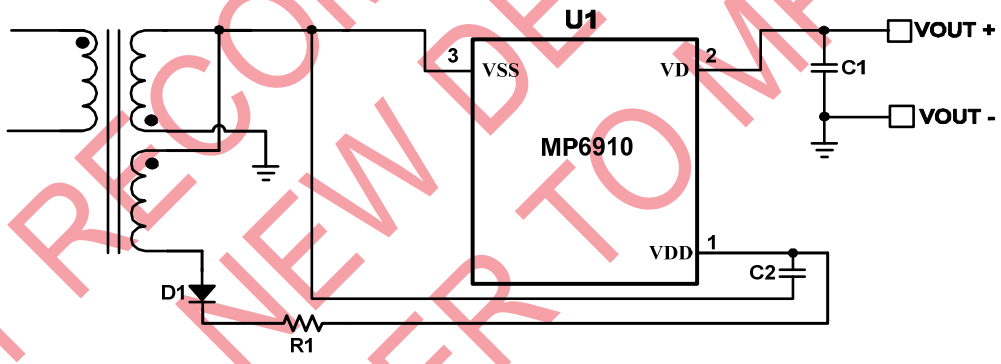


Figure 9—IC supply derived from auxiliary winding in high-side rectification

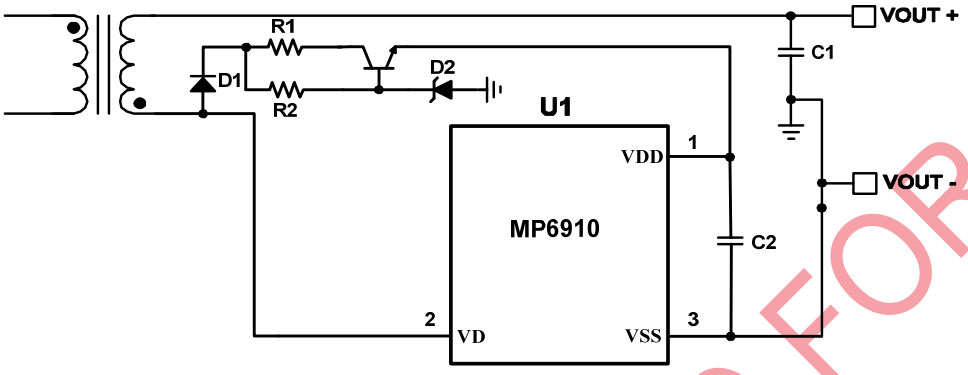


Figure 10—IC supply derived from secondary winding in low-side rectification

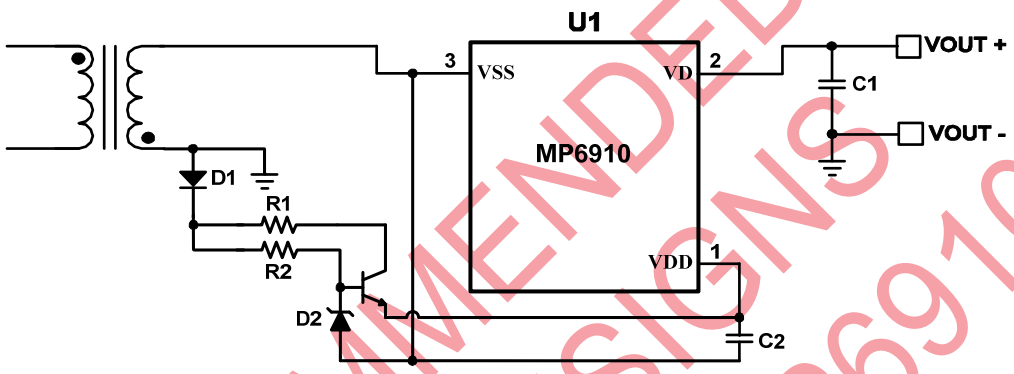
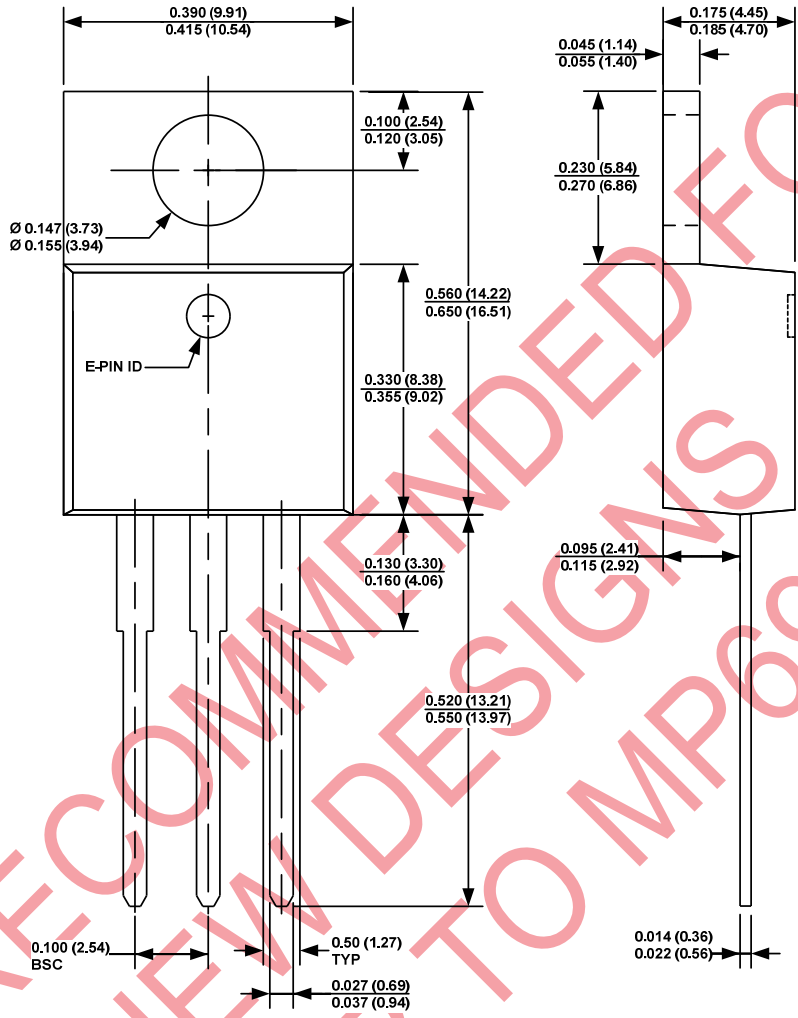


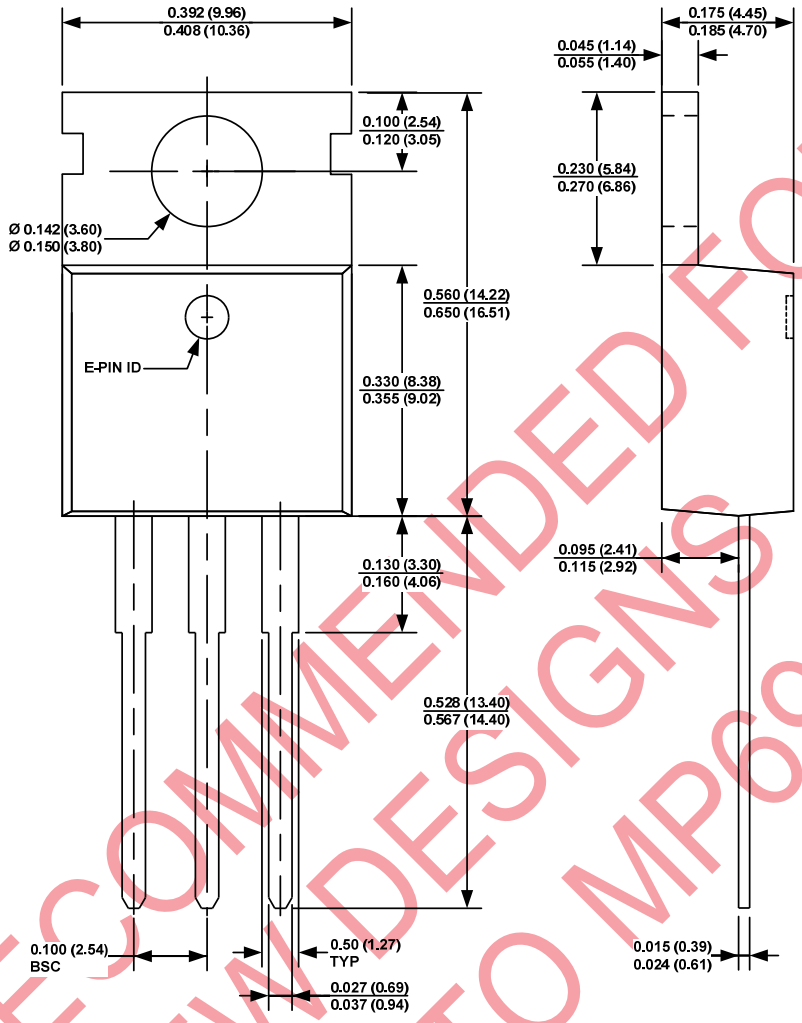
Figure 11—IC supply derived from secondary winding in high-side rectification

PACKAGE INFORMATION



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) DRAWING CONFORMS TO JEDEC TO-220
6) DRAWING IS NOT TO SCALE.



TOP VIEW **SIDE VIEW**

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