CS5101

Secondary Side Post Regulator for AC/DC and DC/DC Multiple Output Converters

The CS5101 is a bipolar monolithic secondary side post regulator (SSPR) which provides tight regulation of multiple output voltages in AC/DC or DC/DC converters. Leading edge pulse width modulation is used with the CS5101.

The CS5101 is designed to operate over an 8.0 V to 45 V supply voltage (V_{CC}) range and up to a 75 V drive voltage (V_C).

The CS5101 features include a totem pole output with 1.5 A peak output current capability, externally programmable overcurrent protection, an on chip 2.0% precision 5.0 V reference, internally compensated error amplifier, externally synchronized switching frequency, and a power switch drain voltage monitor. It is available in a 14 lead plastic DIP or a 16 lead wide body SOIC package.

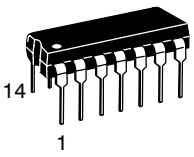
Features

- 1.5 A Peak Output (Grounded Totem Pole)
- 8.0 V to 75 V Gate Drive Voltage
- 8.0 V to 45 V Supply Voltage
- 300 ns Propagation Delay
- 1.0% Error Amplifier Reference Voltage
- Lossless Turn On and Turn Off
- Sleep Mode: < 100 μA
- Overcurrent Protection with Dedicated Differential Amp
- Synchronization to External Clock
- External Power Switch Drain Voltage Monitor
- Pb−Free Packages are Available*

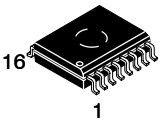
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

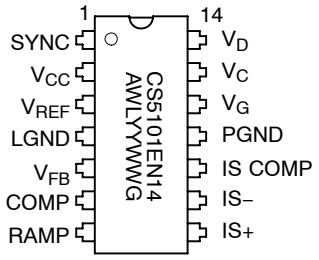


PDIP−14
N SUFFIX
CASE 646

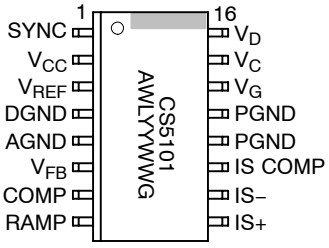


SO−16WB
DW SUFFIX
CASE 751G

MARKING DIAGRAMS AND PIN ASSIGNMENTS



PDIP−14



SO−16WB

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

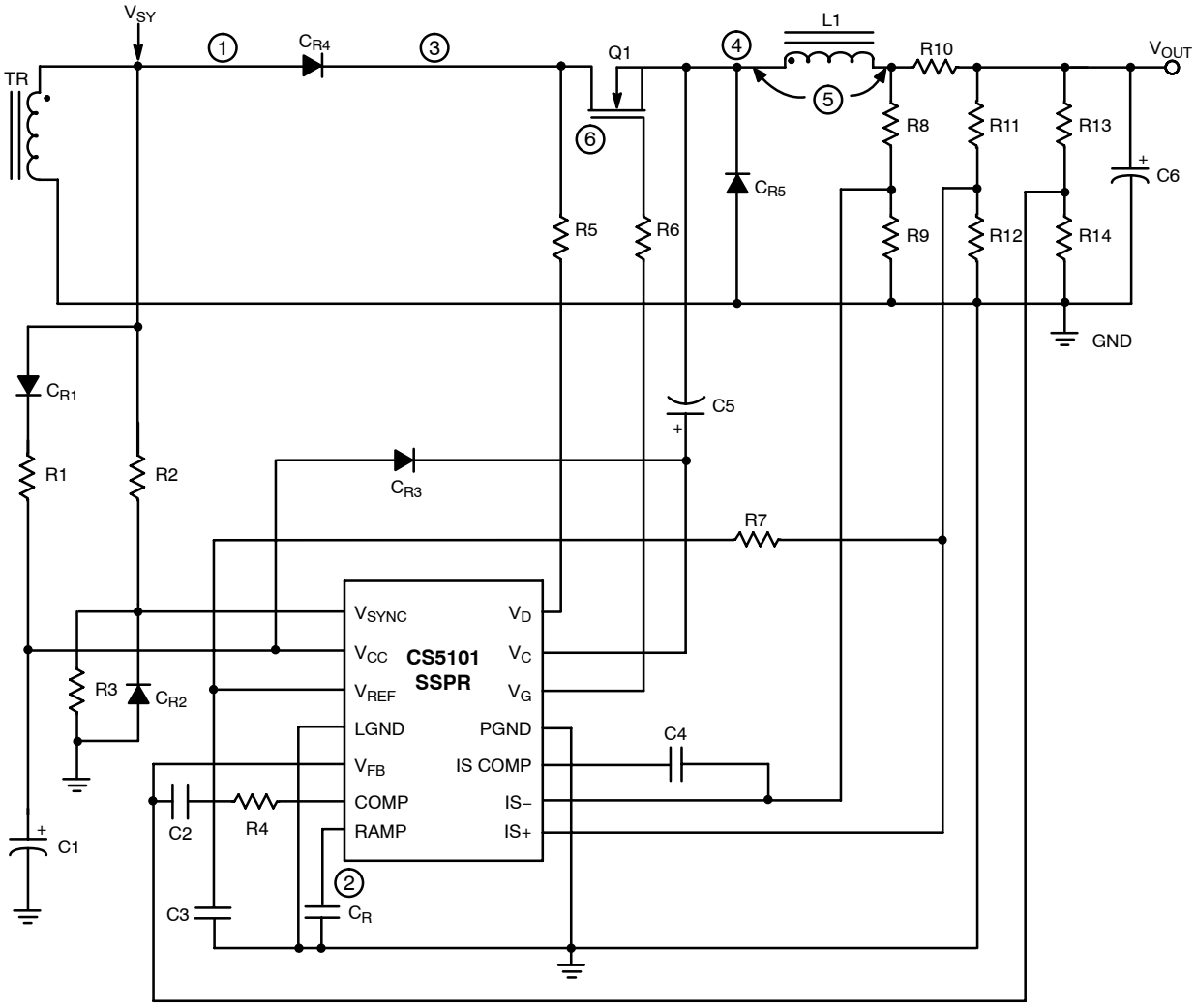


Figure 1. Application Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage, V_{CC}		−0.3 to 45	V
V_{SYNC} and Output Supply Voltages, V_C, V_G, V_{SYNC}, V_D		−0.3 to 75	V
V_{IS+}, V_{IS-} (V_{CC} − 4.0 V, up to 24 V)		−0.3 to 24	V
V_{REF}, V_{FB}, V_{COMP}, V_{RAMP}, V_{ISCOMP}		−0.3 to 10	V
Operating Junction Temperature, T_J		−40 to +150	°C
Operating Temperature Range		−40 to +85	°C
Storage Temperature Range		−65 to +150	°C
Output Energy (Capacitive Load Per Cycle)		5.0	μJ
ESD Human Body		2.0	kV
Lead Temperature Soldering	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 second maximum
2. 60 second maximum above 183°C

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, $-40°C \le T_J \le 150°C$, $10\ V < V_{CC} < 45\ V$, $8.0\ V < V_C < 75\ V$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
Input Voltage Initial Accuracy	$V_{FB} = V_{COMP}$, V_{CC} = 15 V, T = 25°C, Note 3	1.98	2.00	2.02	V
Input Voltage	$V_{FB} = V_{COMP}$, includes line and temp	1.94	2.00	2.06	V
Input Bias Current	V_{FB} = 0 V, IV_{FB} flows out of pin	–	–	500	nA
Open Loop Gain	$1.5\ V < V_{COMP} < 3.0\ V$	60	70	–	dB
Unity Gain Bandwidth	$1.5\ V < V_{COMP} < 3.0\ V$, Note 3	0.7	1.0	–	MHz
Output Sink Current	V_{COMP} = 2.0 V, V_{FB} = 2.2 V	2.0	8.0	–	mA
Output Source Current	V_{COMP} = 2.0 V, V_{FB} = 1.8 V	2.0	6.0	–	mA
V_{COMP} High	V_{FB} = 1.8 V	3.3	3.5	3.7	V
V_{COMP} Low	V_{FB} = 2.2 V	0.85	1.0	1.15	V
PSRR	$10\ V < V_{CC} < 45\ V$, $V_{FB} = V_{COMP}$, Note 3	60	70	–	dB
Voltage Reference					
Output Voltage Initial Accuracy	V_{CC} = 15 V, T = 25°C, Note 3	4.9	5.0	5.1	V
Output Voltage	$0\ A < I_{REF} < 8.0\ mA$	4.8	5.0	5.2	V
Line Regulation	$10\ V < V_{CC} < 45\ V$, I_{REF} = 0 A	–	10	60	mV
Load Regulation	$0\ A < I_{REF} < 8.0\ mA$	–	20	60	mV
Current Limit	V_{REF} = 4.8 V	10	50	–	mA
$V_{REF_}$OK FAULT V	V_{SYNC} = 5.0 V, $V_{REF} = V_{LOAD}$	4.10	4.40	4.60	V
$V_{REF_}$OK V	V_{SYNC} = 5.0 V, $V_{REF} = V_{LOAD}$	4.30	4.50	4.80	V
$V_{REF_}$OK Hysteresis	–	40	100	250	mV
Current Sense Amplifier					
IS COMP High V	IS+ = 5.0 V, IS− = IS COMP	4.7	5.0	5.3	V
IS COMP Low V	IS+ = 0 V, IS− = IS COMP	0.5	1.0	1.3	V
Source Current	IS+ = 5.0 V, IS− = 0 V	2.0	10	–	mA
Sink Current	IS− = 5.0 V, IS+ = 0 V	10	20	–	mA
Open Loop Gain	$1.5\ V \le V_{COMP} \le 4.5\ V$, R_L = 4.0 kΩ	60	80	–	dB
CMRR	Note 3	60	80	–	dB
PSRR	$10\ V < V_{CC} < 45\ V$, Note 3	60	80	–	dB
Unity Gain Bandwidth	$1.5\ V \le V_{COMP} \le 4.5\ V$, R_L = 4.0 kΩ, Note 3	0.5	0.8	–	MHz
Input Offset Voltage	$V_{IS}+ = 2.5\ V$, $V_{IS}- = V_{ISCOMP}$	−8.0	0	8.0	mV
Input Bias Currents	$V_{IS}+ = V_{IS}- = 0\ V$, I_{IS} flows out of pins	–	20	250	nA
Input Offset Current (IS+, IS−)	–	−250	0	250	nA
Input Signal Voltage Range	Note 3	−0.3	–	V_{CC} − 4.0	V
RAMP/SYNC Generator					
RAMP Source Current Initial Accuracy	V_{SYNC} = 5.0 V, V_{RAMP} = 2.5 V, T = 25°C, Note 3	0.18	0.20	0.22	mA
RAMP Source Current	V_{SYNC} = 5.0 V, V_{RAMP} = 2.5 V	0.16	0.20	0.24	mA
RAMP Sink Current	V_{SYNC} = 0 V, V_{RAMP} = 2.5 V	1.0	4.0	–	mA
RAMP Peak Voltage	V_{SYNC} = 5.0 V	3.3	3.5	3.7	V
RAMP Valley Voltage	V_{SYNC} = 0 V	1.4	1.5	1.6	V
RAMP Dynamic Range	$V_{RAMPDR} = V_{RAMPPK} - V_{RAMPVY}$	1.7	2.0	2.3	V
RAMP Sleep Threshold Voltage	V_{RAMP} @ $V_{REF} < 2.0\ V$	0.3	0.6	1.0	V
SYNC Threshold	V_{SYNC} @ $V_{RAMP} > 2.5\ V$	2.3	2.5	2.7	V
SYNC Input Bias Current	V_{SYNC} = 0 V, I_{SYNC} flows out of pin	–	1.0	20	μA

3. Guaranteed by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, $-40°C \le T_J \le 150°C$, $10\ V < V_{CC} < 45\ V$, $8.0\ V < V_C < 75\ V$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
V_G, High	V_{SYNC} = 5.0 V, IV_G = 200 mA, $V_C - V_G$	–	1.6	2.5	V
V_G, Low	V_{SYNC} = 0 V, IV_G = 200 mA	–	0.9	1.5	V
V_G Rise Time	Switch V_{SYNC} High, C_G = 1.0 nF, V_{CC} = 15 V, measure 2.0 V to 8.0 V	–	30	75	ns
V_G Fall Time	Switch V_{SYNC} Low, C_G = 1.0 nF, V_{CC} = 15 V, measure 8.0 V to 2.0 V	–	40	100	ns
V_G Resistance to GND	Remove supplies, V_G = 10 V	–	50	100	kΩ
V_D Resistance to GND	Remove supplies, V_D = 10 V	500	1500	–	Ω
General					
I_{CC}, Operating	V_{SYNC} = 5.0 V	–	12	18	mA
I_{CC} in UVL	V_{CC} = 6.0 V	–	300	500	μA
I_{CC} in Sleep Mode High	V_{RAMP} = 0 V, V_{CC} = 45 V	–	80	200	μA
I_{CC} in Sleep Mode Low	V_{RAMP} = 0 V, V_{CC} = 10 V	–	20	50	μA
I_C, Operating High	V_{SYNC} = 5.0 V, $V_{FB} = V_{IS-}$ = 0 V, V_C = 75 V	–	4.0	8.0	mA
I_C, Operating Low	V_{SYNC} = 5.0 V, $V_{FB} = V_{IS-}$ = 0 V, V_C = 8.0 V	–	3.0	6.0	mA
UVLO Start Voltage	–	7.4	8.0	9.2	V
UVLO Stop Voltage	–	6.4	7.0	8.3	V
UVLO Hysteresis	–	0.8	1.0	1.2	V
Leading Edge, t_{DELAY}	V_{SYNC} = 2.5 V to V_G = 8.0 V	–	280	–	ns
Trailing Edge, t_{DELAY}	V_{SYNC} = 2.5 V to V_G = 2.0 V	–	750	–	ns

PACKAGE PIN DESCRIPTION

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
PDIP−14	SO−16WB		
1	1	SYNC	Synchronization input.
2	2	V_{CC}	Logic supply (10 V to 45 V).
3	3	V_{REF}	5.0 V voltage reference.
4	–	LGND	Logic level ground (analog and digital ground tied).
5	6	V_{FB}	Error amplifier inverting input.
6	7	COMP	Error amplifier output and compensation.
7	8	RAMP	RAMP programmable with the external capacitor.
8	9	IS+	Current sense amplifier non−inverting input.
9	10	IS−	Current sense amplifier inverting input.
10	11	IS COMP	Current sense amplifier compensation and output.
11	12, 13	PGND	Power ground.
12	14	V_G	External power switch gate drive.
13	15	V_C	Output power stage supply voltage (8.0 V to 75 V).
14	16	V_D	External FET DRAIN voltage monitor.
–	5	AGND	Analog ground.
–	4	DGND	Digital ground.

ORDERING INFORMATION

Device	Package	Shipping†
CS5101EN14	PDIP−14	25 Units / Rail
CS5101EN14G	PDIP−14 (Pb−Free)	
CS5101EDW16	SOIC−16WB	47 Units / Rail
CS5101EDW16G	SOIC−16WB (Pb−Free)	
CS5101EDWR16	SOIC−16WB	1000 / Tape & Reel
CS5101EDWR16G	SOIC−16WB (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

CIRCUIT DESCRIPTION

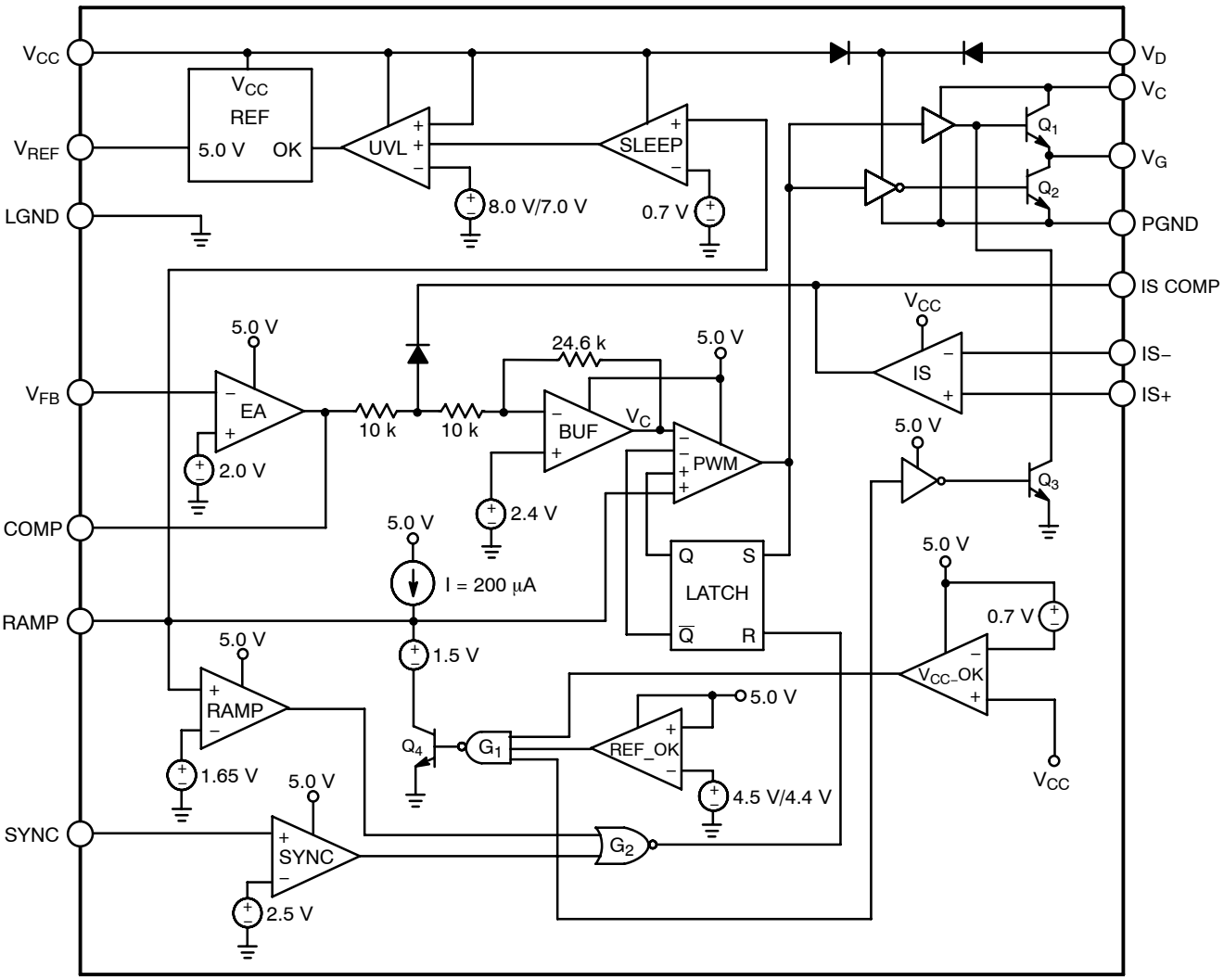


Figure 2. Block Diagram

Theory of Operation

The CS5101 is designed to regulate voltages in multiple output power supplies. Functionally, it is similar to a magnetic amplifier, operating as a switch with a delayed turn−on. It can be used with both single ended and dual ended topologies.

The V_{FB} voltage is monitored by the error amplifier EA. It is compared to an internal reference voltage and the amplified differential signal is fed through an inverting amplifier into the buffer, BUF. The buffered signal is compared at the PWM comparator with the ramp voltage generated by capacitor C_R. When the ramp voltage V_R, exceeds the control voltage V_C, the output of the PWM comparator goes high, latching its state through the LATCH, the output stage transistor Q_1 turns on, and the external power switch, usually an N−FET, turns on.

SYNC Function

The SYNC circuit is activated at time t_1 (Figure 3) when the voltage at the SYNC pin exceeds the threshold level (2.5V) of the SYNC comparator. The external ramp capacitor C_R is allowed to charge through the internal current source I (200 μA). At time t_2, the ramp voltage intersects with the control voltage V_C and the output of the PWM comparator goes high, turning on the output stage and the external power switch. At the same time, the PWM comparator is latched by the RS latch, LATCH.

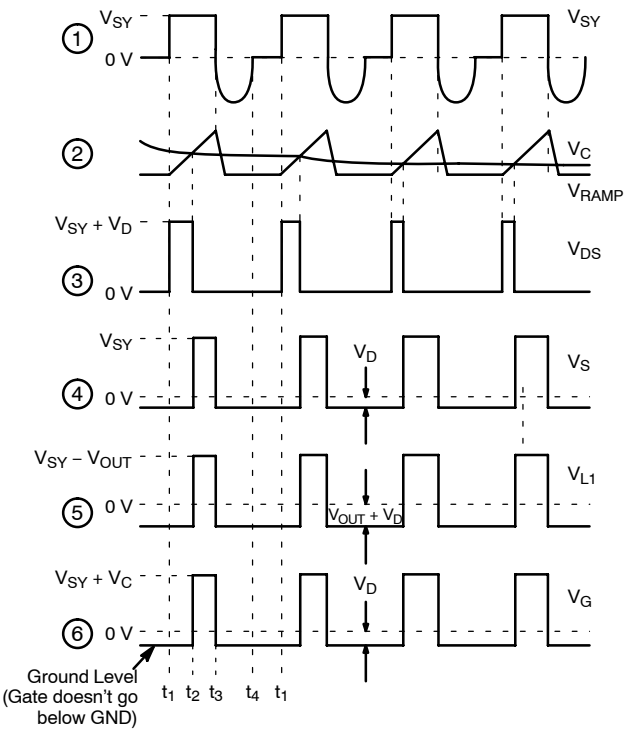


Figure 3. Waveforms for CS5101. The Number to the Left of Each Curve Refers to a Node On the Application Diagram on Page 2.

The logic state of the LATCH can be changed only when both the voltage level of the trailing edge of the power pulse at the SYNC pin is less than the threshold voltage of the SYNC comparator (2.5 V) and the RAMP voltage is less than the threshold voltage of the RAMP comparator (1.65 V). On the negative going transition of the secondary side pulse V_{SY}, gate G_2 output goes high, resetting the latch at time t_3. Capacitor C_R is discharged through transistor Q_4. C_R's output goes low disabling the output stage, and the external power switch (an N−FET) is turned off.

RAMP Function

The value of the ramp capacitor C_R is based on the switching frequency of the regulator and the maximum duty cycle of the secondary pulse V_{SY}.

If the RAMP pin is pulled externally to 0.3 V or below, the SSPR is disabled. Current drawn by the IC is reduced to less than 100 μA, and the IC is in SLEEP mode.

FAULT Function

The voltage at the V_{CC} pin is monitored by the undervoltage lockout comparator with hysteresis. When V_{CC} falls below the UVL threshold, the 5.0 V reference and all the circuitry running off of it is disabled. Under this condition the supply current is reduced to less than 500 μA.

The V_{CC} supply voltage is further monitored by the V_{CC}_OK comparator. When V_{CC} is reduced below V_{REF} – 0.7 V, a fault signal is sent to gate G_1. This fault signal, which determines if V_{CC} is absent, works in conjunction with the ramp signal to disable the output, but only after the current cycle has finished and the RS latch is reset. Therefore this fault will not cause the output to turn off during the middle of an on pulse, but rather will utilize lossless turn−off. This feature protects the FET from overvoltage stress. This is accomplished through gate G_1 by driving transistor Q_4 on.

An additional fault signal is derived from the REF_OK comparator. V_{REF} is monitored so to disable the output through gate G_1 when the V_{REF} voltage falls below the OK threshold. As in the V_{CC}_OK fault, the REF_OK fault disables the output after the current cycle has been completed. The fault logic will operate normally only when V_{REF} voltage is within the specification limits of REF_OK.

DRAIN Function

The drain pin, V_D monitors the voltage on the drain of the power switch and derives energy from it to keep the output stage in an off state when V_C or V_{CC} is below the minimum specified voltage.

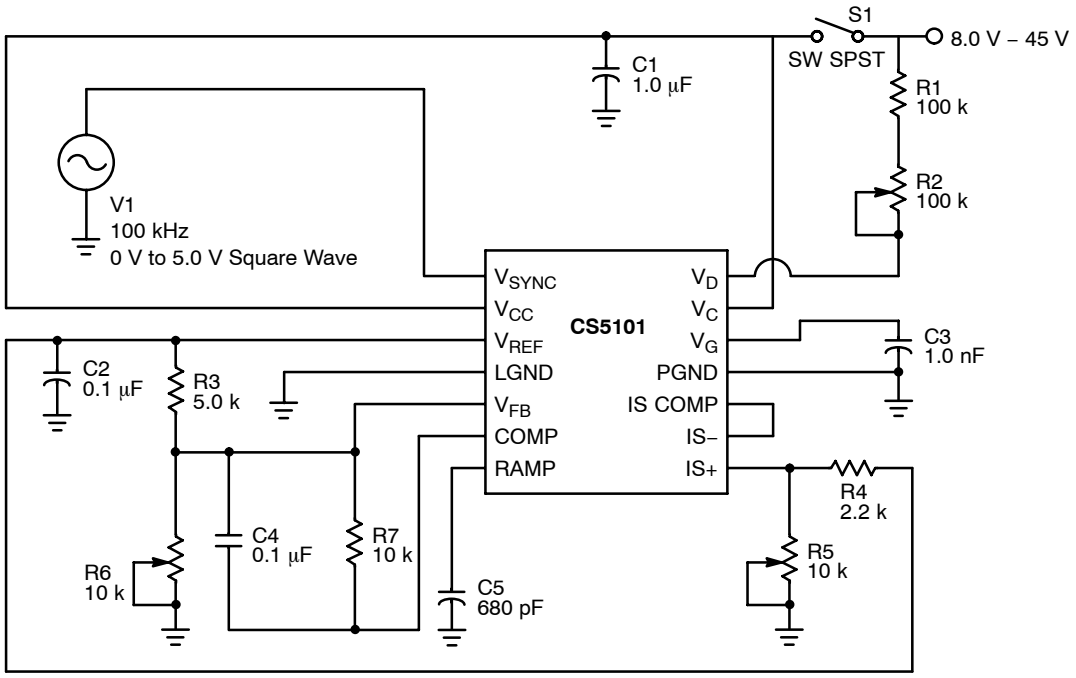


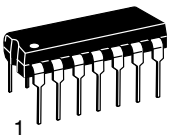
Figure 4. CS5101 Bench Test on DIP−14 Package

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

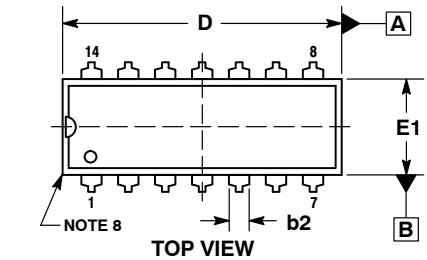
ON Semiconductor®

PDIP−14
CASE 646−06
ISSUE S

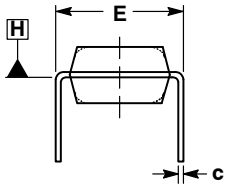
DATE 22 APR 2015



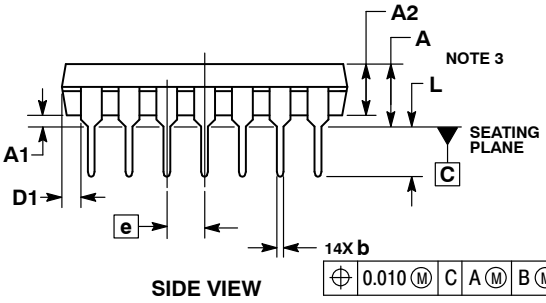
SCALE 1:1



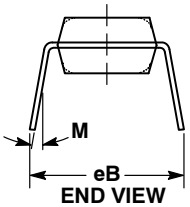
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

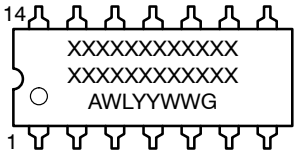


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42428B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	PDIP−14		PAGE 1 OF 2

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

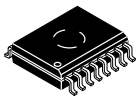
STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

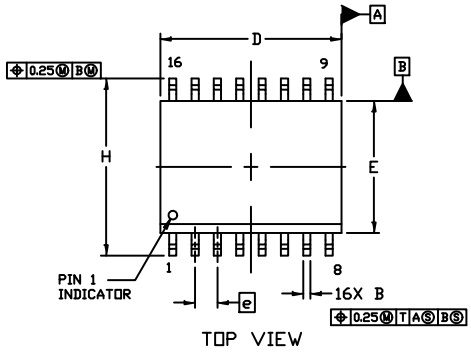
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

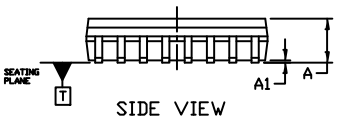
DATE 08 OCT 2021



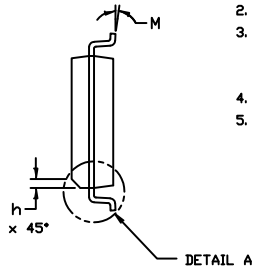
1
SCALE 1:1



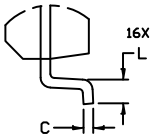
TOP VIEW



SIDE VIEW



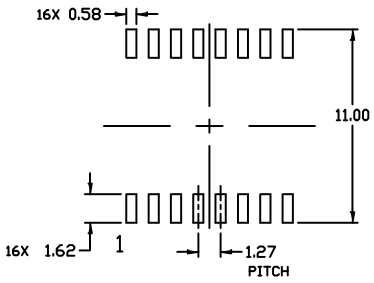
END VIEW



DETAIL A
2X SCALE

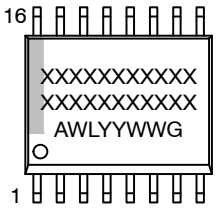
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

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