



# MPQ2179A

## 5.5V, 3A, 2.4MHz, Synchronous Step-Down Converter with Power Good and Soft Start, AEC-Q100 Qualified

### DESCRIPTION

The MPQ2179A is a monolithic, step-down, switch-mode converter with integrated internal power MOSFETs. It can achieve up to 3A of output current ( $I_{OUT}$ ) across a 2.5V to 5.5V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation. The output voltage ( $V_{OUT}$ ) can be regulated to as low as 0.6V.

The MPQ2179A is ideal for a wide range of applications, including automotive clusters, telematics, and infotainment systems.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization.

Full protection features include cycle-by-cycle current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ2179A requires a minimal number of readily available, standard external components, and is available in a compact QFN-8 (1.5mmx2mm) package.

### FEATURES

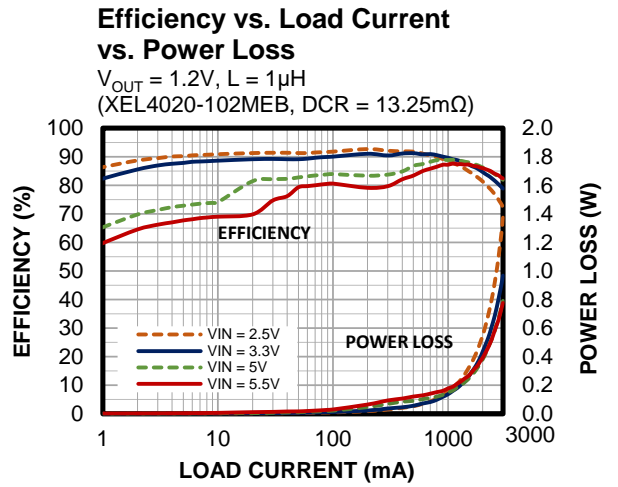
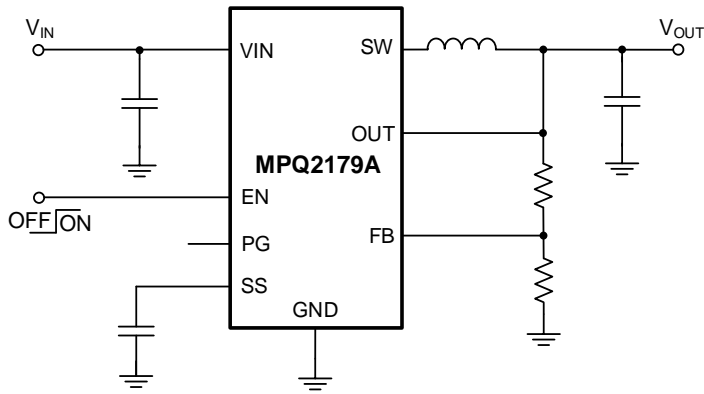
- **Designed for Automotive Applications:**
  - Wide 2.5V to 5.5V Operating Input Voltage ( $V_{IN}$ ) Range
  - Up to 3A Output Current ( $I_{OUT}$ )
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C Operating Junction Temperature ( $T_J$ ) Range
  - Available in AEC-Q100 Grade 1
- **Increased Battery Life:**
  - 21 $\mu$ A Sleep Mode Quiescent Current ( $I_Q$ )
  - AAM Mode for Increased Efficiency under Light-Load Conditions
- **High Performance for Improved Thermals:**
  - 65m $\Omega$  and 35m $\Omega$  Integrated Internal Power MOSFETs
- **Optimized for EMC and EMI:**
  - 2.4MHz Switching Frequency ( $f_{SW}$ )
  - MeshConnect™ Flip-Chip Package
- **Optimized for Board Size and BOM:**
  - Integrated Internal Power MOSFETs
  - Integrated Compensation Network
  - Available in a Compact QFN-8 (1.5mmx2mm) Package
- **Additional Features:**
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - OVP and SCP with Hiccup Mode
  - Available in a Wettable Flank Package

### APPLICATIONS

- Automotive Clusters, Telematics, and Infotainment Systems
- Camera Modules
- Key Fobs
- Industrial Supplies
- Battery-Powered Devices

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2179AGQHE-AEC1***	QFN-8 (1.5mmx2mm)	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MPQ2179AGQHE-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable Flank

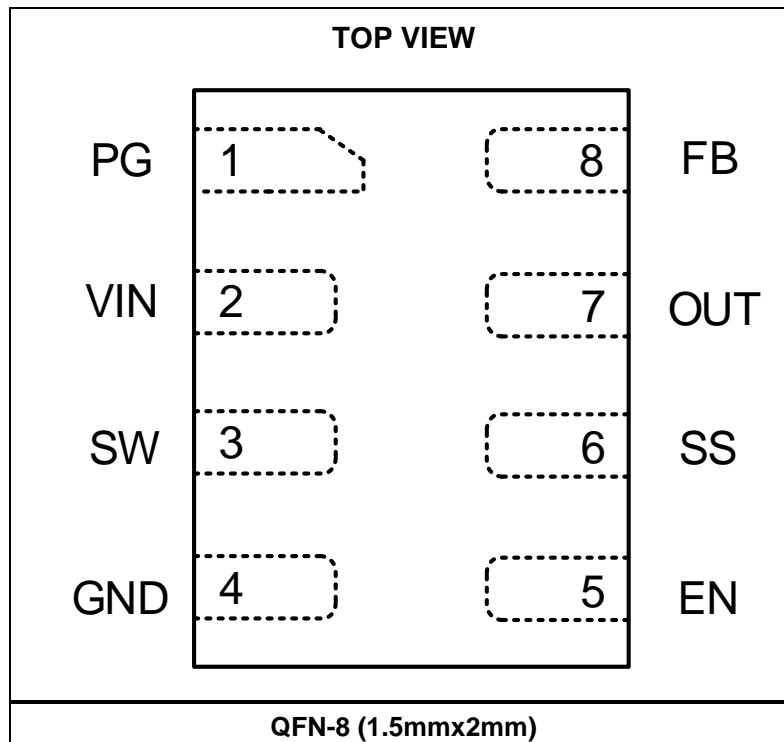
### TOP MARKING

—  
**MC**  
**LL**

MC: Product code of the MPQ2179AGQHE-AEC1

LL: Lot number

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	PG	<b>Power good indicator.</b> The PG pin is an open-drain output. Connect PG to a voltage source via an external resistor. If the feedback (FB) voltage ( $V_{FB}$ ) exceeds 90% of the reference voltage ( $V_{REF}$ ), then PG is pulled high. If $V_{FB}$ drops below 85% of $V_{REF}$ , then PG is pulled to GND. Float this pin if not used.
2	VIN	<b>Supply voltage.</b> The MPQ2179A operates from a 2.5V to 5.5V input. A decoupling capacitor is required to prevent large voltage spikes at the input.
3	SW	<b>Output switching node.</b> The SW pin is the drain of the internal P-channel high-side MOSFET (HS-FET). Connect the inductor to SW to complete the converter.
4	GND	<b>Ground.</b>
5	EN	<b>Enable (EN) control.</b> Pull the EN pin above 0.9V to turn the converter on; pull EN below 0.65V or float EN to turn it off. There is an internal 2M $\Omega$ resistor connected between EN and GND.
6	SS	<b>Soft start.</b> Connect a capacitor between SS and GND to set the soft-start time ( $t_{SS}$ ) and to avoid start-up inrush current. The recommended minimum soft-start capacitance ( $C_{SS}$ ) is 1nF.
7	OUT	<b>Output voltage (<math>V_{OUT}</math>).</b> The OUT pin is $V_{OUT}$ 's power rail and input sense. Connect OUT to the load. An output capacitor (C2) is required to reduce the output voltage ripple ( $\Delta V_{OUT}$ ).
8	FB	<b>Feedback (FB).</b> The FB pin is tapped to an external resistor divider connected between the output and GND. To set the regulation voltage, $V_{FB}$ is compared to the internal $V_{REF}$ (0.6V).

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

All pins .....	-0.3V to +6.5V
Junction temperature .....	150°C
Lead temperature .....	260°C
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2) (5)</sup>	2.2W
Storage temperature .....	-65°C to +150°C

### ESD Ratings

Human body model (HBM) .....	$\pm 2000\text{V}$
Charged device model (CDM) .....	$\pm 750\text{V}$

### Recommended Operating Conditions

Input voltage ( $V_{IN}$ ) .....	2.5V to 5.5V
Output voltage ( $V_{OUT}$ ) .....	0.6V to $V_{IN} - 0.5\text{V}$
Operating junction temp ( $T_J$ ) ....	-40°C to +150°C

### Thermal Resistance

 $\theta_{JA}$     $\theta_{JC}$ 

QFN-8 (1.5mmx2mm)		
JESD51-7 <sup>(3) (4)</sup> .....	130.....25.....	°C/W
EVQ2179A-LE-00A <sup>(5)</sup> .....	59.....14.....	°C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.
- The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- Measured on the EVQ2179A-LE-00A, a 4-layer, 6.3cmx6.3cm PCB with 2oz per layer.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage	$V_{IN}$		2.5		5.5	V
Under-voltage lockout (UVLO) rising threshold	$V_{UVLO\_RISING}$			2.3	2.45	V
UVLO threshold hysteresis	$V_{UVLO\_HYS}$			200		mV
Shutdown current	$I_{SD}$	$V_{EN} = 0V$ , $T_J = 25^{\circ}C$		0.01	1	$\mu A$
		$V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(6)</sup>			3	$\mu A$
		$V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$			20	$\mu A$
Quiescent current	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = 25^{\circ}C$		21	30	$\mu A$
		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(6)</sup>			40	$\mu A$
		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$			80	$\mu A$
Feedback (FB) voltage	$V_{FB}$	$T_J = 25^{\circ}C$	594	600	606	mV
		$T_J = -40^{\circ}C$ to $+150^{\circ}C$	591	600	609	
FB current	$I_{FB}$	$V_{FB} = 0.63V$		50	100	nA
P-channel high-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	$V_{IN} = 5V$		65	85	m $\Omega$
N-channel low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	$V_{IN} = 5V$		35	55	m $\Omega$
Zero-current detection (ZCD) threshold				50		mA
Switch leakage current		$V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = 25^{\circ}C$		0	1	$\mu A$
		$V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(6)</sup>			30	$\mu A$
Switching frequency	$f_{SW}$	$V_{IN} = 5V$ , $V_{OUT} = 1.2V$ , CCM	2000	2400	2640	kHz
Minimum on time <sup>(6)</sup>	$t_{ON\_MIN}$	$V_{IN} = 5V$		50		ns
Minimum off time <sup>(6)</sup>	$t_{OFF\_MIN}$	$V_{IN} = 5V$		80		ns
P-channel HS-FET peak current limit	$I_{LIMIT\_PEAK}$		4	5	6	A
N-channel LS-FET valley current limit	$I_{LIMIT\_VALLEY}$		1.5	3	4.5	A
Soft-start current	$I_{SS}$		1.5	3	4.5	$\mu A$
Maximum duty cycle				100		% $V_{FB}$
Power good (PG) UVLO rising threshold	$V_{PG\_UVLO\_RISING}$	FB rising edge	87	90	93	% $V_{FB}$
PG UVLO falling threshold	$V_{PG\_UVLO\_FALLING}$	FB falling edge	82	85	88	% $V_{FB}$
PG delay	$t_{DELAY\_PG}$	PG rising/falling edge		80		ms
PG sink current capability	$V_{PG\_LOW}$	1mA sink current			0.4	V
PG logic high voltage	$V_{PG\_HIGH}$	$V_{IN} = 5V$ , $V_{FB} = 0.6V$	4.9			V
Self-biased PG		$V_{IN} = 0V$ , $V_{EN} = 0V$ , PG is pulled up between 3V and 5.5V via a 100k $\Omega$ resistor			0.7	V
PG leakage current and logic high		5V logic high			100	nA
Enable (EN) start-up delay		EN on to activate SW		100		$\mu s$
EN shutdown delay		EN off to stop switching		30		$\mu s$
EN input logic low voltage			0.4	0.65		V

**ELECTRICAL CHARACTERISTICS (continued)**
 **$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN input logic high voltage				0.9	1.2	V
EN pull-down resistor				2		M $\Omega$
Output discharge resistor	R <sub>DISCHARGE</sub>	$V_{EN} = 0V$ , $V_{OUT} = 1.2V$		150		$\Omega$
EN input current		$V_{EN} = 2V$		1.2		$\mu A$
		$V_{EN} = 0V$		0		$\mu A$
Output over-voltage protection (OVP) rising threshold	$V_{OVP\_RISING}$		110	115	120	% $V_{FB}$
Output OVP hysteresis	$V_{OVP\_HYS}$			10		% $V_{FB}$
Output over-voltage delay				2		$\mu s$
Low-side MOSFET (LS-FET) current limit		Current flows from SW to GND		1.2		A
Absolute $V_{IN}$ over-voltage protection (OVP)		After $V_{OUT}$ OVP is enabled		6.1		V
Absolute $V_{IN}$ OVP hysteresis				160		mV
Thermal shutdown <sup>(6)</sup>				170		$^{\circ}C$
Thermal shutdown hysteresis <sup>(6)</sup>				20		$^{\circ}C$

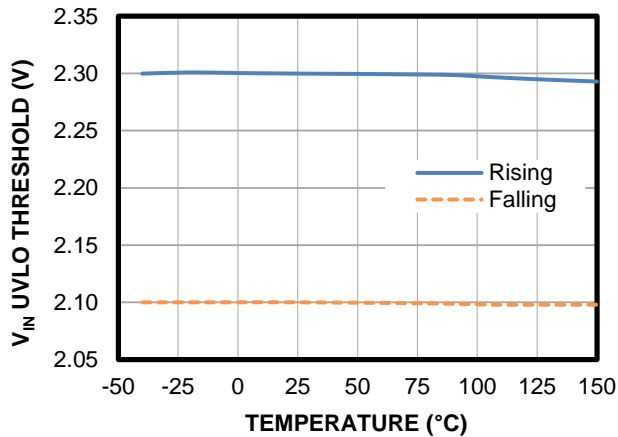
**Note:**

6) Guaranteed by design and bench characterization. Not tested in production.

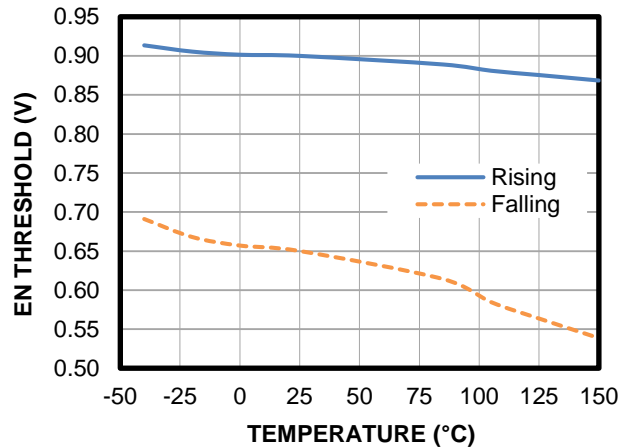
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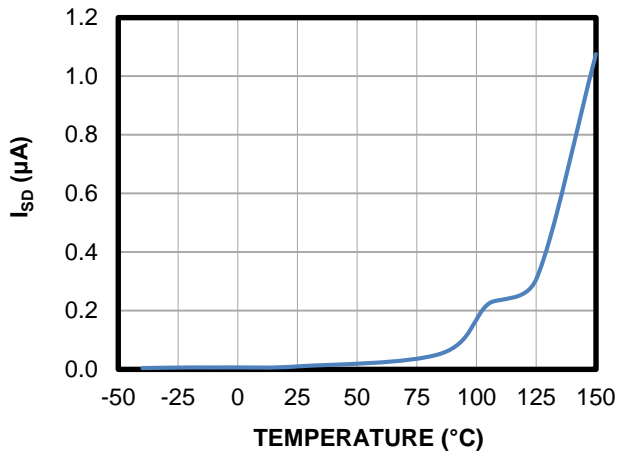
$V_{IN}$  UVLO Threshold vs. Temperature



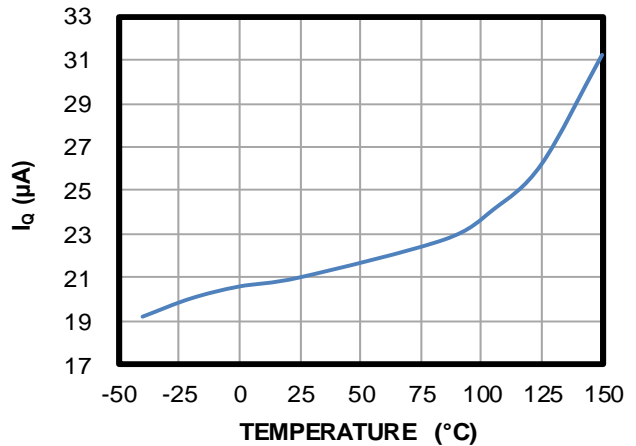
EN Threshold vs. Temperature



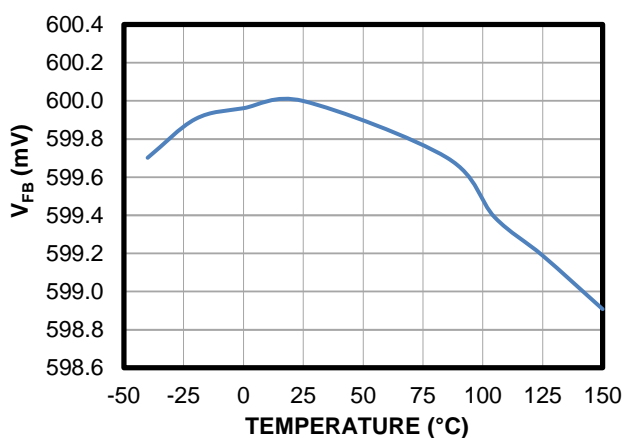
Shutdown Current vs. Temperature



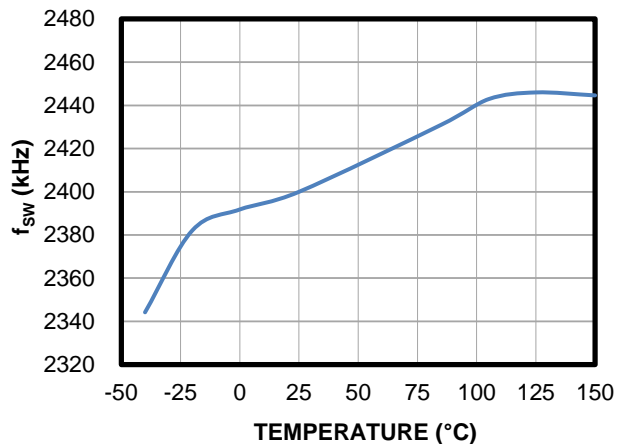
Quiescent Current vs. Temperature



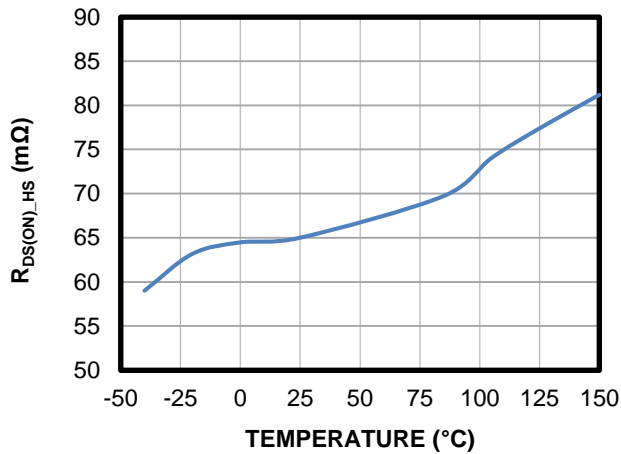
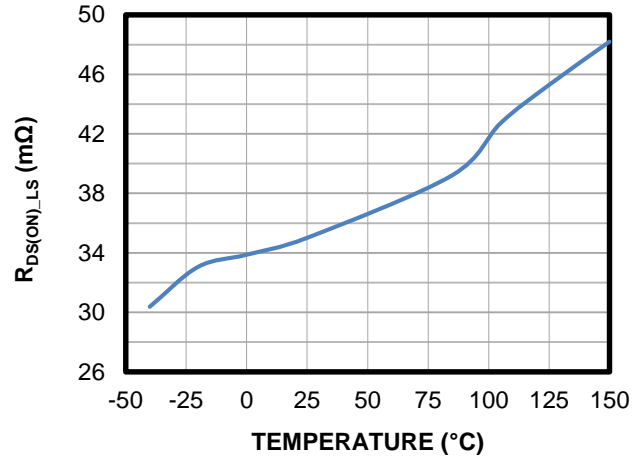
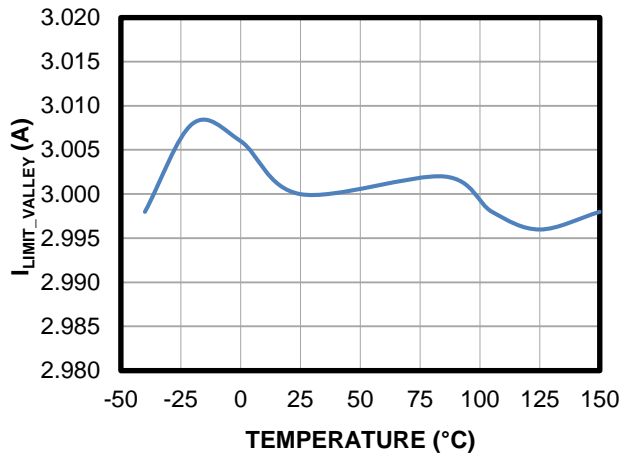
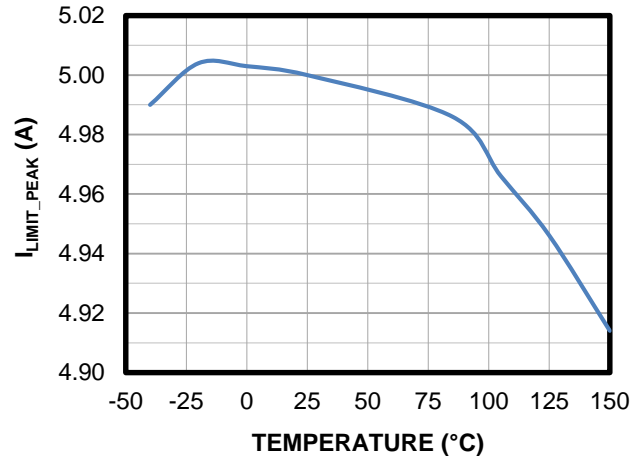
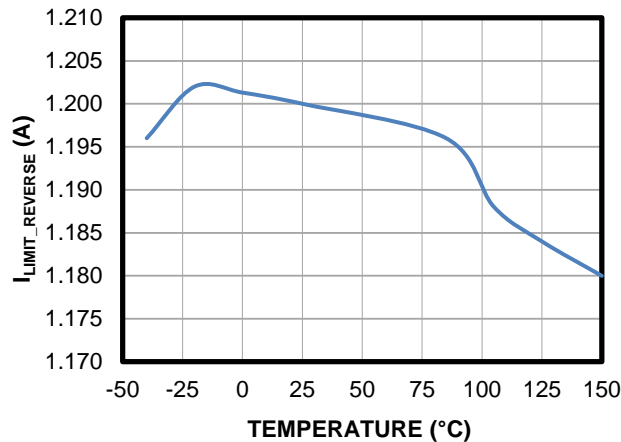
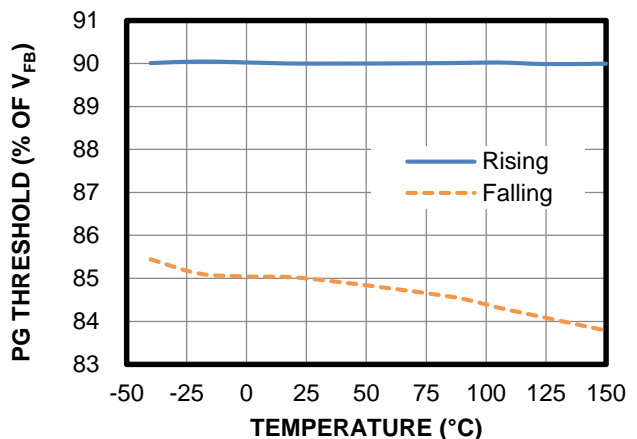
Feedback Voltage vs. Temperature



Switching Frequency vs. Temperature



**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

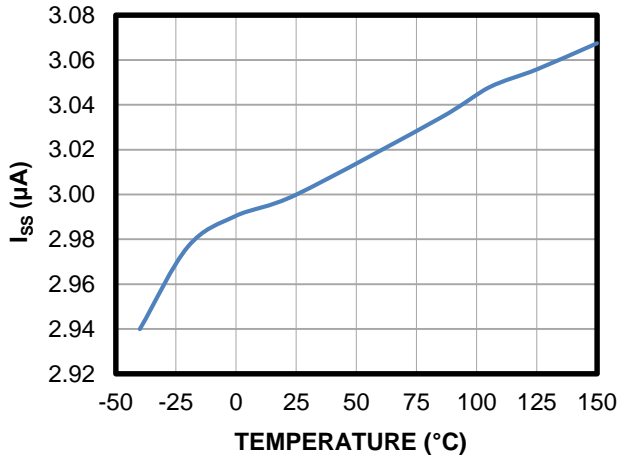
 **$R_{DS(ON)_HS}$  vs. Temperature**

 **$R_{DS(ON)_LS}$  vs. Temperature**

**LS-FET Valley Current Limit vs. Temperature**

**HS-FET Peak Current Limit vs. Temperature**

**LS-FET Reverse Current Limit vs. Temperature**

**PG Threshold vs. Temperature**




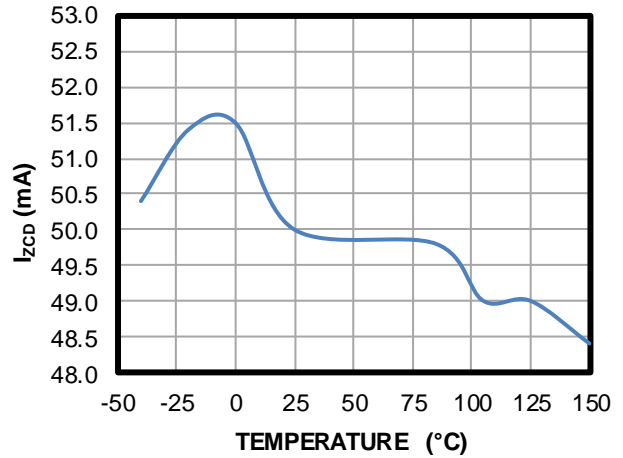
**TYPICAL CHARACTERISTICS (continued)**

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

**Soft-Start Current vs. Temperature**



**Zero-Current Detection vs. Temperature**

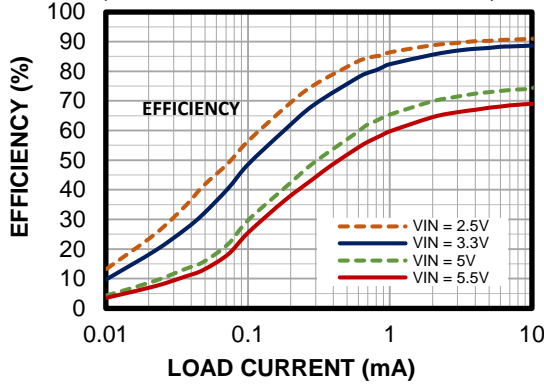


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

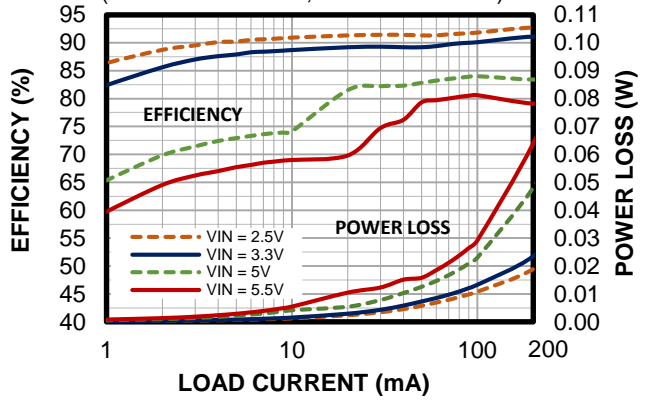
### Efficiency vs. Load Current

$V_{OUT} = 1.2V$ ,  $L = 1\mu H$   
(XEL4020-102MEB, DCR = 13.25m $\Omega$ )



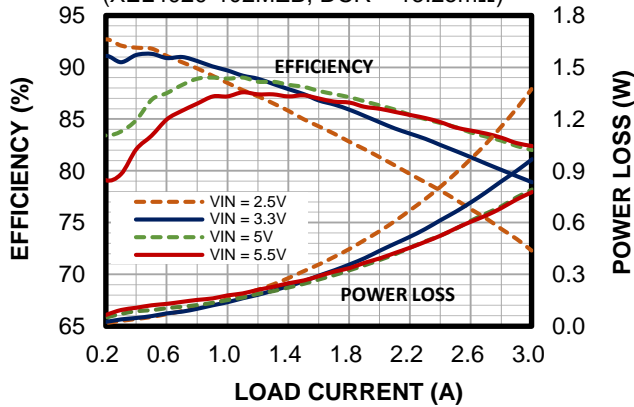
### Efficiency vs. Load Current vs. Power Loss

$V_{OUT} = 1.2V$ ,  $L = 1\mu H$   
(XEL4020-102MEB, DCR = 13.25m $\Omega$ )



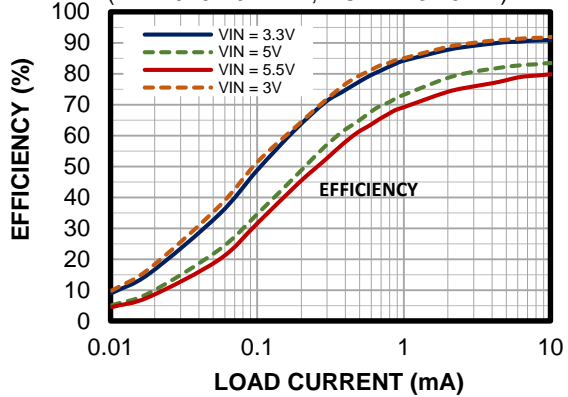
### Efficiency vs. Load Current vs. Power Loss

$V_{OUT} = 1.2V$ ,  $L = 1\mu H$   
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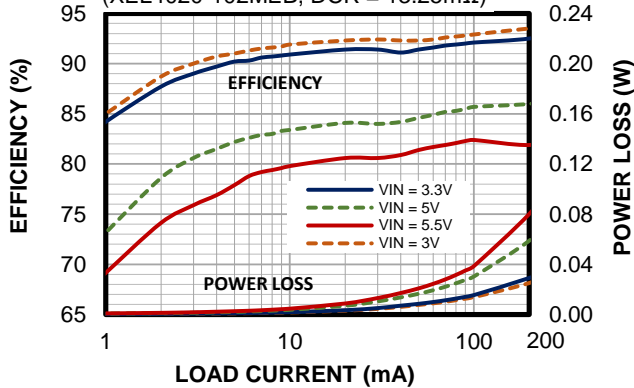
### Efficiency vs. Load Current

$V_{OUT} = 1.8V$ ,  $L = 1\mu H$   
(XEL4020-102MEB, DCR = 13.25m $\Omega$ )



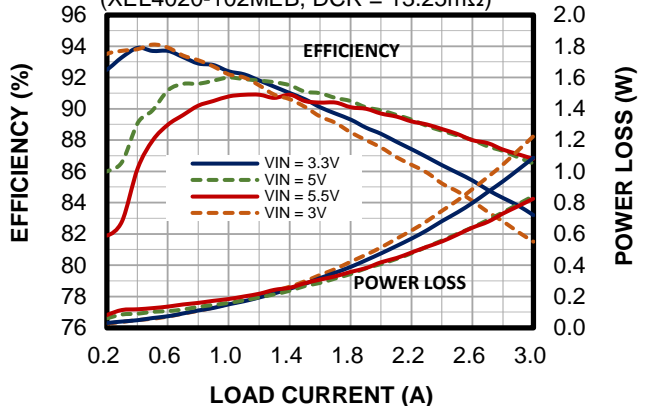
### Efficiency vs. Load Current vs. Power Loss

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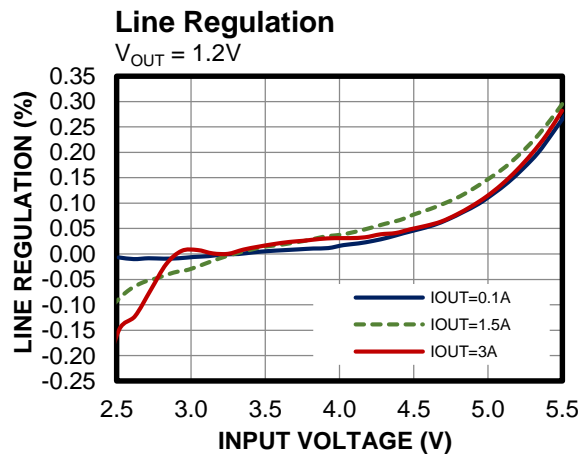
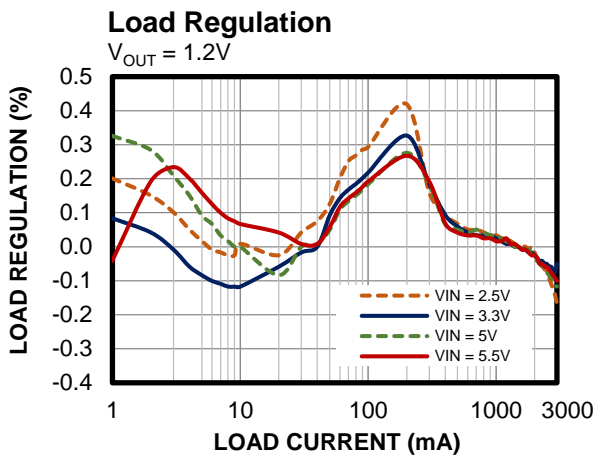
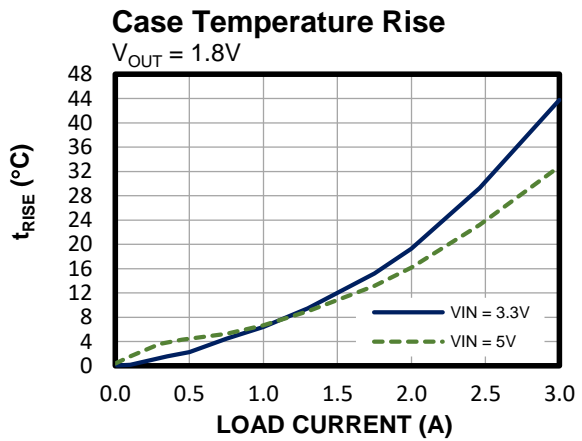
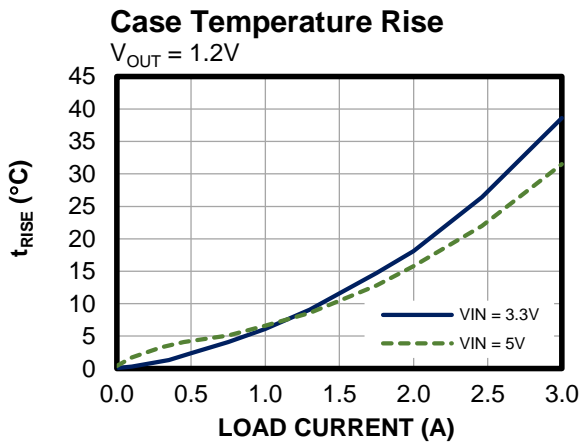
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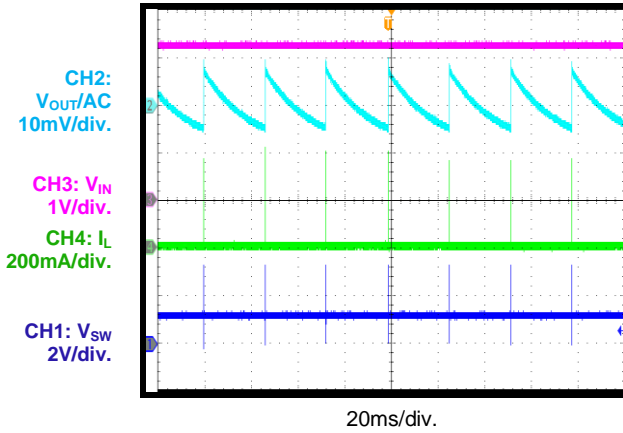
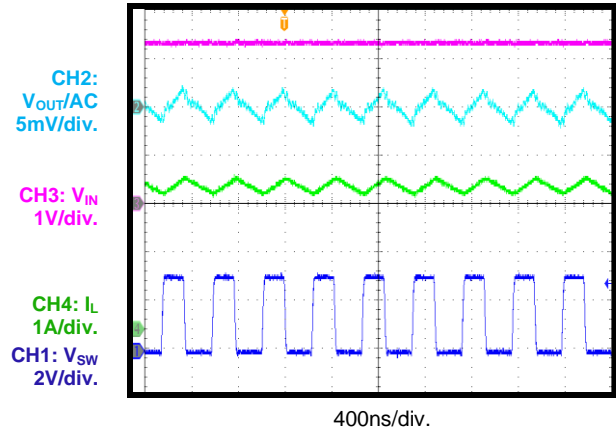
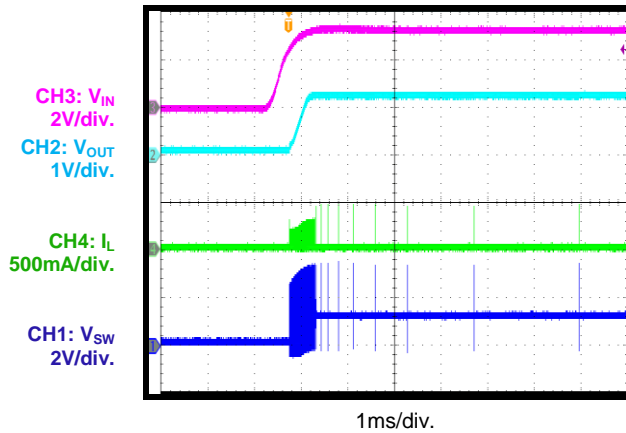
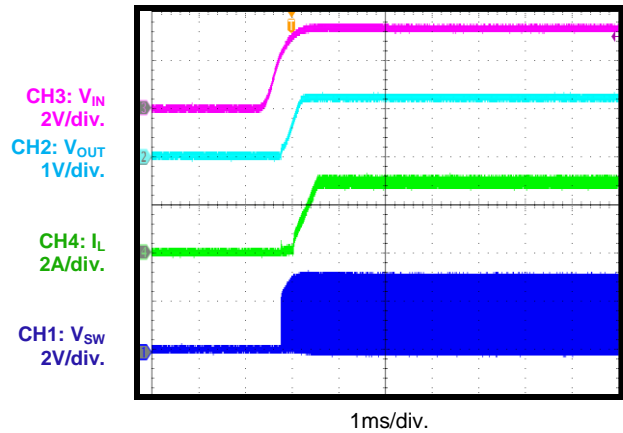
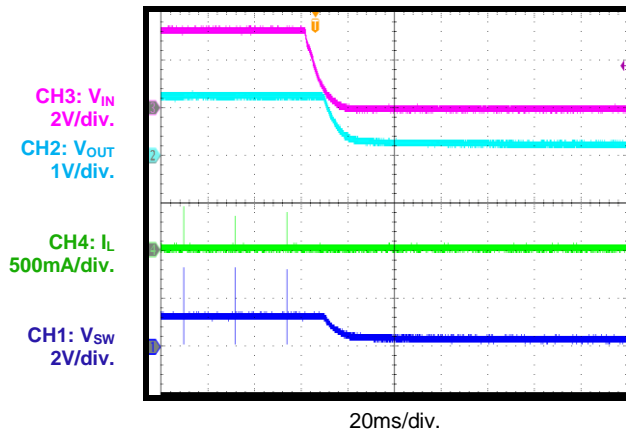
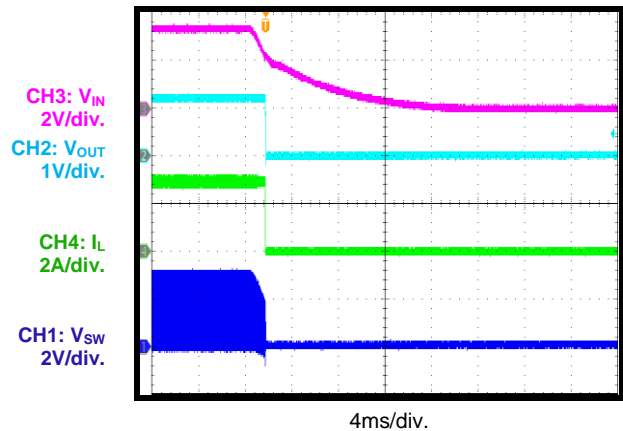


### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

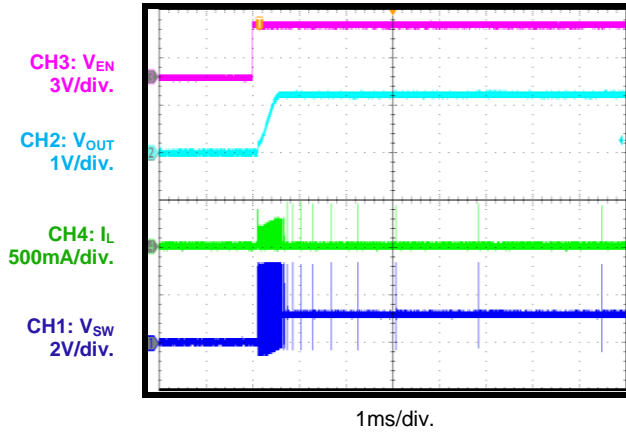
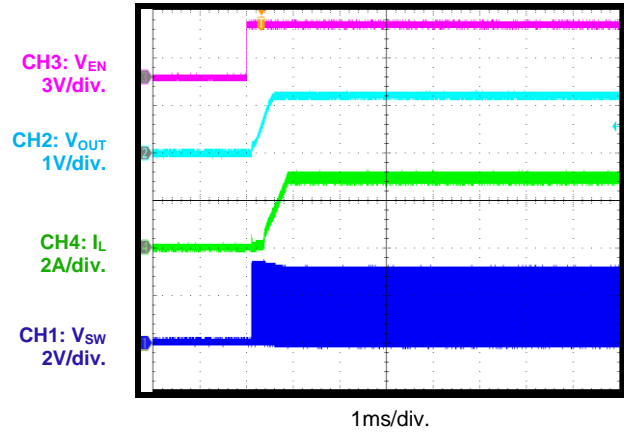
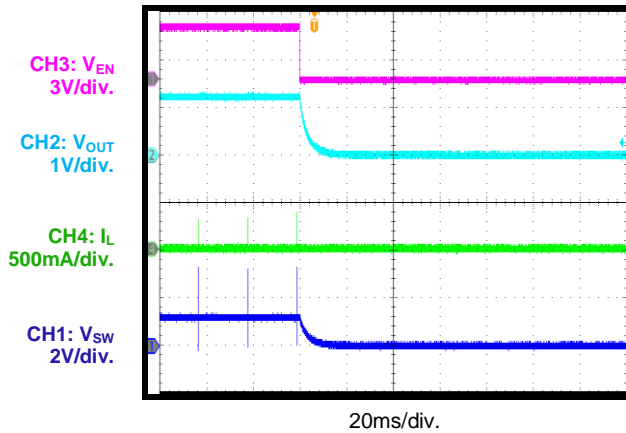
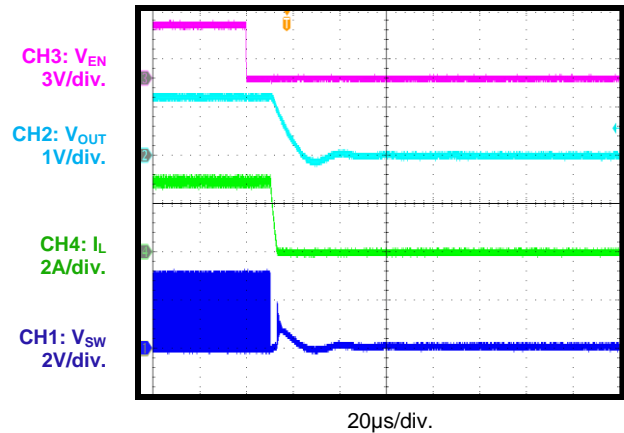
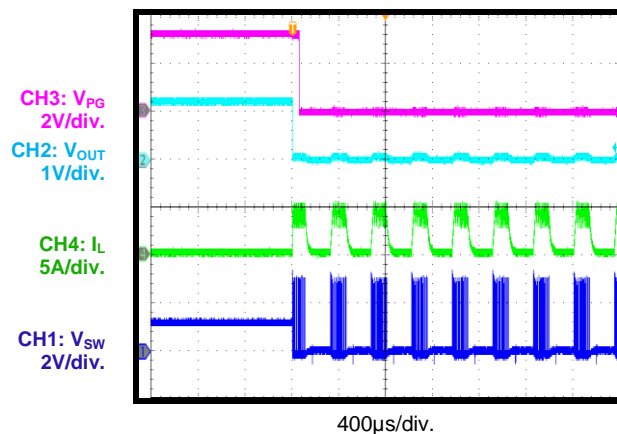
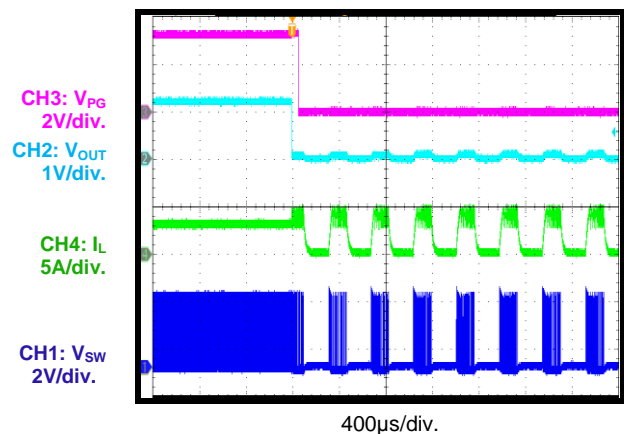
$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



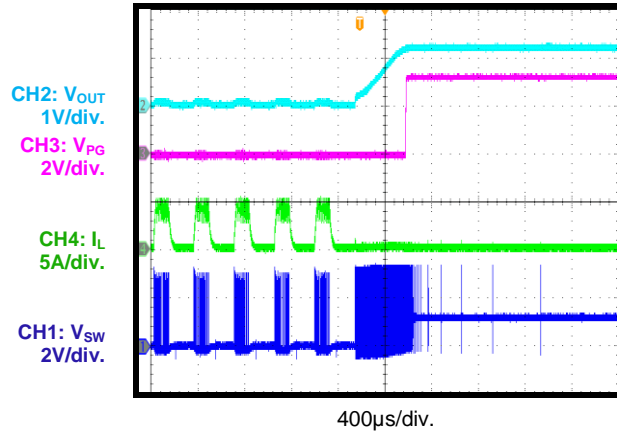
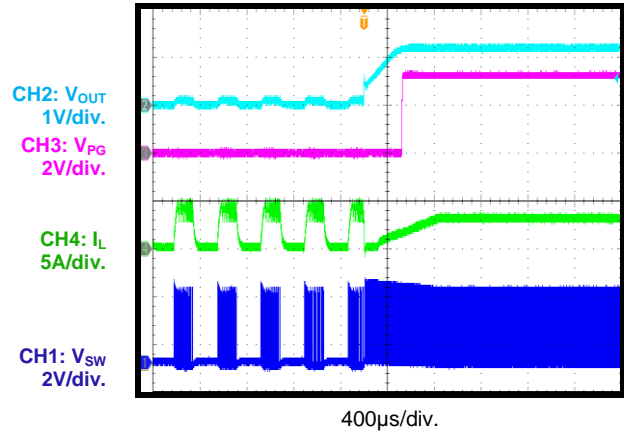
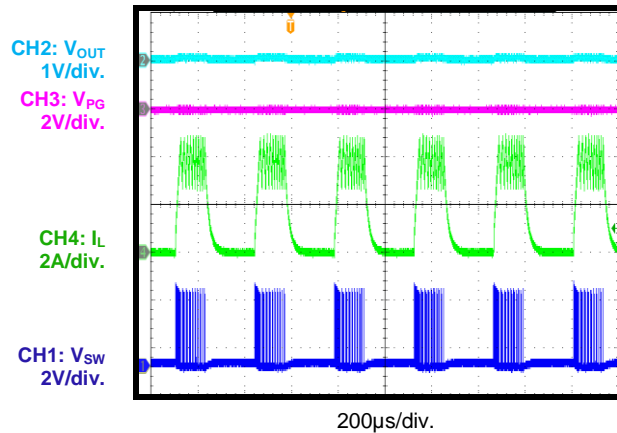
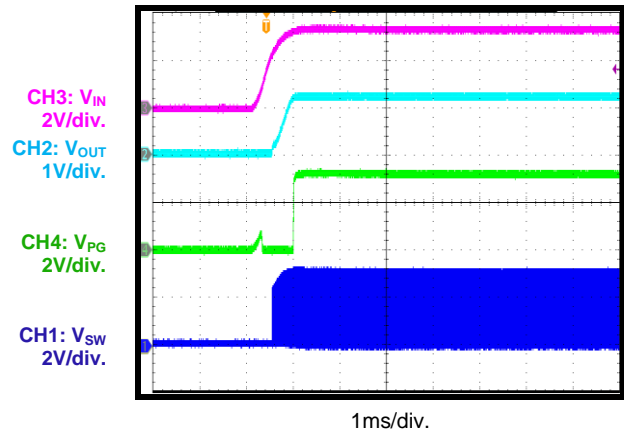
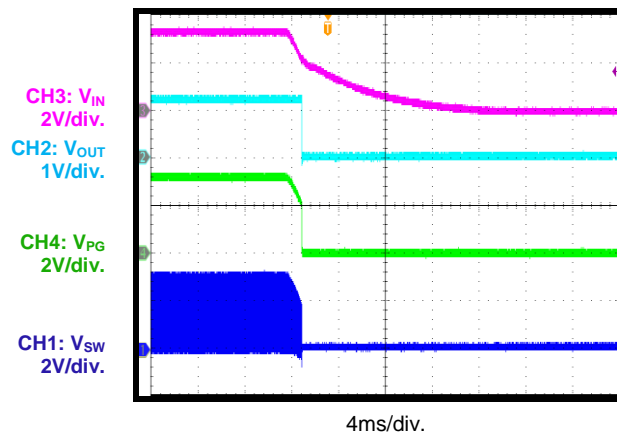
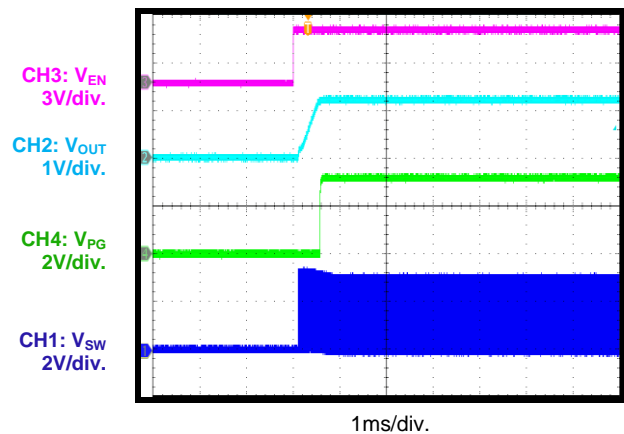
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Steady State**
 $I_{OUT} = 0A$ 

**Steady State**
 $I_{OUT} = 3A$ 

**Start-Up through VIN**
 $I_{OUT} = 0A$ 

**Start-Up through VIN**
 $I_{OUT} = 3A$ 

**Shutdown through VIN**
 $I_{OUT} = 0A$ 

**Shutdown through VIN**
 $I_{OUT} = 3A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

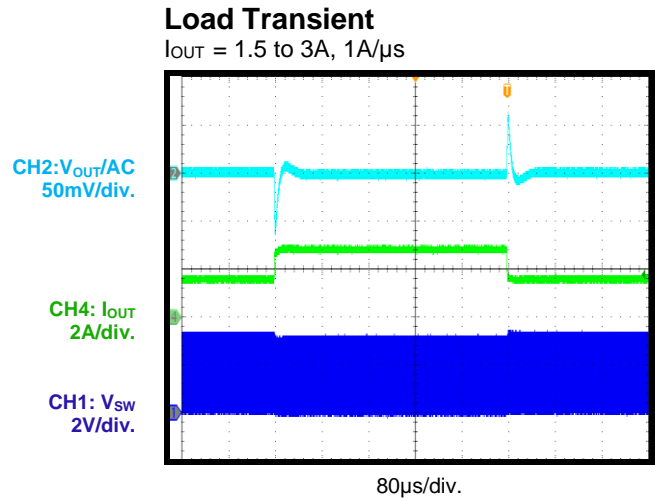
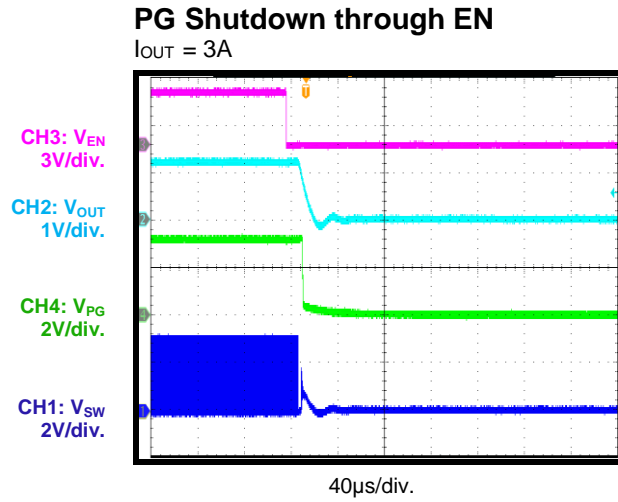
**Start-Up through EN**
 $I_{OUT} = 0A$ 

**Start-Up through EN**
 $I_{OUT} = 3A$ 

**Shutdown through EN**
 $I_{OUT} = 0A$ 

**Shutdown through EN**
 $I_{OUT} = 3A$ 

**SCP Entry**
 $I_{OUT} = 0A$ 

**SCP Entry**
 $I_{OUT} = 3A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**SCP Recovery**
 $I_{OUT} = 0A$ 

**SCP Recovery**
 $I_{OUT} = 3A$ 

**Short Circuit Protection**

**PG Start-Up through VIN**
 $I_{OUT} = 3A$ 

**PG Shutdown through VIN**
 $I_{OUT} = 3A$ 

**PG Start-Up through EN**
 $I_{OUT} = 3A$ 


### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1\mu H$ ,  $C2 = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



### FUNCTIONAL BLOCK DIAGRAM

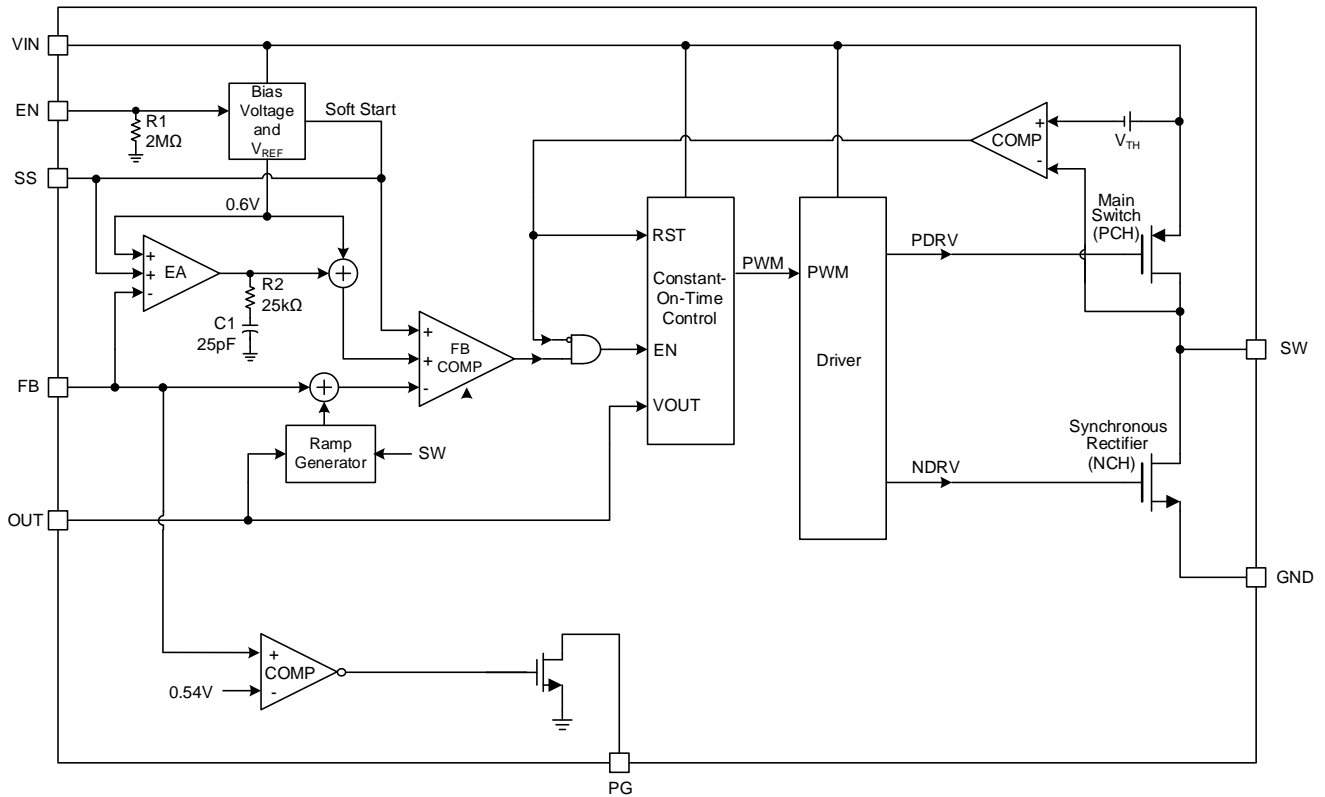


Figure 1: Functional Block Diagram



## OPERATION

The MPQ2179A employs input voltage ( $V_{IN}$ ) feed-forward and constant-on-time (COT) control to stabilize the switching frequency ( $f_{SW}$ ) across the entire  $V_{IN}$  range. It can achieve 3A of output current ( $I_{OUT}$ ) across a 2.5V to 5.5V  $V_{IN}$  range, with excellent load and line regulation. The output voltage ( $V_{OUT}$ ) can be regulated to as low as 0.6V. A 100% maximum duty cycle can be reached in low-dropout mode.

### Constant-On-Time (COT) Control

COT control provides a simpler control loop and faster transient response. The MPQ2179A's switching cycles have a fixed minimum off time ( $t_{OFF\_MIN}$ ) to prevent inductor current ( $I_L$ ) runaway during load transient. If the low-side MOSFET (LS-FET) turns on remains on for at least  $t_{MIN\_OFF}$  (typically 80ns). The high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage ( $V_{FB}$ ) drops below the reference voltage ( $V_{REF}$ ). This indicates an insufficient  $V_{OUT}$ . Input voltage feed-forward allows the device to maintain a nearly constant  $f_{SW}$  across the input range and load range. The  $f_{SW}$  on time ( $t_{ON}$ ) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

### Sleep Mode

The MPQ2179A employs sleep mode for high efficiency under light-load conditions. In sleep mode, most of the circuit block input currents ( $I_{IN}$ ) decrease, specifically the error amplifier (EA) and pulse-width modulation (PWM) comparator.

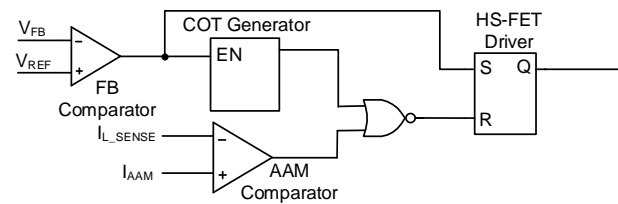
As the load becomes lighter, the converter's  $f_{SW}$  decreases. If the load continues to decrease and the off time ( $t_{OFF}$ ) exceeds  $3.5\mu s$ , then the MPQ2179A enters sleep mode. To further improve light-load efficiency, the converter consumes a very low quiescent current ( $I_Q$ ) while in sleep mode.

Once an HS-FET pulse occurs, the MPQ2179A exits sleep mode.

### Advanced Asynchronous Modulation (AAM) Mode under Light-Load Conditions

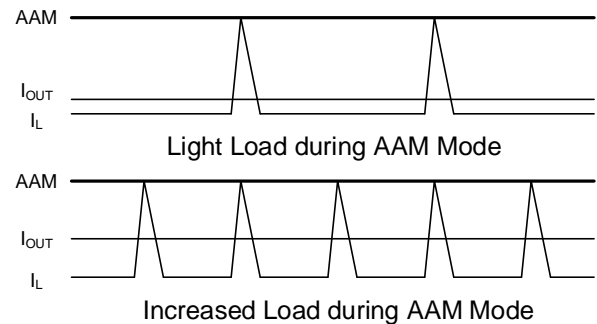
The device features advanced asynchronous modulation (AAM) mode and a zero-current detection (ZCD) circuit for light-load operation.

The AAM current ( $I_{AAM}$ ) is set internally. The SW pin's on time ( $t_{ON}$ ) is determined by the on-timer generator and AAM comparator. Under light-load conditions, SW's  $t_{ON}$  exceeds the AAM comparator's  $t_{ON}$ . Figure 2 shows the simplified AAM control logic.



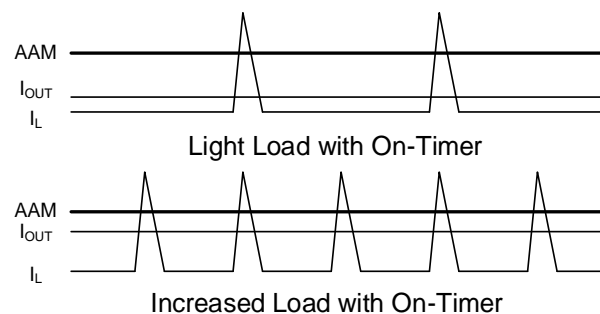
**Figure 2: Simplified AAM Control Logic**

If the AAM comparator's  $t_{ON}$  exceeds the on-timer's pulse, then the AAM comparator controls SW's  $t_{ON}$  (see Figure 3).



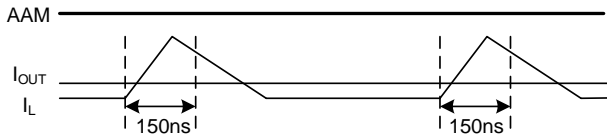
**Figure 3: AAM Comparator Controls SW's  $t_{ON}$**

When using a lower-value inductor, the AAM comparator's  $t_{ON}$  is below the on-timer, the operation mode is below in Figure 4. The HS-FET depends on the on-timer, therefore the on-timer controls  $t_{ON}$  (see Figure 4).



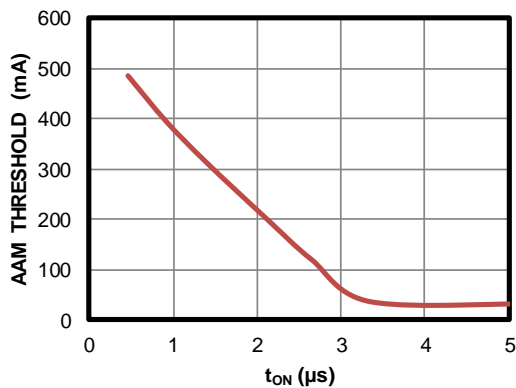
**Figure 4: On-Timer Controls SW's  $t_{ON}$**

Aside from the on-timer method, the AAM circuit has another AAM blanking time (150ns) for sleep mode. This means that if the on-timer drops below 150ns, then the HS-FET turns off after an on-timer pulse is generated without AAM control. In this scenario,  $I_L$  may not reach the AAM threshold (see Figure 5).



**Figure 5: AAM Blanking Time during Sleep Mode**

In sleep mode, the on-timer’s pulse is about 40% greater than its pulse during discontinuous conduction mode (DCM) and continuous conduction mode (CCM). Figure 6 shows how the AAM threshold decreases as  $t_{ON}$  increases gradually. For CCM,  $I_{OUT}$  must exceed half of the AAM threshold.



**Figure 6: AAM Threshold Decreases as  $t_{ON}$  Increases**

The MPQ2179A employs ZCD to determine whether  $I_L$  begins to reverse. If  $I_L$  reaches the ZCD threshold (typically 50mA), then the LS-FET turns off.

Even if  $V_{OUT}$  is close to  $V_{IN}$ , AAM mode and ZCD allow the device to operate continually in DCM under light-load conditions.

### Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the MPQ2179A on and off. Pull EN above 0.9V to turn the converter on; pull EN below 0.65V or float EN to turn it off. Pulling EN to GND also disables the device. There is an internal 2M $\Omega$  resistor connected between EN and GND.

### Output Discharge

If the MPQ2179A shuts down, the device initiates output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C2) between the OUT pin and GND. To block the output discharge path, add an external capacitor between  $V_{OUT}$  and the OUT pin (see the Output Discharge Blocking section on page 21).

### Soft Start (SS)

The MPQ2179A features external soft start (SS). To avoid overshoot during start-up, the SS pin ramps up  $V_{OUT}$  at a controlled slew rate. The SS pin’s charge current is typically 3 $\mu A$ . The soft-start time ( $t_{SS}$ ) is determined by the external soft-start capacitor ( $C_{SS}$ ).  $t_{SS}$  can be calculated with Equation (2):

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times 0.6\text{V}}{I_{SS}(\mu\text{A})} \quad (2)$$

Where  $I_{SS}$  is the internal soft-start charge current (3 $\mu A$ ).

It is recommended that  $C_{SS}$  be  $\geq 1\text{nF}$ .

The device has a pre-biased start-up function. Once EN is pulled above 0.9V, the converter starts up regardless of any pre-biased voltage on the output. Pre-biased start-up works even while the output discharge path is blocked.

### Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. If  $I_L$  reaches the HS-FET’s peak current limit ( $I_{LIMIT\_PEAK}$ ) threshold (typically 5A), the HS-FET turns off and the LS-FET turns on to discharge the energy. The HS-FET does not turn again until  $I_L$  drops below the valley current limit ( $I_{LIMIT\_VALLEY}$ ) threshold (typically 3A). This prevents current runaway during overload and short-circuit events.

### Short-Circuit Protection (SCP) and SCP Recovery

Short-circuit protection (SCP) protects the circuitries from over-current (OC) faults. If a  $V_{OUT}$  short to GND occurs and the device has exceeded its current limit, then SCP is triggered and the IC attempts to recover via hiccup mode. In hiccup mode, the output power stage is disabled and the SS voltage ( $V_{SS}$ ) is

discharged. Once  $V_{SS}$  is discharged completely, the device initiates a new SS. This process repeats until the fault condition is removed.

### **Over-Voltage Protection (OVP)**

The MPQ2179A monitors  $V_{FB}$  to detect over-voltage (OV) conditions. If  $V_{FB}$  exceeds 115% of  $V_{REF}$ , then the converter enters its dynamic regulation period. During this period, the LS-FET remains on until the LS-FET current reaches -1.2A. This process discharges  $V_{OUT}$  to keep it within its normal range. If the OV condition still remains after this process, there is a 1.5 $\mu$ s delay and then the LS-FET turns on again. Once  $V_{FB}$  falls below 105% of  $V_{REF}$ , the converter exits the regulation period. If the dynamic regulation period cannot prevent  $V_{OUT}$  from increasing and a 6.1V  $V_{IN}$  is detected, then over-voltage protection (OVP) is triggered. The device stops switching until  $V_{IN}$  drops below 6V. Once  $V_{IN}$  drops below 6V, the MPQ2179A resumes normal operation.

### **Power Good (PG) Indicator**

The MPQ2179A has a power good (PG) output to indicate whether the converter is operating normally after start-up. PG is the open drain of an internal MOSFET. It is recommended that this MOSFET's maximum  $R_{DS(ON)}$  be below 400 $\Omega$ . PG can be connected to  $V_{IN}$  or an external voltage source via an external resistor (10k $\Omega$  to 100k $\Omega$ ). Once  $V_{IN}$  is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. After  $V_{FB}$  reaches 90% of  $V_{REF}$ , PG is pulled high by the external voltage source. If  $V_{FB}$  drops to 85% of  $V_{REF}$ , then the PG voltage ( $V_{PG}$ ) is pulled to GND to indicate an output failure.

If  $V_{IN}$  and EN are not available, and PG is pulled up via an external power supply, then PG self-biases and asserts. If a 100k $\Omega$  pull-up resistor is being used, then  $V_{PG}$  should be below 0.7V.

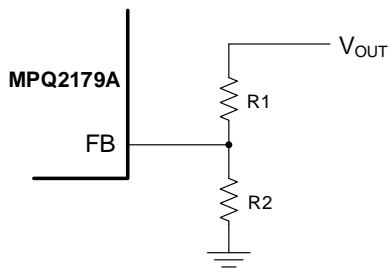
## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the MPQ2179A's adjustable output voltage ( $V_{OUT}$ ). Select a feedback (FB) resistor ( $R1$ ) to reduce the  $V_{OUT}$  leakage current (typically between 10k $\Omega$  and 100k $\Omega$ ). Then  $R2$  can then be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 7 shows the FB network.



**Figure 7: Feedback Network**

Table 1 shows the recommended resistor values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

$V_{OUT}$ (V)	$R1$ (k $\Omega$ )	$R2$ (k $\Omega$ )
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

### Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage decreases as the on time ( $t_{ON}$ ) increases and the duty cycle is extended. If the minimum off time ( $t_{OFF\_MIN}$ ) is reached at a low input voltage and under heavy-load conditions, then  $f_{SW}$  scales down. To maintain a constant  $f_{SW}$  during heavy-load operation, a larger  $V_{OUT}$  is required for a larger  $V_{IN}$ . For a 1.8V  $V_{OUT}$  at a 2A load,  $V_{IN}$  should be above 2.9V to keep  $f_{SW}$  above 2MHz. If the frequency begins to scale down,  $V_{IN}$  can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)\_HS} \times I_{OUT}}{1 - \frac{t_{OFF\_MIN}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum  $t_{OFF\_MIN}$  is 125ns. <sup>(7)</sup>

**Note:**

7) Guaranteed by design and bench characterization. Not tested in production.

### Selecting the Inductor

A 0.47 $\mu$ H to 1.5 $\mu$ H inductor is recommended for most applications. For high efficiency, select an inductor with a DC resistance below 25m $\Omega$ .

High-frequency, switch-mode power supplies with magnetic devices (such as the MPQ2179A) can have strong electromagnetic interference (EMI). It is recommended to avoid using unshielded power inductors, as they provide poor magnetic shielding. Shielded inductors (e.g. metal alloy or multi-layer chip power inductors) are highly recommended for their effective EMI reduction.

For most designs, the inductance ( $L_1$ ) can be estimated with Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where  $\Delta I_L$  is the inductor ripple current.

Choose an inductor with a ripple current rating that is approximately 30% of the maximum load current ( $I_{LOAD}$ ). The maximum inductor peak current ( $I_{L\_MAX}$ ) can be calculated with Equation (6):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current ( $I_{IN}$ ), and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. For most applications, a 10 $\mu$ F capacitor is sufficient. Higher output voltages

may require a 22μF capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating to absorb the switching  $I_{IN}$ .

C1's RMS current rating ( $I_{C1}$ ) can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case scenario occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C1 can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic or tantalum capacitors, place a small, high-quality, 0.1μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple ( $\Delta V_{IN}$ ) can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC  $V_{OUT}$ . It is recommended to use ceramic capacitors for C2. Low-ESR capacitors are recommended, as they effectively limit the output voltage ripple ( $\Delta V_{OUT}$ ).  $\Delta V_{OUT}$  can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (10)$$

Where  $L_1$  is the inductance, and  $R_{ESR}$  is C2's equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of  $\Delta V_{OUT}$ .

For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

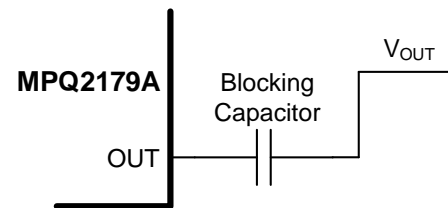
For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

C2's characteristics can also affect the stability of the regulation system.

### Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT pin and GND is enabled to discharge C2. The discharge path can be blocked by adding an external capacitor between  $V_{OUT}$  and the OUT pin (see Figure 8).



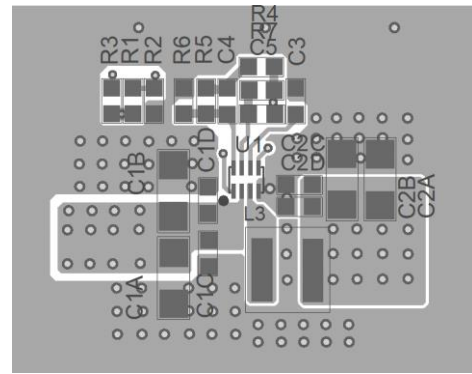
**Figure 8: Circuit with  $V_{OUT}$  Discharge Blocking**

To avoid influencing the loop and load transient, select a  $\geq 10\text{nF}$  blocking capacitor. It is recommended to use a 10nF to 100nF blocking capacitor. A larger-value blocking capacitor does not have an impact on loop performance, but a larger-value capacitor is physically larger and is typically unnecessary for the best results.

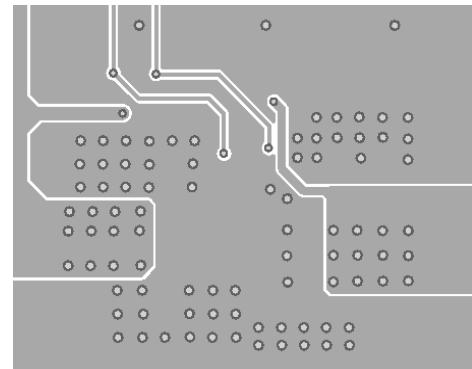
### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout design can result in poor line regulation, load regulation, and stability issues. For the best results, refer to Figure 9 and follow the guidelines below:

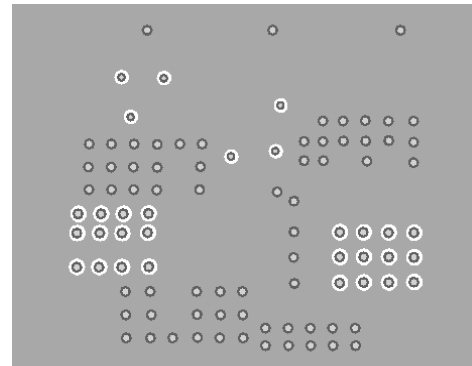
1. Place the high-current paths (GND, VIN, and SW) close to the IC with short, direct, and wide traces.
2. Place the input capacitor (C1) as close to the VIN and GND pins as possible.
3. Place the output capacitor (C2) close to the GND pin.
4. For the adjustable output version, place the external feedback resistors close to the FB pin.
5. Keep the switching node (SW) short and away from the feedback network.
6. Keep the  $V_{OUT\_SENSE}$  line (OUT) as short as possible, and place it as far away from the inductor as possible. OUT should not surround the inductor or be close to SW.



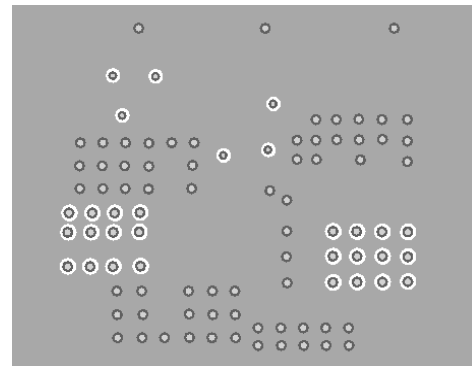
**Top Layer**



**Mid-Layer 2**



**Mid-Layer 1**



**Bottom Layer**

**Figure 9: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

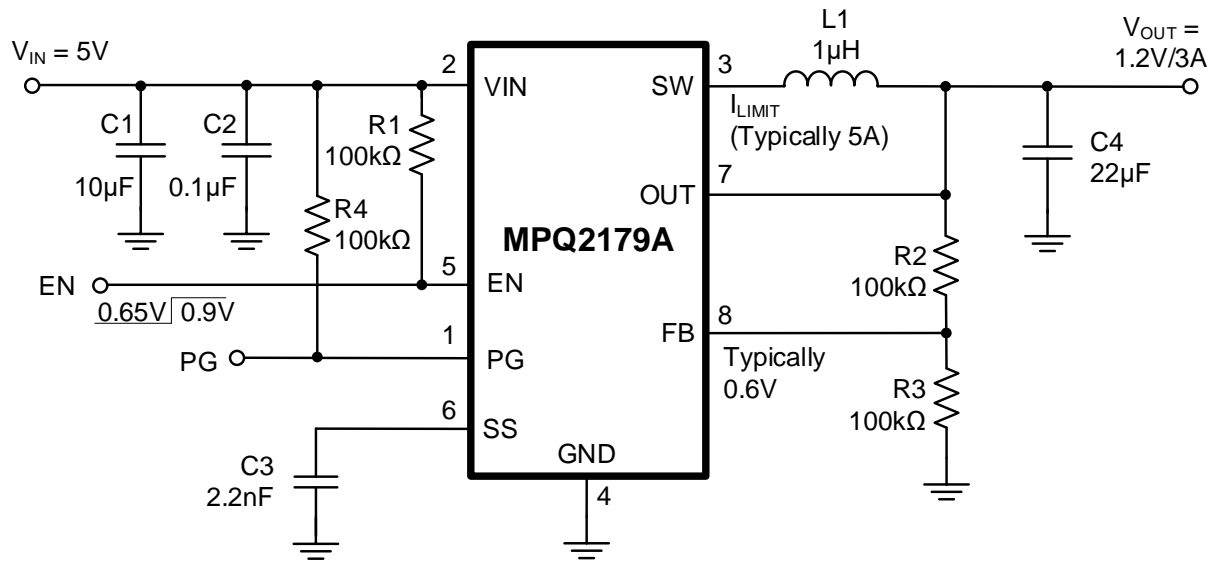


Figure 10: Typical Application Circuit (1.2V Output)

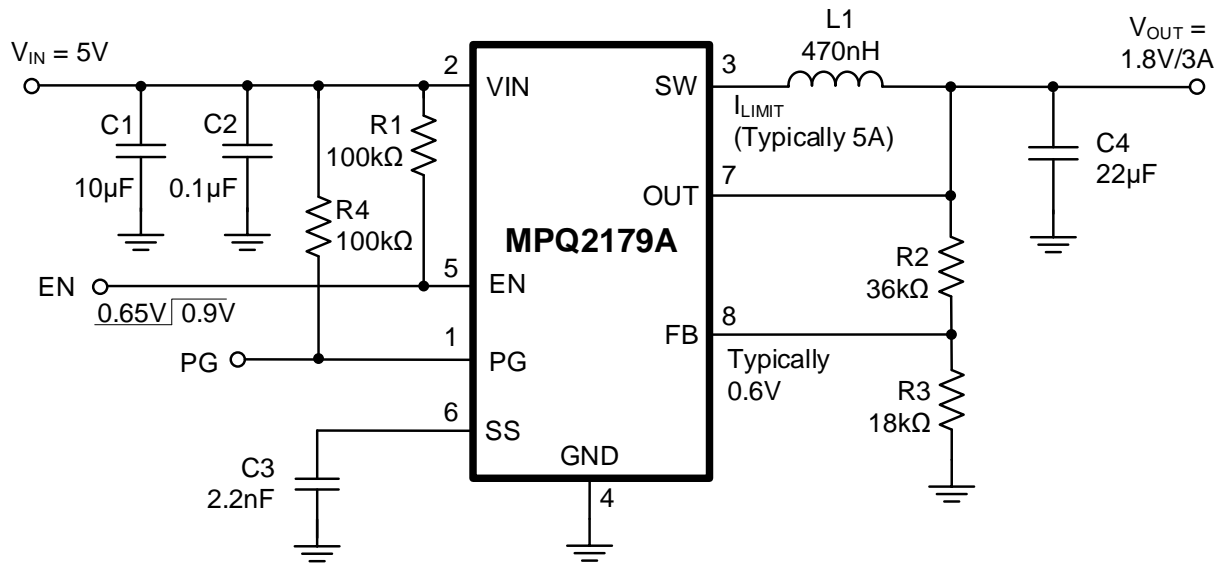
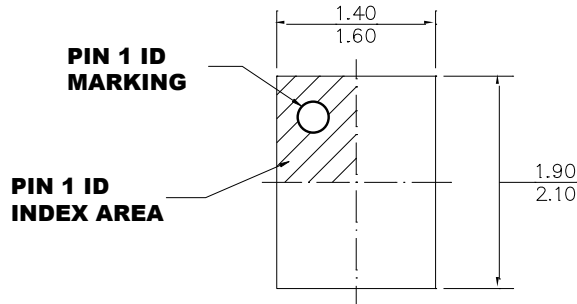


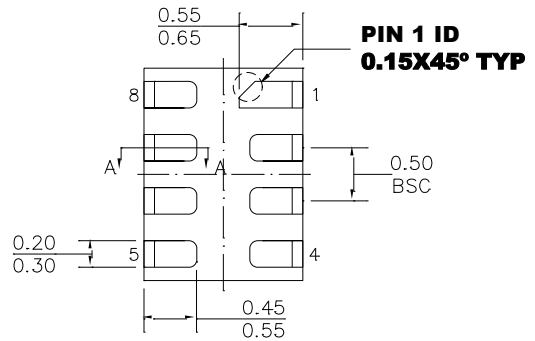
Figure 11: Typical Application Circuit (1.8V Output)

# PACKAGE INFORMATION

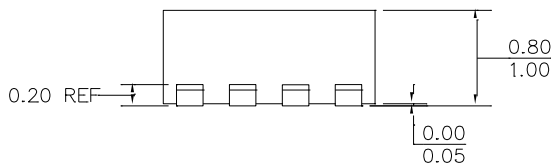
## QFN-8 (1.5mmx2mm) Wettable Flank



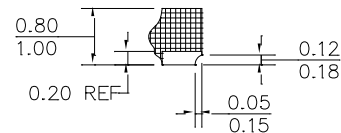
**TOP VIEW**



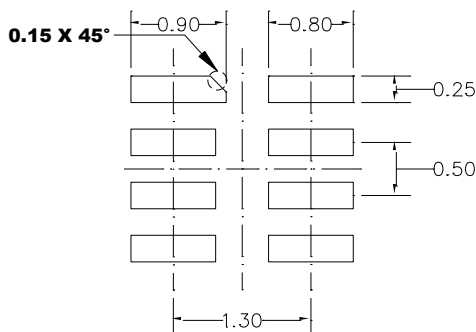
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

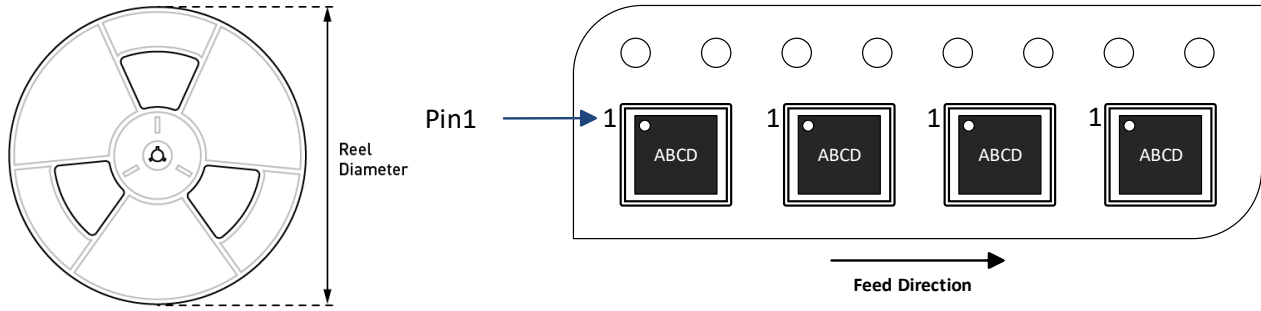


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



**CARRIER INFORMATION**


Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2179AGQHE-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	8mm	4mm



## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/06/2021	Initial Release	-

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