

# CLL3H0914L-700; CLL3H0914LS-700

L-band internally pre-matched GaN-SiC HEMT **AMPLEON**

Rev. 1 — 15 July 2022

Product data sheet

## 1. Product profile

### 1.1 General description

The CLL3H0914L-700 and CLL3H0914LS-700 are 700 W internally pre-matched RF GaN-SiC HEMTs power transistors that are usable in the frequency range from 0.9 GHz to 1.4 GHz. The devices offer excellent efficiency, thermal resistance and ruggedness suitable for short- and long-pulse applications. Further, [Section 8.3](#) highlights performance curves for application reference designs at frequencies from 1.2 GHz to 1.4 GHz, 1030 MHz and 960 MHz to 1215 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 3\text{ ms}$ ;  $\delta = 10\%$ ;  $V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 200\text{ mA}$ ; frequencies from 1200 MHz to 1400 MHz, tested on a straight lead device soldered in a class-AB demo circuit.

Test signal	f	P <sub>L</sub> [1]	G <sub>p</sub>	η <sub>D</sub>	RL <sub>in</sub>
	(MHz)	(W)	(dB)	(%)	(dB)
pulsed CW	1200	850	16.0	62	-12
	1300	750	16.0	71	-16
	1400	750	16.0	68	-15

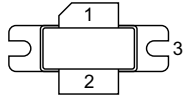
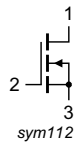
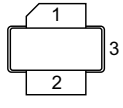
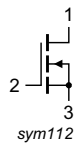
[1]  $P_L = P_{L(sat)}$ .

### 1.2 Features and benefits

- 700 W internally pre-matched GaN-SiC HEMT covering a frequency range from 0.9 GHz to 1.4 GHz with internal stability network
- Low thermal resistance
- Excellent ruggedness
- High efficiency, short pulse reference designs at 960 MHz to 1215 MHz and 1030 MHz for avionics applications
- High efficiency, long pulse reference designs at 1.2 GHz to 1.4 GHz
- Typical performance features of all three reference designs summarized in [Section 8.3](#)
- For RoHS compliance see the product details on the Ampleon website

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>CLL3H0914L-700 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		
<b>CLL3H0914LS-700 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT502A	CLL3H0914L-700U	9349 603 40112	Tray; 20-fold; non-dry pack	20
SOT502B	CLL3H0914LS-700U	9349 603 39112	Tray; 20-fold; non-dry pack	20

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	150	V
$V_{GS}$	gate-source voltage		-8	+2	V
$I_{GF}$	forward gate current		-	36	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{ch}$	active die channel temperature	<sup>[1]</sup>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(ch-c)}$ [1]	transient thermal impedance from active die channel to case	$T_{case} = 85\text{ °C}; V_{DS} = 50\text{ V}; P_{dis} = 360\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.20	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.23	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.25	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.23	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.29	K/W
		$t_p = 1\text{ ms}; \delta = 10\text{ }\%$	0.31	K/W
		$t_p = 3\text{ ms}; \delta = 10\text{ }\%$	0.39	K/W
	steady state	0.48	K/W	

[1] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

## 6. Characteristics

**Table 6. DC characteristics**

$T_{case} = 25\text{ °C};$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = -8\text{ V}; I_D = 16\text{ mA}$	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 6\text{ V}; I_D = 1080\text{ mA}$	-	-2.9	-	V
$I_{DSX}$	drain cut-off current	$V_{GS} = 2\text{ V}; V_{DS} = 6\text{ V}$	-	75	-	A
$g_{fs}$	forward transconductance	$V_{GS} = 0\text{ V}; V_{DS} = 6\text{ V}$	-	19	-	S
$R_{Dson}$	drain-source on-state resistance	$V_{GS} = 0\text{ V}; V_{DS} = 100\text{ mV}$	-	35	-	m $\Omega$

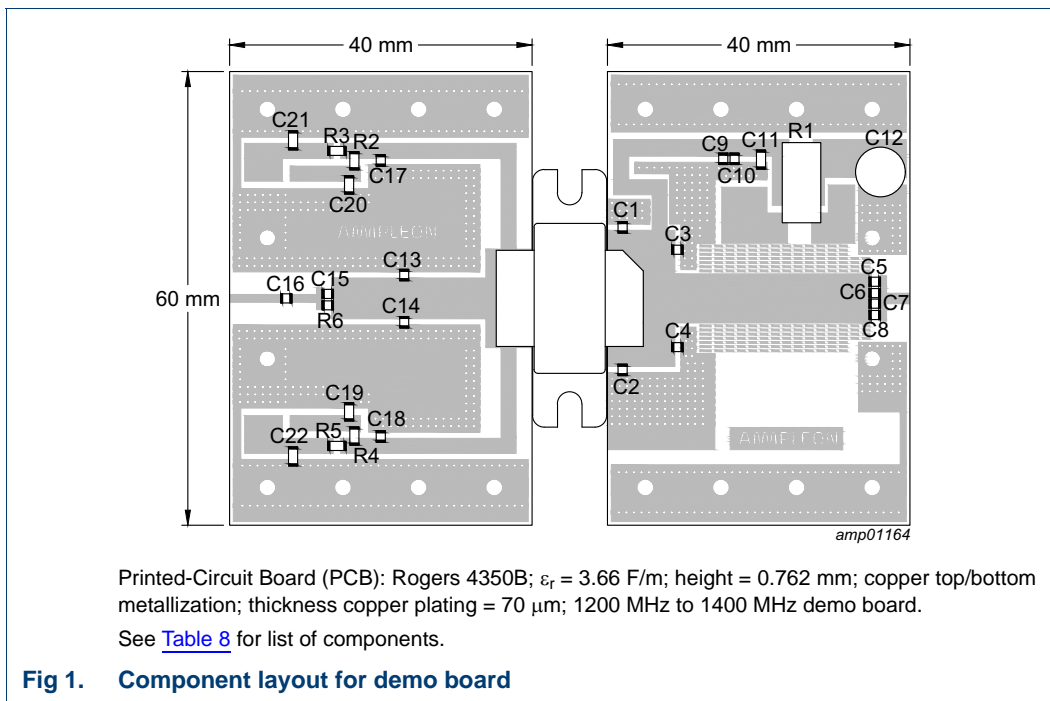
**Table 7. RF characteristics**

Test signal: pulsed RF;  $t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 50\text{ V}; I_{Dq} = 500\text{ mA}; T_{case} = 25\text{ °C};$  unless otherwise specified, in a class-AB production circuit, tested at frequencies from 1200 MHz to 1400 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_L$	output power	$P_{L(3dB)}$	725	800	-	W
$G_p$	power gain	$P_L = 725\text{ W}$	15	17	-	dB
$\eta_D$	drain efficiency	$P_L = 725\text{ W}$	58	65	-	%
$RL_{in}$	input return loss	$P_L = 725\text{ W}$	-	-10	-	dB
$P_{droop(pulse)}$	pulse droop power	$P_L = 725\text{ W}$	-	0.1	-	dB

## 7. Application information

### 7.1 Circuit information



**Table 8. List of components**

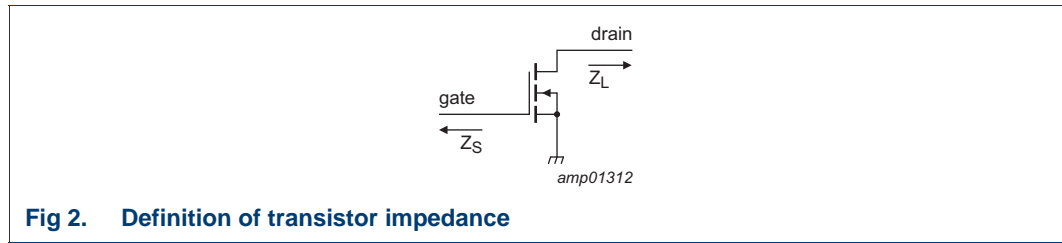
For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	9.1 pF	ATC 100A
C3, C4	multilayer ceramic chip capacitor	5.1 pF	ATC 100A
C5, C6, C7, C8, C9, C10, C16	multilayer ceramic chip capacitor	100 pF	ATC 100A
C11	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	Murata: GRM42256X7S475K100H530
C12	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
C13, C14	multilayer ceramic chip capacitor	1.2 pF	ATC 100A
C15	multilayer ceramic chip capacitor	24 pF	ATC 100A
C17, C18	multilayer ceramic chip capacitor	72 pF	ATC 100A
C19, C20	multilayer ceramic chip capacitor	10 nF, 50 V	Murata: C1206C104K1RAC
C21, C22	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$	TDK
R1	shunt resistor	10 m $\Omega$ , 5 W	
R2, R3	resistor	8.2 $\Omega$	SMD 1206
R4, R5	resistor	4.7 $\Omega$	SMD 1206
R6	shunt resistor	82 $\Omega$	SMD 0603

## 7.2 Impedance information

**Table 9. Typical impedance**  
*Typical values unless otherwise specified.*

f (MHz)	Z <sub>S</sub> (Ω)	Z <sub>L</sub> (Ω)
960	1.419 – j2.007	0.935 – j0.770
1030	1.526 – j2.099	1.053 – j0.613
1090	1.611 – j2.163	1.094 – j0.583
1150	1.638 – j2.186	1.015 – j0.588
1215	1.540 – j2.153	0.813 – j0.518
1200	1.090 – j2.359	1.337 – j0.707
1300	1.842 – j1.747	1.167 – j0.711
1400	2.215 – j1.272	0.722 – j0.604



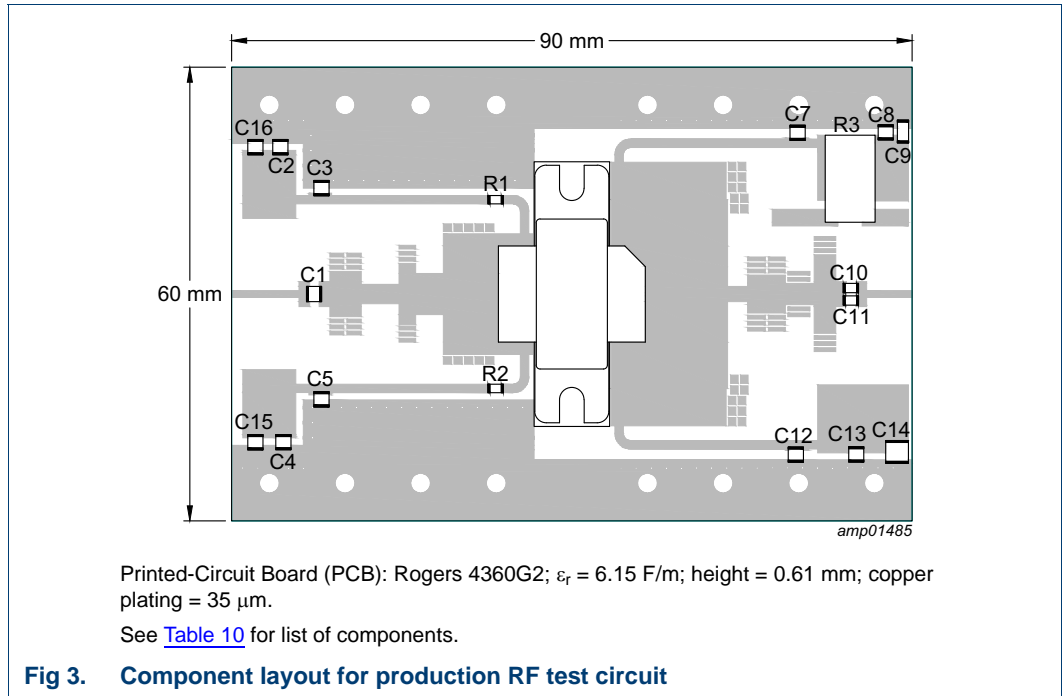
**Fig 2. Definition of transistor impedance**

## 8. Test information

### 8.1 Ruggedness in class-AB operation

The CLL3H0914L-700 and CLL3H0914LS-700 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 50$  V;  $f = 1300$  MHz at rated load power on RF development board using a pulsed CW RF signal.

8.2 Test circuit information



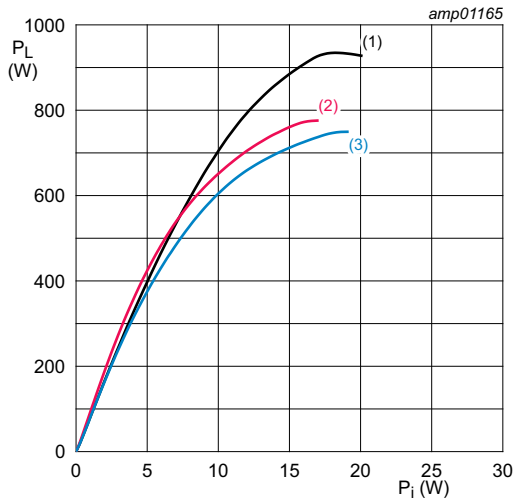
**Table 10. List of components**

For test circuit see [Figure 3](#).

Component	Description	Value	Remarks
C1, C3, C5, C7, C12	multilayer ceramic chip capacitor	430 pF	ATC 800A
C10, C11	multilayer ceramic chip capacitor	160 pF	ATC 800A
C2, C4, C8, C13	multilayer ceramic chip capacitor	1 nF	ATC 800A
C9, C14, C15, C16	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	GMR42 258K7S 475K 100 H53
R1, R2	resistor	5.6 $\Omega$	SMD 0603
R3	resistor	10 m $\Omega$	FC4L110R010FER

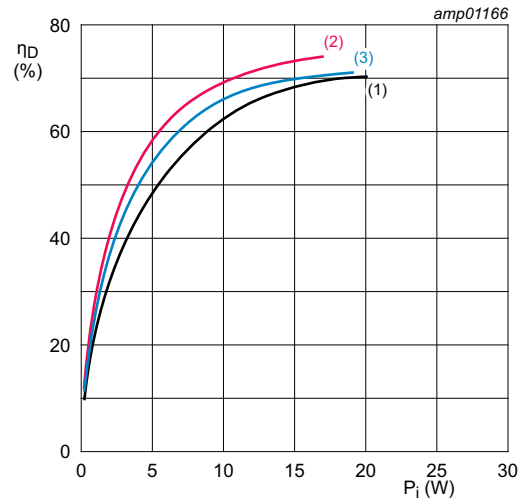
8.3 Graphical data

8.3.1 1200 MHz to 1400 MHz demo board



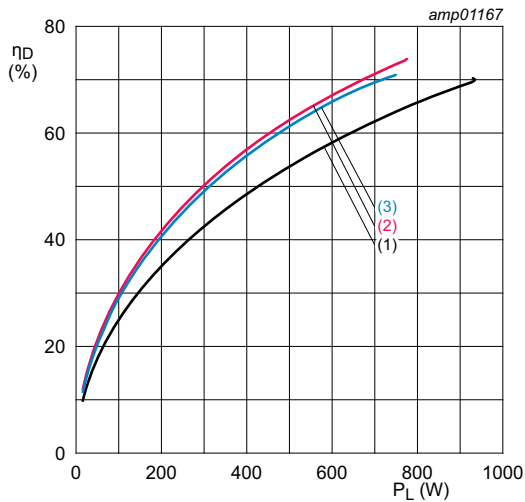
$V_{DS} = 50\text{ V}; I_{DQ} = 500\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 4. Output power as a function of input power; typical values**



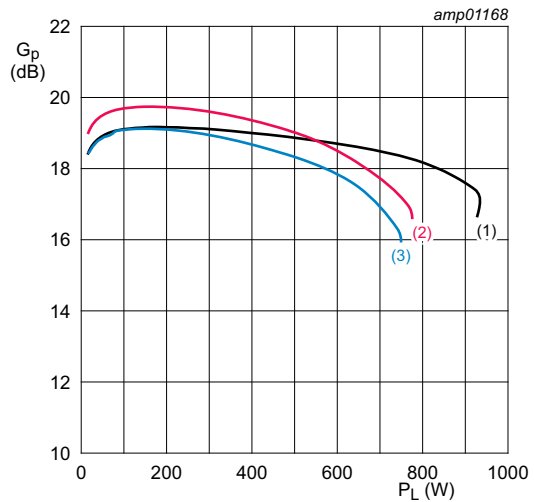
$V_{DS} = 50\text{ V}; I_{DQ} = 500\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 5. Drain efficiency as a function of input power; typical values**



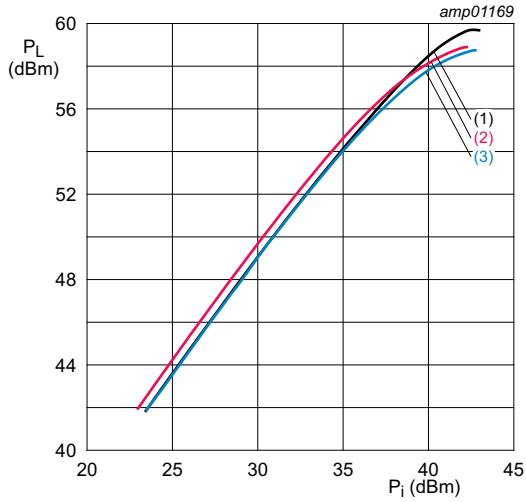
$V_{DS} = 50\text{ V}; I_{DQ} = 500\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 6. Drain efficiency as a function of output power; typical values**



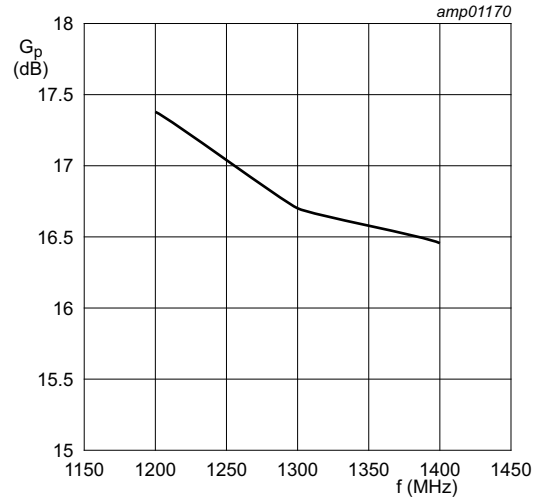
$V_{DS} = 50\text{ V}; I_{DQ} = 500\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 7. Power gain as a function of output power; typical values**



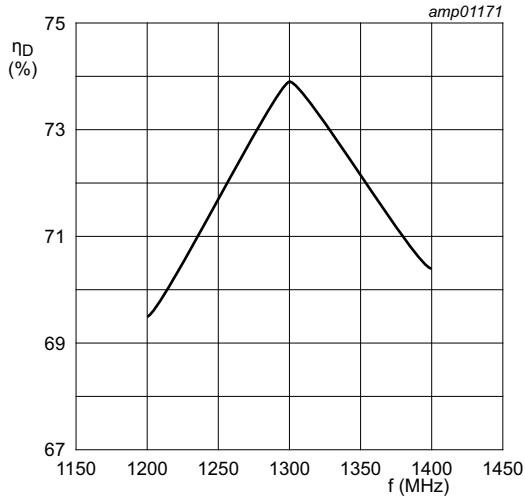
$V_{DS} = 50\text{ V}; I_{Dq} = 500\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 1200\text{ MHz}$   
 (2)  $f = 1300\text{ MHz}$   
 (3)  $f = 1400\text{ MHz}$

**Fig 8. Output power as a function of input power; typical values**



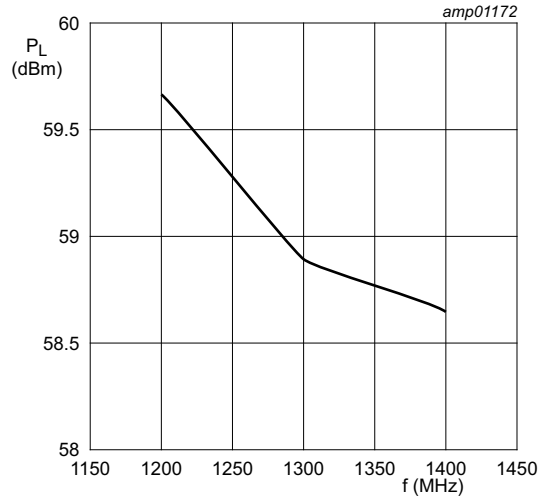
$V_{DS} = 50\text{ V}; I_{Dq} = 500\text{ mA}; P_i = 42.3\text{ dBm}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

**Fig 9. Power gain as a function of frequency; typical values**



$V_{DS} = 50\text{ V}; I_{Dq} = 500\text{ mA}; P_i = 42.3\text{ dBm}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

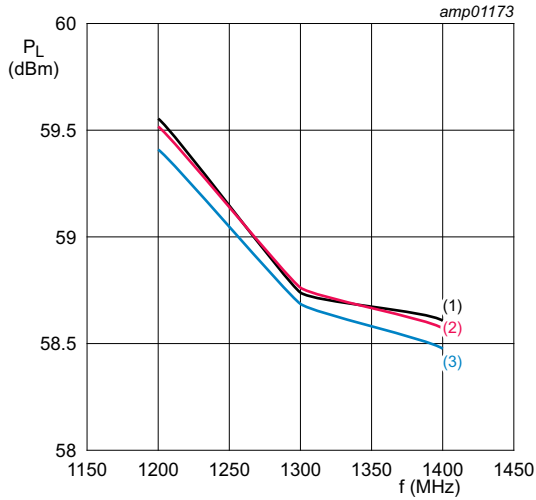
**Fig 10. Drain efficiency as a function of frequency; typical values**



$V_{DS} = 50\text{ V}; I_{Dq} = 500\text{ mA}; P_i = 42.3\text{ dBm}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

**Fig 11. Output power as a function of frequency; typical values**

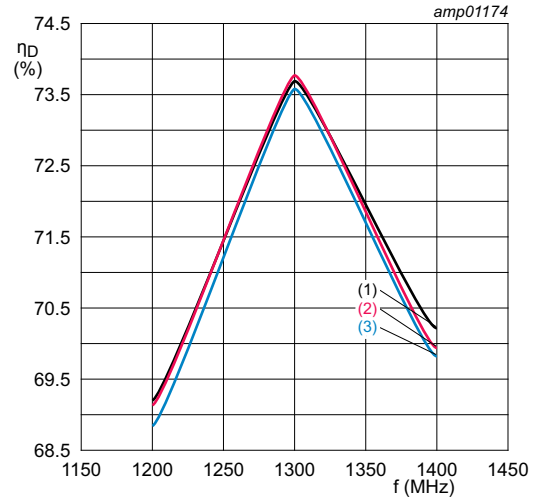




$V_{DS} = 50 \text{ V}$ ;  $I_{DQ} = 500 \text{ mA}$ ;  $P_i = 42.5 \text{ dBm}$ ;  $\delta = 20 \%$ .

- (1)  $t_p = 500 \mu\text{s}$
- (2)  $t_p = 1 \text{ ms}$
- (3)  $t_p = 2 \text{ ms}$

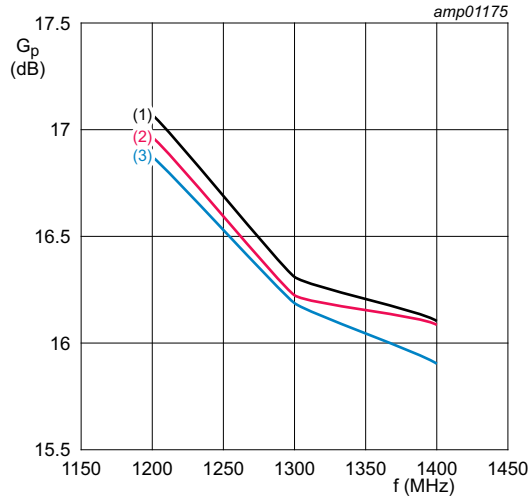
**Fig 12. Output power as a function of frequency, typical values**



$V_{DS} = 50 \text{ V}$ ;  $I_{DQ} = 500 \text{ mA}$ ;  $P_i = 42.5 \text{ dBm}$ ;  $\delta = 20 \%$ .

- (1)  $t_p = 500 \mu\text{s}$
- (2)  $t_p = 1 \text{ ms}$
- (3)  $t_p = 2 \text{ ms}$

**Fig 13. Drain efficiency as a function of frequency; typical values**

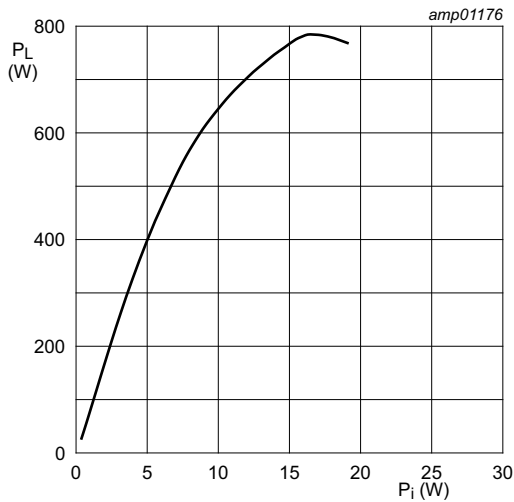


$V_{DS} = 50 \text{ V}$ ;  $I_{DQ} = 500 \text{ mA}$ ;  $P_i = 42.5 \text{ dBm}$ ;  $\delta = 20 \%$ .

- (1)  $t_p = 500 \mu\text{s}$
- (2)  $t_p = 1 \text{ ms}$
- (3)  $t_p = 2 \text{ ms}$

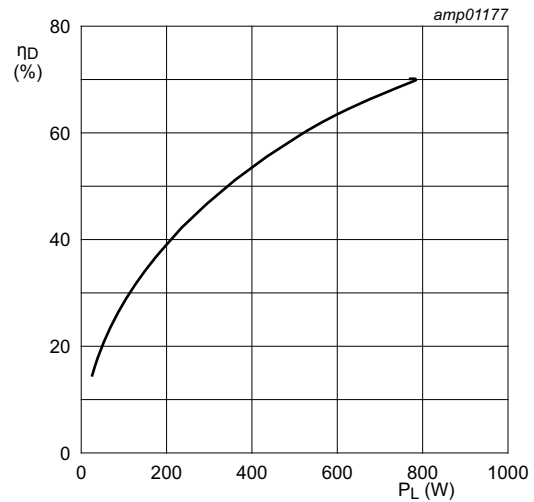
**Fig 14. Power gain as a function of frequency, typical values**

8.3.2 1030 MHz demo board



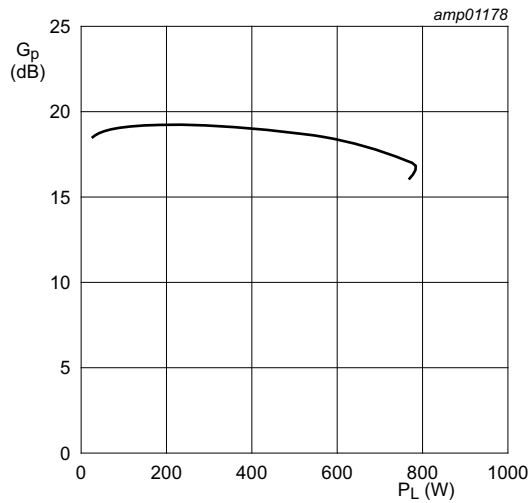
$f = 1030 \text{ MHz}; V_{DS} = 50 \text{ V}; I_{Dq} = 200 \text{ mA}; t_p = 128 \text{ }\mu\text{s}; \delta = 1 \text{ \%}$ .

Fig 15. Output power as a function of input power; typical values



$f = 1030 \text{ MHz}; V_{DS} = 50 \text{ V}; I_{Dq} = 200 \text{ mA}; t_p = 128 \text{ }\mu\text{s}; \delta = 1 \text{ \%}$ .

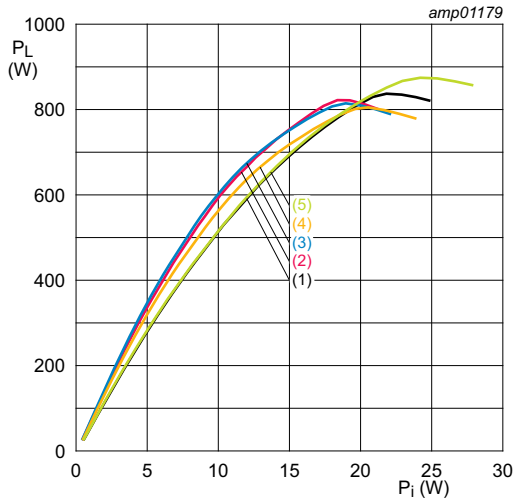
Fig 16. Drain efficiency as a function of output power; typical values



$f = 1030 \text{ MHz}; V_{DS} = 50 \text{ V}; I_{Dq} = 200 \text{ mA}; t_p = 128 \text{ }\mu\text{s}; \delta = 1 \text{ \%}$ .

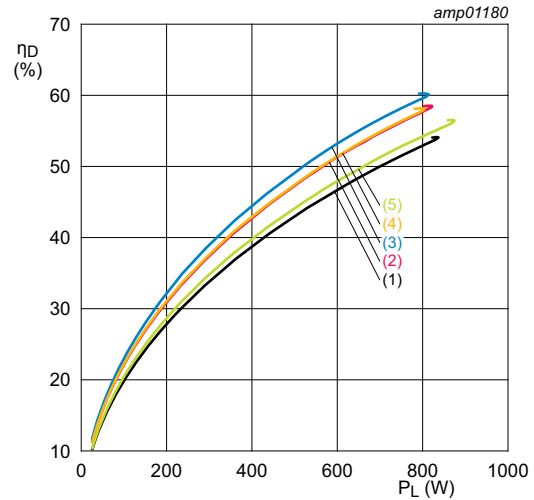
Fig 17. Power gain as a function of output power; typical values

8.3.3 960 MHz to 1215 MHz demo board



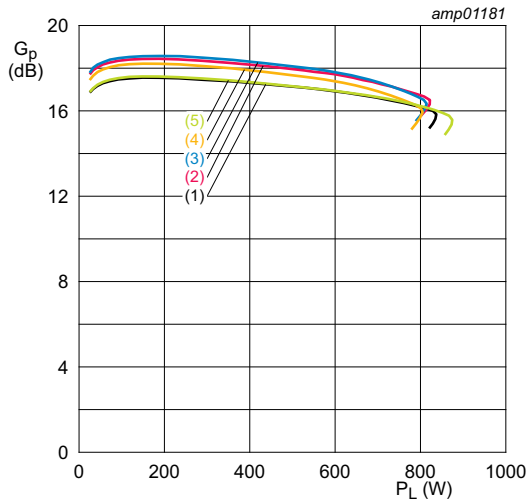
- $V_{DS} = 50 \text{ V}; I_{Dq} = 200 \text{ mA}; t_p = 100 \text{ }\mu\text{s}; \delta = 10 \text{ \%}.$
- (1)  $f = 960 \text{ MHz}$
  - (2)  $f = 1030 \text{ MHz}$
  - (3)  $f = 1090 \text{ MHz}$
  - (4)  $f = 1150 \text{ MHz}$
  - (5)  $f = 1215 \text{ MHz}$

**Fig 18. Output power as a function of input power; typical values**



- $V_{DS} = 50 \text{ V}; I_{Dq} = 200 \text{ mA}; t_p = 100 \text{ }\mu\text{s}; \delta = 10 \text{ \%}.$
- (1)  $f = 960 \text{ MHz}$
  - (2)  $f = 1030 \text{ MHz}$
  - (3)  $f = 1090 \text{ MHz}$
  - (4)  $f = 1150 \text{ MHz}$
  - (5)  $f = 1215 \text{ MHz}$

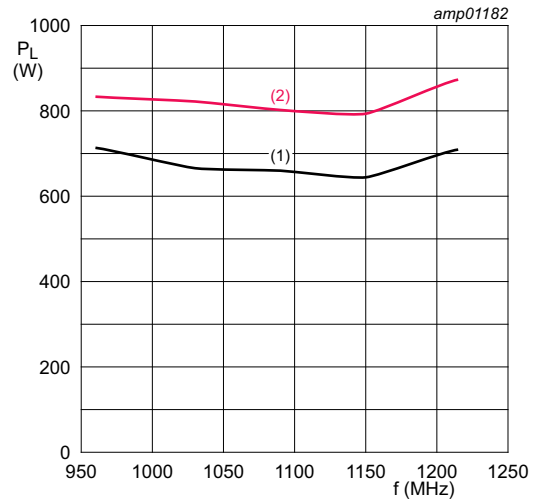
**Fig 19. Drain efficiency as a function of output power; typical values**



$V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 200 \text{ mA}$ ;  $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ .

- (1)  $f = 960 \text{ MHz}$
- (2)  $f = 1030 \text{ MHz}$
- (3)  $f = 1090 \text{ MHz}$
- (4)  $f = 1150 \text{ MHz}$
- (5)  $f = 1215 \text{ MHz}$

**Fig 20. Power gain as a function of output power; typical values**



$V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 200 \text{ mA}$ ;  $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ .

- (1)  $P_{L(1dB)}$
- (2)  $P_{L(2dB)}$

**Fig 21. Output power as a function of frequency; typical values**

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

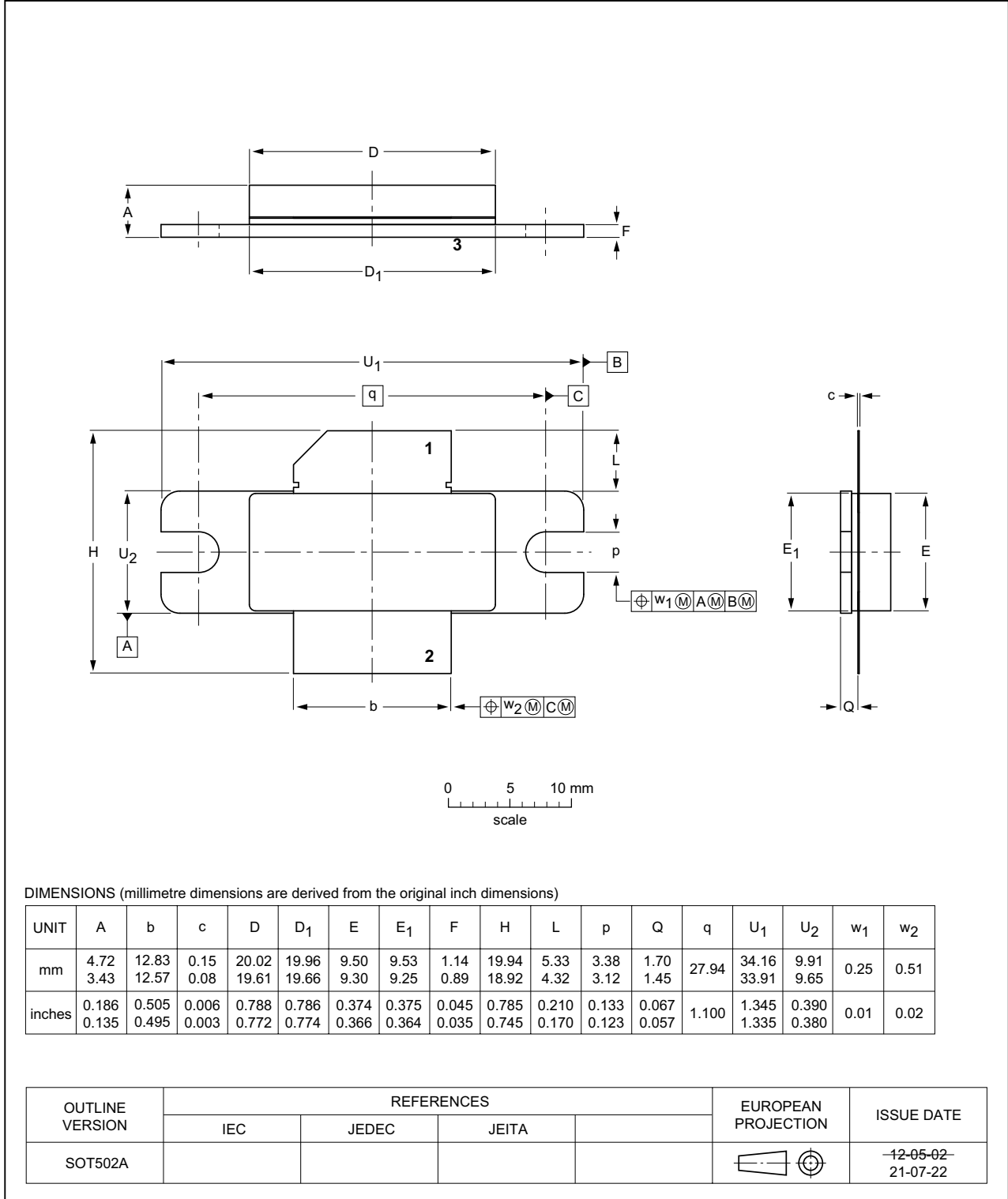


Fig 22. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

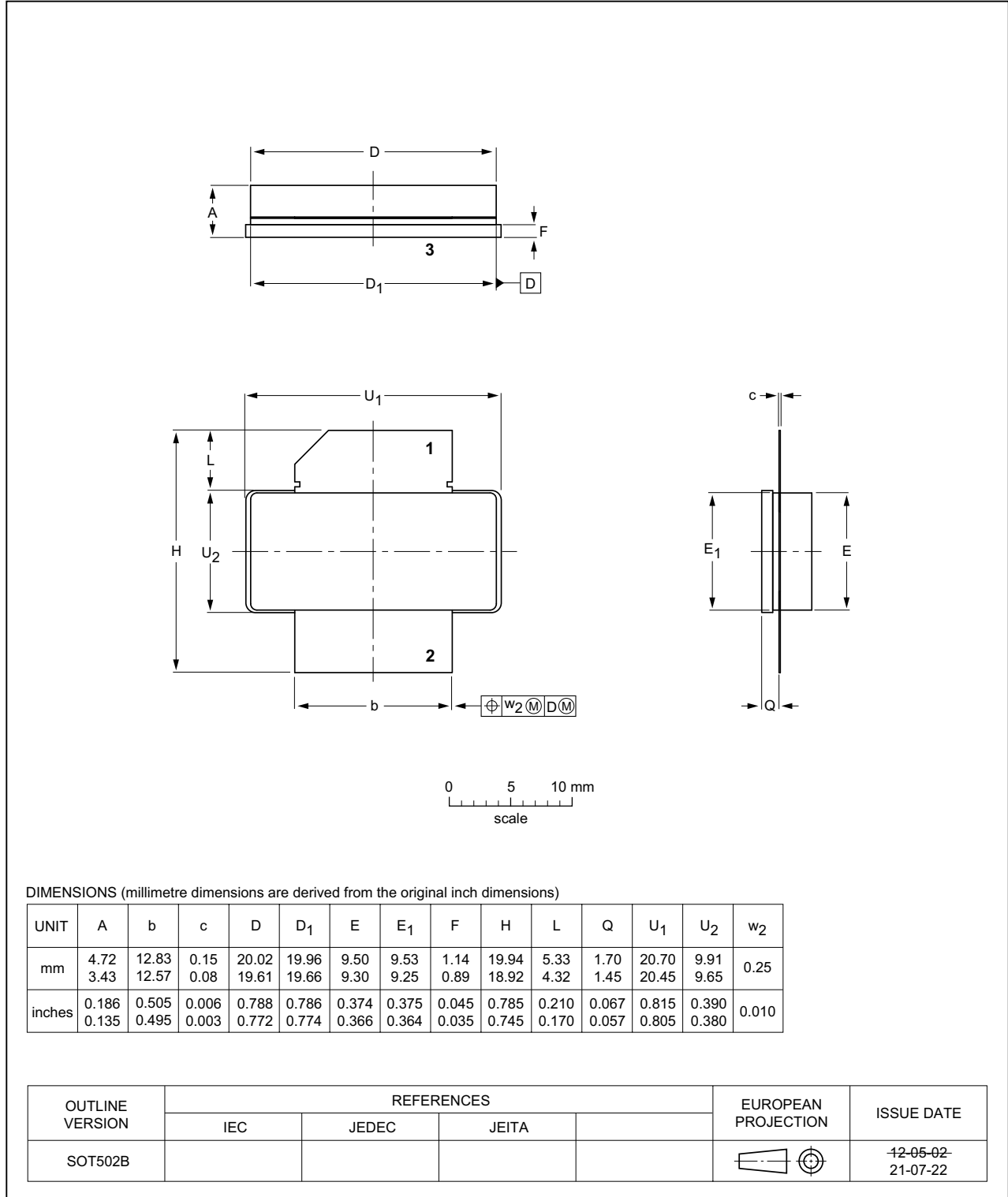


Fig 23. Package outline SOT502B

## 10. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 11. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A <a href="#">[2]</a>

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

## 11. Abbreviations

**Table 12. Abbreviations**

Acronym	Description
CW	Continuous Wave
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
L-band	Long wave band
MTF	Median Time to Failure
SiC	Silicon Carbide
SMD	Surface Mounted Device
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

## 12. Revision history

**Table 13. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLL3H0914L-700_0914LS-700 v.1	20220715	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

### 13.2 Definitions

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