High-Side Measurement Current Shunt Monitor with Comparator

General Description

The RT6052 devices are high-side current-shunt monitors which contain a current-sense amplifier, bandgap reference, and a comparator with latching output. The RT6052 senses drops across shunts at common-mode voltages from 2V to 80V. The RT6052 series support two output voltage scales : 20V/V, and 100V/V.

The RT6052 build in an open-drain comparator and internal reference providing a 0.6V threshold. External dividers set the current trip point. The comparator features a latching capability, that can be made easily by grounding (or leaving open) the $\overline{\text{RESET}}$ pin.

The RT6052 is available in a small 8-pins MSOP package.

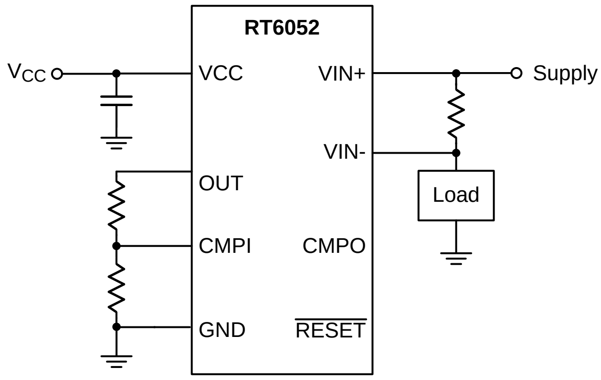
Features

- **High Accuracy Current Sensing**
- **2.9V to 18V Power-Supply Range**
- **RT6052 Gain = 100V/V**
- **Common-Mode Range : 2V to 80V**
- **0.6V Internal Voltage Reference**
- **Internal Open-Drain Comparator**
- **Latching Capability on Comparator**
- **Packages : MSOP-8**

Applications

- Server, Storage and Network Equipment
- Portable, Battery-Powered Systems
- Point of Load (POL) Power Modules
- Notebook Computers
- High End Digital TVs

Simplified Application Circuit



Ordering Information

RT605□ □□

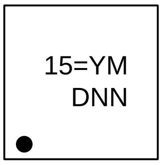
- Package Type
  F : MSOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Gain Options
  2 : 100V/V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

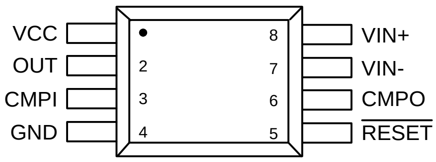


15= : Product Code

YMDNN : Date Code

Pin Configuration

(TOP VIEW)

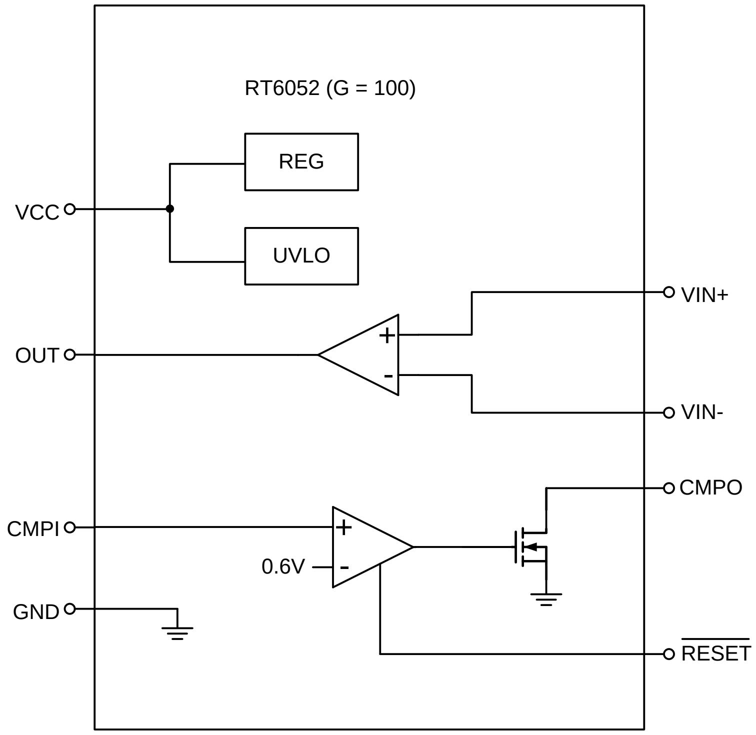


MSOP-8

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCC	Power input. Connect a 0.1μF capacitor as close to the VCC pin as possible.
2	OUT	Voltage output. V_{OUT} is proportional to V_{SENSE} (VIN+ – VIN-).
3	CMPI	Comparator input. Positive input of an internal comparator. The negative terminal is connected to a 0.6V internal reference.
4	GND	Ground.
5	$\overline{\text{RESET}}$	Reset input pin. Reset the output latch of the comparator, active low.
6	CMPO	Open-drain comparator output. Connect $\overline{\text{RESET}}$ to GND to disable the latch.
7	VIN-	Negative current-sensing input. Connect load side to external sense resistor.
8	VIN+	Positive current-sensing input. Connect power side to external sense resistor.

Functional Block Diagram



Operation

The RT6052 devices are high-side, unidirectional, current-shunt monitors with a high common-mode input range extending from 2V to 80V. The devices are available with two output voltage scales: 20V/V and 100V/V, with up to 500kHz bandwidth. The over-current protection is also available by internal comparator, when the voltage at CMPI pin is higher than internal reference 0.6V, the CMPO pulls high to indicate over-current situation. Connect a divider from OUT pin to CMPI pin to set the over-current trip point, the devices provides an open-drain comparator with a latching function, that the output signal of comparator can be latched or non-latched by $\overline{\text{RESET}}$ pin setting.

Comparator and Reset

The RT6052 devices incorporate an open-drain comparator. This comparator typically has 1.3μs (typical) response time. The output of the comparator latches and is reset through the $\overline{\text{RESET}}$ pin. From the Figure 1. The control logic can be described as 3 stages.

Stage1. The V_{CMPO} goes high after V_{CMPI} increases and eventually over than 0.6V.

Stage2. When the $V_{\overline{RESET}}$ is high, The V_{CMPO} is kept high even V_{CMPI} decreases and lower than 0.6V, when the $V_{\overline{RESET}}$ goes low, the V_{CMPO} goes low as well.

Stage3. When the $V_{\overline{RESET}}$ is low, The V_{CMPO} goes high/low depending on V_{CMPI} higher/lower than 0.6V.

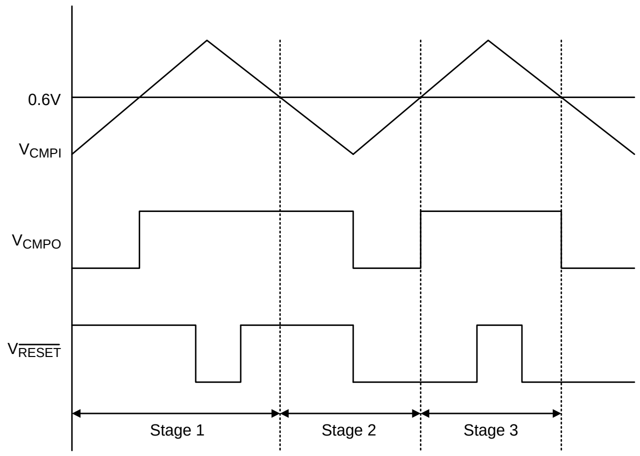


Figure 1. Comparator Latching and Reset Logic

Power On

The RT6052 implements power on reset (POR) function to prevent operation without fully turn-on the internal control circuit. When the V_{CC} is increasing and eventually higher than POR rising threshold (2.75V, typical), the device starts output voltage, in contrast, when the V_{CC} is lower than POR falling threshold (2.55V, typical), the device stops output voltage**.**

Gain Error and Input Offset Voltage

Using two-step method to characterize gain error and offset voltage, first of all, the gain can be obtained by measuring different sense voltage.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV\text{-}20mV}$$

Where

- V_{OUT1} = output voltage with V_{SENSE} = 100mV
- V_{OUT2} = output voltage with V_{SENSE} = 20 V

Then the offset voltage is measured at V_{SENSE} = 100mV, and referred to the input (RTI) of the current shunt monitor, as shown in Electrical Characteristics: Current-Shunt Monitor.

$$\text{VRTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100mV$$

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- –0.3V to 19.8V
- Power Sensing PINS, VIN+, VIN- (common mode), V_{CM} ---------- –6V to 88V
- Power Sensing PINS, VIN+ -VIN- (different mode), V_{SENSE} ---------- –6V to 18V
- Other Pins, CMPI, CMPO, OUT, $\overline{RESET}$ ---------- –0.3V to 19.8V
- Power Dissipation, P_D @ T_A = 25°C
  MSOP-8 ---------- 0.27W
- Package Thermal Resistance (Note 2)
  MSOP-8, θ_{JA} ---------- 361.6°C/W
  MSOP-8, θ_{JC} ---------- 90.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 4kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} ---------- 2.9V to 18V
- Common mode input range, V_{CM} ---------- 2V to 80V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 12V, V_{CM} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Operating Power Supply	V_{CC}		2.9	--	18	V
Quiescent Current	I_Q	V_{OUT} = 2V	--	--	1000	μA
		V_{SENSE} = 0mV	--	--	300	
POR Rising Threshold	V_{PORH}		2.7	2.75	2.85	V
POR Falling Threshold	V_{PORL}		--	2.55	--	V
Current Sense						
Full Scale Sense Input Voltage			--	0.15	--	V
Common Mode Input Range	V_{CM}		2	--	80	V
Common Mode Rejection (Note 5)	CMR	V_{IN+} = 2V to 80V, V_{SENSE} = 100mV	80	100	--	dB
Offset Voltage, RTI	V_{OS}	T_A = 25°C	--	±0.5	±2.5	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PSR of Offset Voltage, RTI	PSR	V_{OUT} = 2V, V_{IN+} = 18V, V_{CC} = 2.9V	--	2.5	50	μV/V
Input bias current	I_B	VIN- pin	--	13	--	μA
Gain	G		--	100	--	V/V
Gain Error	GE%	V_{SENSE} = 20mV to 100mV	--	±0.2	±1	%
Total Output Error	$\Delta V_{OUT\%}$	V_{SENSE} = 120mV, V_{CC} = 16V	--	±0.75	±2.2	%
Nonlinearity Error (Note 5)	NLIN%	V_{SENSE} = 20mV to 100mV	--	0.1	--	%
Maximum Capacitive Load (Note 5)			--	10	--	nF
Output Voltage Range H		V_{IN-} = 11V, V_{IN+} = 12V	--	V_{CC} −0.15	--	V
Output Voltage Range L		V_{IN-} = 0V, V_{IN+} = −0.5V	--	4	350	mV
Slew Rate	SR		--	1.5	--	V/μs
Settling Time	T_{ST}	V_{SENSE} = 10mV to 100mV 10%~90% V_{OUT} C_{LOAD} = 5pF	--	6	--	μs
Noise Density, RTI (Note 5)		Frequency = 10k	--	40	--	nV/√Hz
Comparator						
Threshold	V_{TH}		585	600	615	mV
Hysteresis	V_{HYS}		--	−8	--	mV
Input Bias Current	I_{B_CM}		--	0.005	10	nA
Maximum Input			--	V_{CC} −1.5	--	V
Output Open-Drain						
Voltage Gain (Note 5)	CMP_{GAIN}		--	200	--	V/mV
Leakage Current	I_{LEAK}		--	0.0001	1	μA
Dropout Voltage	V_{DROP}	I_{LOAD} = 2.35mA	--	125	220	mV
Response Time	T_{RS}	R_L to 5V, C_L = 15pF 100mV input step with 10mV overdrive	--	1.3	--	μs
$\overline{\text{RESET}}$						
$\overline{\text{RESET}}$ Pin Threshold	V_{RST_H}	High Level	1	--	--	V
	V_{RST_L}	Low Level	--	--	0.4	V
$\overline{\text{RESET}}$ Input Impedance			--	2	--	MΩ
$\overline{\text{RESET}}$ Minimum Pulse Width			--	1.5	--	μs
RESET Propagation Delay			--	1.6	--	μs

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

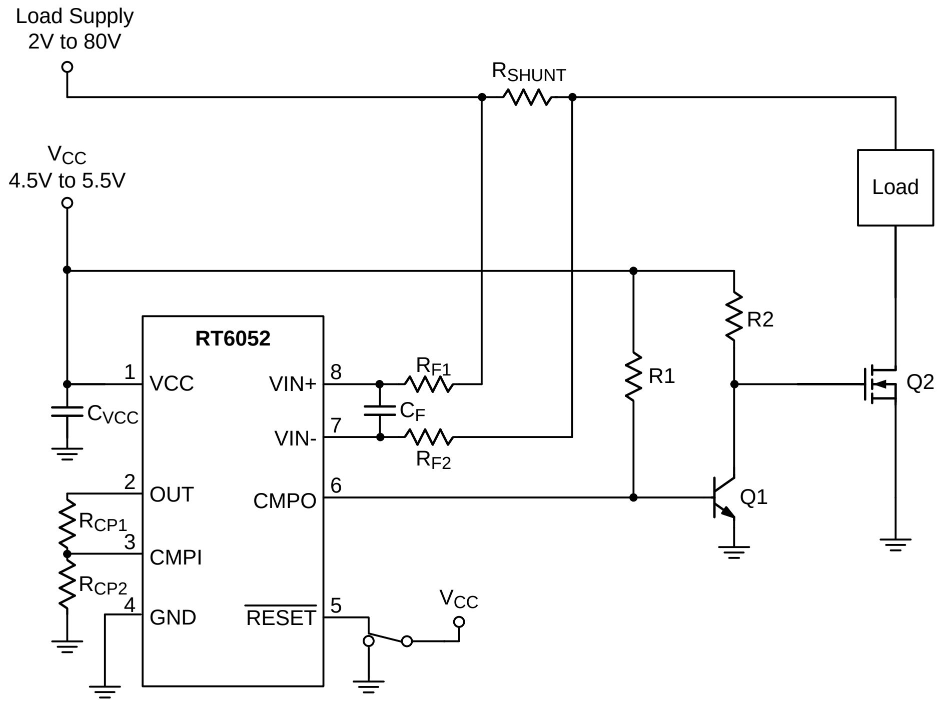
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

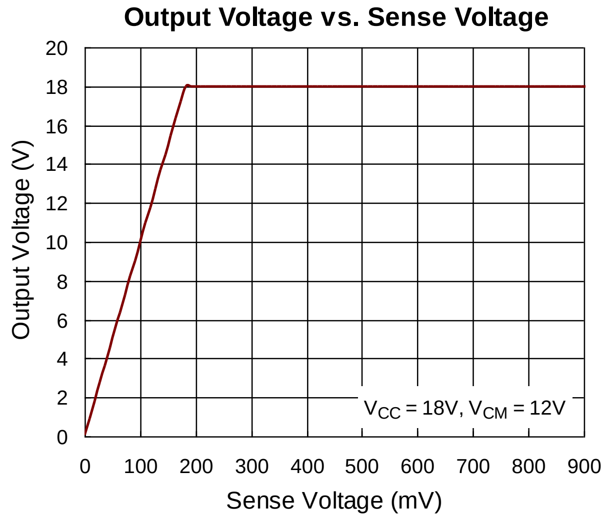
Note 4. The device is not guaranteed to function outside its operating conditions.

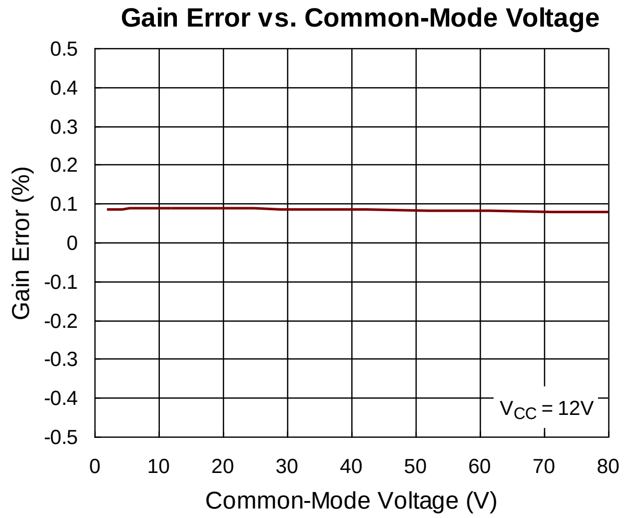
Note 5. Specifications are guaranteed by design, not production tested.

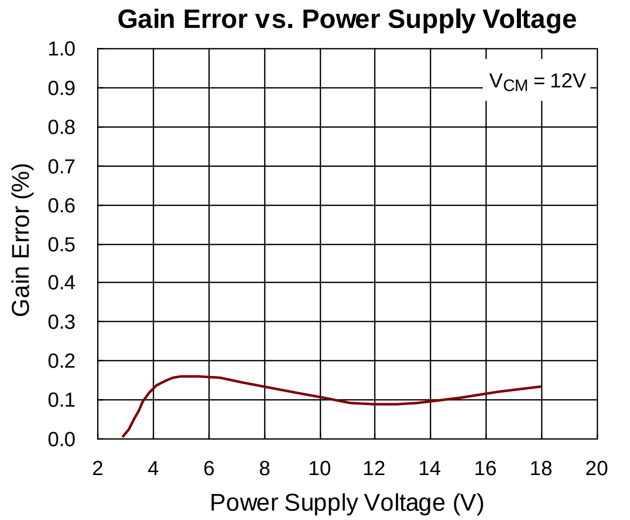
Typical Application Circuit

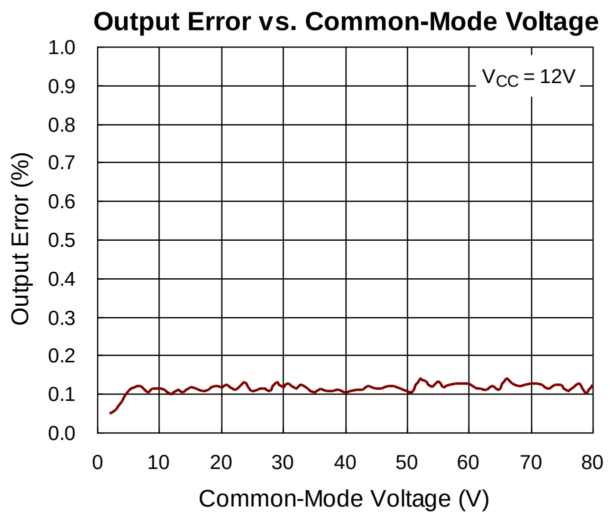


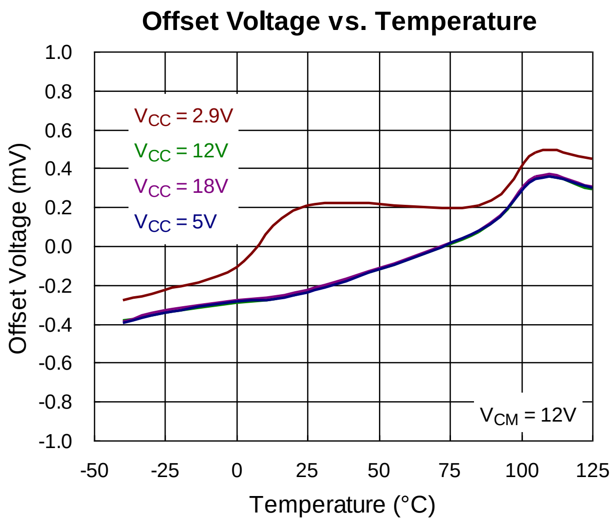
Typical Operating Characteristics

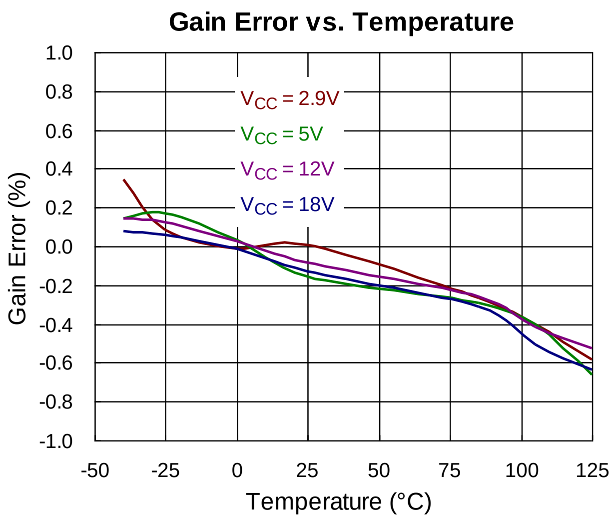


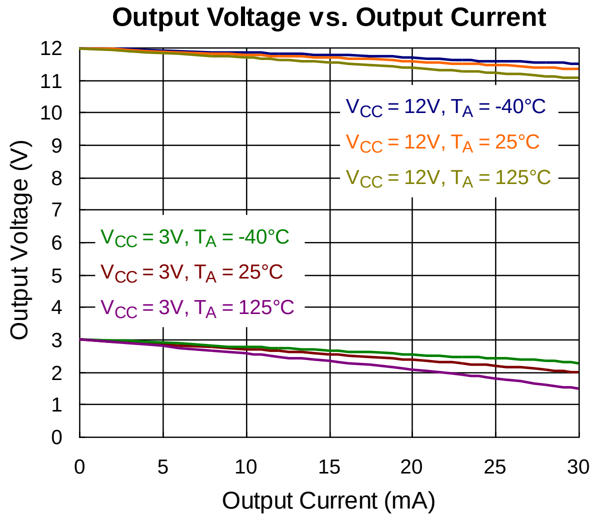


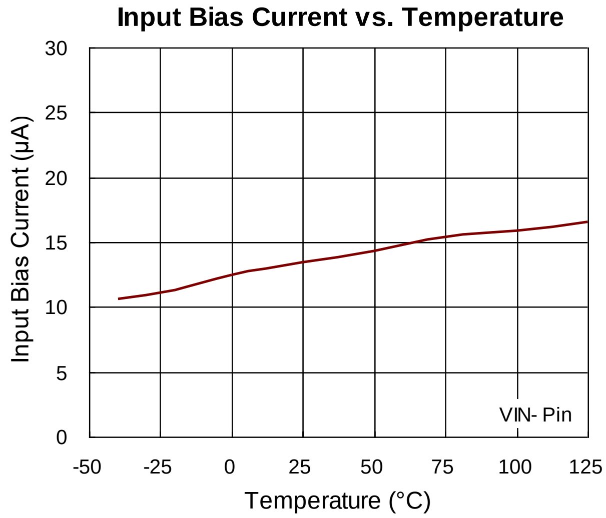


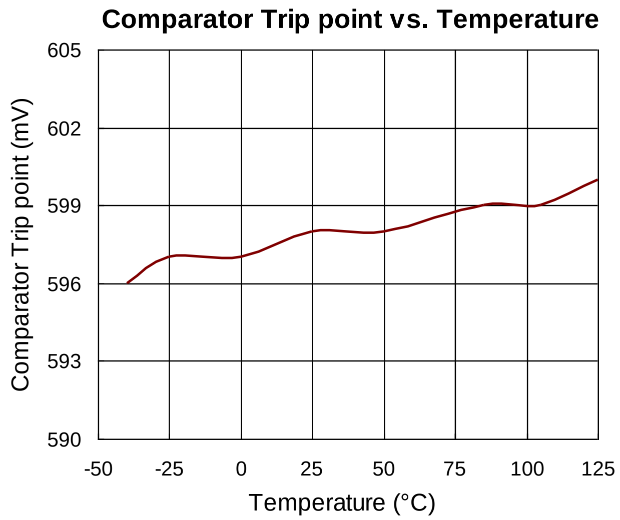







Output Voltage vs. Output Current
Output Voltage (V)
Output Current (mA)
VCC = 12V, TA = -40°C
VCC = 12V, TA = 25°C
VCC = 12V, TA = 125°C
VCC = 3V, TA = -40°C
VCC = 3V, TA = 25°C
VCC = 3V, TA = 125°C
0 1 2 3 4 5 6 7 8 9 10 11 12
0 5 10 15 20 25 30


Input Bias Current vs. Temperature
Input Bias Current (μA)
Temperature (°C)
VIN- Pin
0 5 10 15 20 25 30
-50 -25 0 25 50 75 100 125


Comparator Trip point vs. Temperature
Comparator Trip point (mV)
Temperature (°C)
590 593 596 599 602 605
-50 -25 0 25 50 75 100 125

Application Information

Selecting the Shunt Resistor

The selected value for the shunt resistor, R_{SHUNT}, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_{SHUNT} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{SHUNT} minimize voltage loss in the supply line. For best performance, select R_{SHUNT} to provide approximately 50mV to 100mV of sense voltage for the full-scale current in each application. Maximum input voltage for accurate measurements is 500mV, but output voltage is limited by supply voltage V_{CC}.

Input Filtering

In some applications, the current being measured may be inherently noisy. In the case of a noisy signal, filtering after the output of the current sense amplifier is often simpler; however, this location negates the advantage of the low output impedance of the internal buffer.

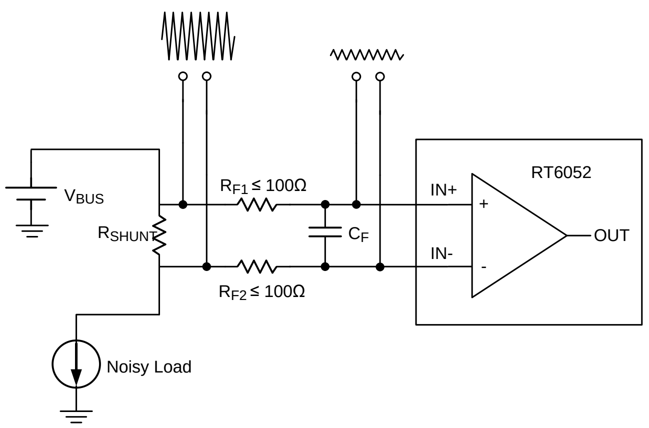


Figure 2. Input Filter

Other applications may require filtering at the input of the current sense amplifier. Figure 2 shows the recommended schematic for input filtering.

Input filtering is complicated by the fact that the added resistance of the filter resistors and the associated resistance mismatch between them can adversely affect gain, CMR, and offset voltage, V_{OS}. The effect on V_{OS} is partly due to input bias currents as well. As a result, the value of the input resistors should be limited to 100Ω or less.

Total Error Analysis

In order to optimize the design, the first is to analysis the contribution of each error, the main influences of sense voltage errors can be identified as follow :

- The tolerance of shunt resistor (R_{SHUNT})
- Sense offset voltage, V_{OS}. When the sense voltage is small, especially low load current and small shunt resistance, the error is dominated by the input offset error.
- Gain Error, GE%
- PSR of offset voltage, PSR
- Common mode rejection, CMR
- The offset voltage caused by input bias current
- Nonlinearity Error, NLIN%

Max Output Error Estimation

Here gives an example. The system bus voltage V_{CM_SYS} connects to VIN+ = 18V, system supply voltage V_{CC_SYS} = 12V, shunt resistor is accuracy 1%, 10mΩ 1.5W, the load current is 10A. To set the design goals, the maximum output voltage errors are calculated as follows.

Input Offset Voltage Error

The rate of offset error in the total error can be estimated directly from the specification table. The input offset voltage is 2.5mV at T_A = 25°C, the error due to offset can be obtained by below equation :

$$V_{OS\_err} = \frac{V_{OS(max)}}{V_{SENSE}} \times 100\% = \frac{2.5mV}{10m\Omega \times 10A} \times 100\% = 2.5\%$$

Shunt Voltage Gain Error

From the electrical characteristics, the max gain error is 1%

PSR Error

The PSR error is to estimate the error caused by different supply voltage, the RT6052 device specification gives the specified power supply voltage for the input offset voltage specification as V_{CC_DS} = 2.9V, when the system supply voltage is not exactly 2.9V may result in an additional error. RT6052 device gives the maximum PSR as 50μV/V. Calculate the PSR error by equation below :

$$PSR\_err = \frac{|V_{CC\_DS} - V_{CC\_SYS}| \times PSR}{V_{SENSE}} \times 100\%$$

$$= \frac{|2.9 - 12V| \times 50\frac{\mu V}{V}}{10m\Omega \times 10A} \times 100\% = 0.45\%$$

CMR Error

The CMR error means the input offset error is influenced by the variation of common-mode voltage, in real conditions, calculate the maximum input offset by determining the actual common-mode voltage as applied to RT6052. According to the RT6052 device specification, it gives the common-mode rejection ratio minimum as 80dB (100μV/V). The offset voltage in the data sheet is specified with a common-mode voltage, V_{CM_DS} that is 12V. To calculate the actual common-mode error at system bus voltage is :

$$80dB = \frac{1}{10^{\left(\frac{80dB}{20}\right)}} \times 10^6 \times \frac{\mu V}{V} = 100\frac{\mu V}{V}$$

$$CMR\_err = \frac{|V_{CM\_DS} - V_{CM\_SYS}| \times CMR}{V_{SENSE}} \times 100\%$$

$$= \frac{|12 - 18| \times 100\frac{\mu V}{V}}{10m\Omega \times 10A} \times 100\% = 0.6\%$$

Input Bias Current Error

The input bias current flows into shunt resistor to cause additional offset, this error is calculated with respect to the ideal voltage across the sense voltage.

$$I_{B\_err} = \frac{I_B \times R_{SHUNT}}{V_{SENSE}} \times 100\% = \frac{13\mu A \times 10m\Omega}{10m\Omega \times 10A} \times 100\%$$

$$= 0.00013\%$$

Nonlinearity Error

The nonlinearity error shown in Figure 3 is the difference between an actual gain and the ideal value. For ideal cases, the voltage gain is constant over fully sense ranges, but in the real application, the voltage gain is not exactly constant, the nonlinearity gain may cause some additional errors. In the specification, the RT6052 gives the nonlinearity error as 0.1% over sense voltage from 20mV to 100mV.

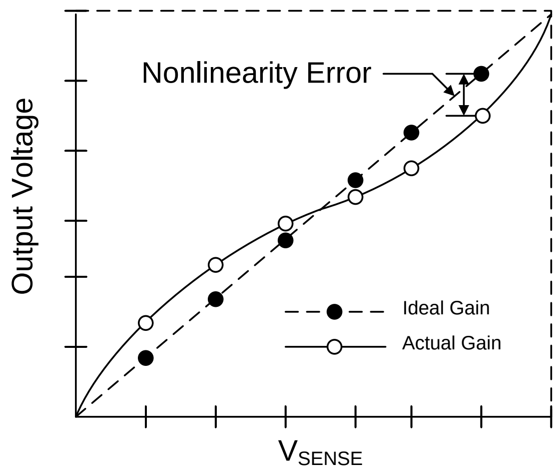


Figure 3. Nonlinearity Error

Total Error

The below equation can calculate the worst case of total error

$$Total\_err = \sqrt{(GE\%)^2 + (R\%)^2 + (V_{OS\_err})^2 + (PSR\_err)^2 + (CMR\_err)^2 + (I_{B\_err})^2 + (NLIN\%)^2}$$

$$= \sqrt{(1\%)^2 + (1\%)^2 + (2.5\%)^2 + (0.45\%)^2 + (0.6\%)^2 + (0.0013\%)^2 + (0.1\%)^2}$$

$$= 3.07\%$$

Layout Guidelines

- A Kelvin sense arrangement is required for best performance. Connect the input pins (VIN+ and VIN-) to the sensing resistor using a 4-wire connection.
- PCB trace resistance from the sense resistor to the VIN+ and VIN- pins can affect the power measurement accuracy. Place the sense resistors as close as possible to the RT6052 and not to use minimum width PCB traces.
- Place the power-supply bypass capacitor 0.1μF as close as possible to the supply and ground pins.

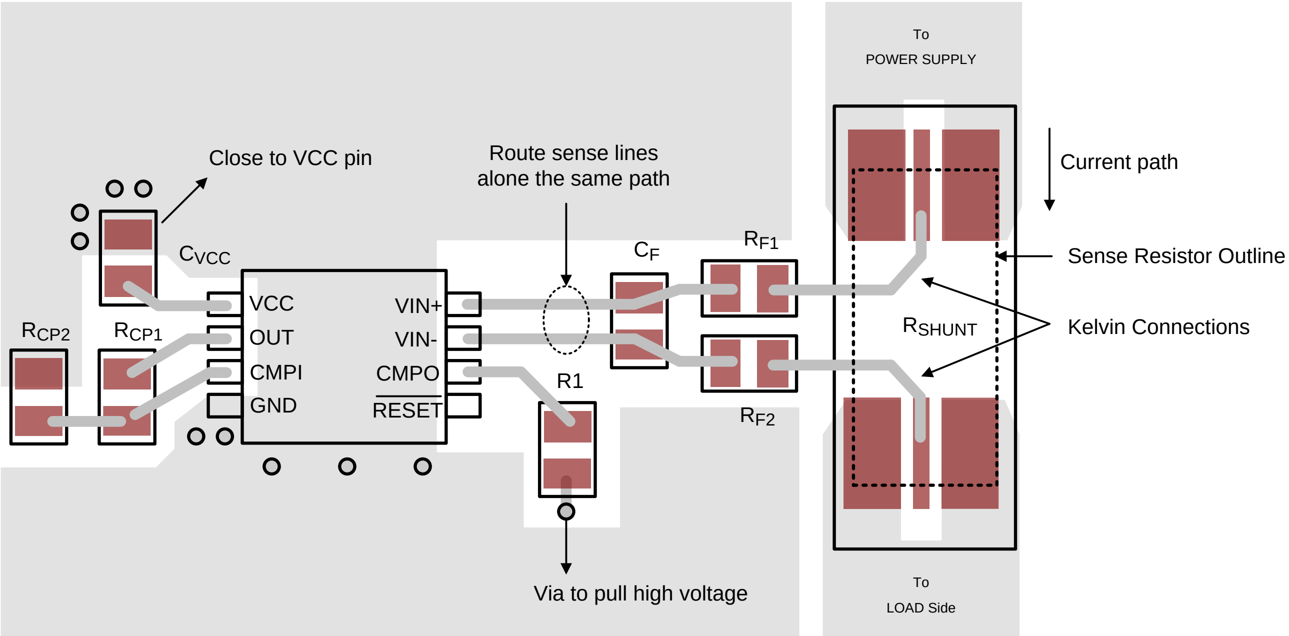
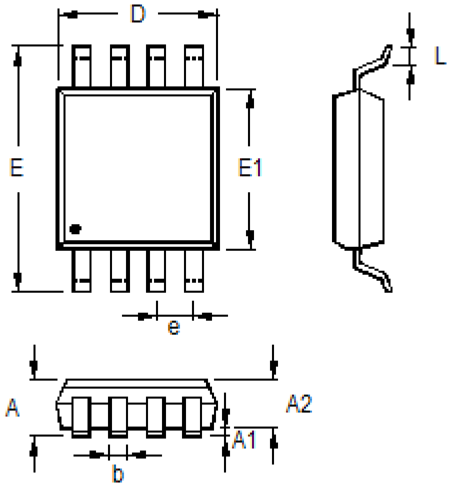


Figure 4. PCB Layout Guide

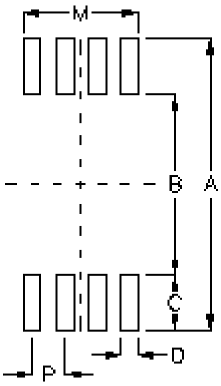
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.220	0.380	0.009	0.015
D	2.900	3.100	0.114	0.122
e	0.650		0.026	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

8-Lead MSOP Plastic Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
MSOP-8	8	0.65	5.80	3.60	1.10	0.35	2.30	±0.10

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