MP3372

8-Channel, 50V Sync-Boost WLED Driver with I²C Interface

DESCRIPTION

The MP3372 is a synchronous boost converter with eight current channels designed to drive WLED arrays for LCD panels in tablets and notebook backlighting applications.

The MP3372 uses peak current mode and pulse-width modulation (PWM) control to regulate the boost converter. The device employs a standard I²C digital interface to set the operation mode, switching frequency, full-scale current, synchronous or asynchronous mode, dimming mode and duty, and various protection thresholds.

The MP3372 features high efficiency due to the low headroom voltage for LED regulation and the switching MOSFET's small on resistance. The synchronous rectifier saves PCB size and total BOM cost.

The MP3372 is available in a QFN-24 (4mmx4mm) package.

FEATURES

- 8 Channels with Maximum 50mA/Channel
- Synchronous Converter with 50V LS-FET/HS-FET with 150m/230mΩ On Resistance
- 3V to 30V Input Voltage Range
- Maximum 2.5% Current Matching
- 350kHz, 500kHz, 650kHz, 800kHz, 950kHz, 1.2MHz, 1.8MHz, or 2.4MHz Selectable Switching Frequency
- A1 Pins for Two I²C Addresses
- 0mA to 50mA Full-Scale LED Current, 8-Bit, 0.196mA/Step
- Selectable Synchronous or Asynchronous Mode
- Multi-Dimming Operation Mode, including:
  - Analog Dimming through External PWM Input, 10-Bit Resolution
  - Analog Dimming through the I²C Interface, 10-Bit Resolution
  - PWM Dimming through External PWM Input, 14-Bit Resolution
  - PWM Dimming through the I²C Interface, 14-Bit Resolution
  - Mixed Dimming Mode through External PWM Input with 6.25%, 12.5%, 25%, or 50% Transfer Point, 14-Bit PWM Duty Resolution
  - Mixed Dimming Mode through the I²C interface with 6.25%, 12.5%, 25%, or 50% Transfer Point,14-Bit PWM Duty Resolution
- Phase Shift Function during PWM Dimming (including PWM Dimming during Mixed Dimming Mode)
- Linear Smooth Dimming with 2µs, 4µs, 8µs, 16µs, 32µs, 64µs, or 128µs Step-Slope Set
- Unused LED Strings Auto-Disabled at Start-Up
- LED Short, Open, OTP, OCP, Inductor or Diode Short Protection
  - 2.5V, 5V, 7.5V, or 10V LED Short Threshold
  - 24V, 31V, 38V, or 46V OVP Threshold
  - 1.8A or 2.5A Current Limit
- Cascade Function to Share Power Stage
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- Tablets/Notebooks
- Automotive Displays

TYPICAL APPLICATION

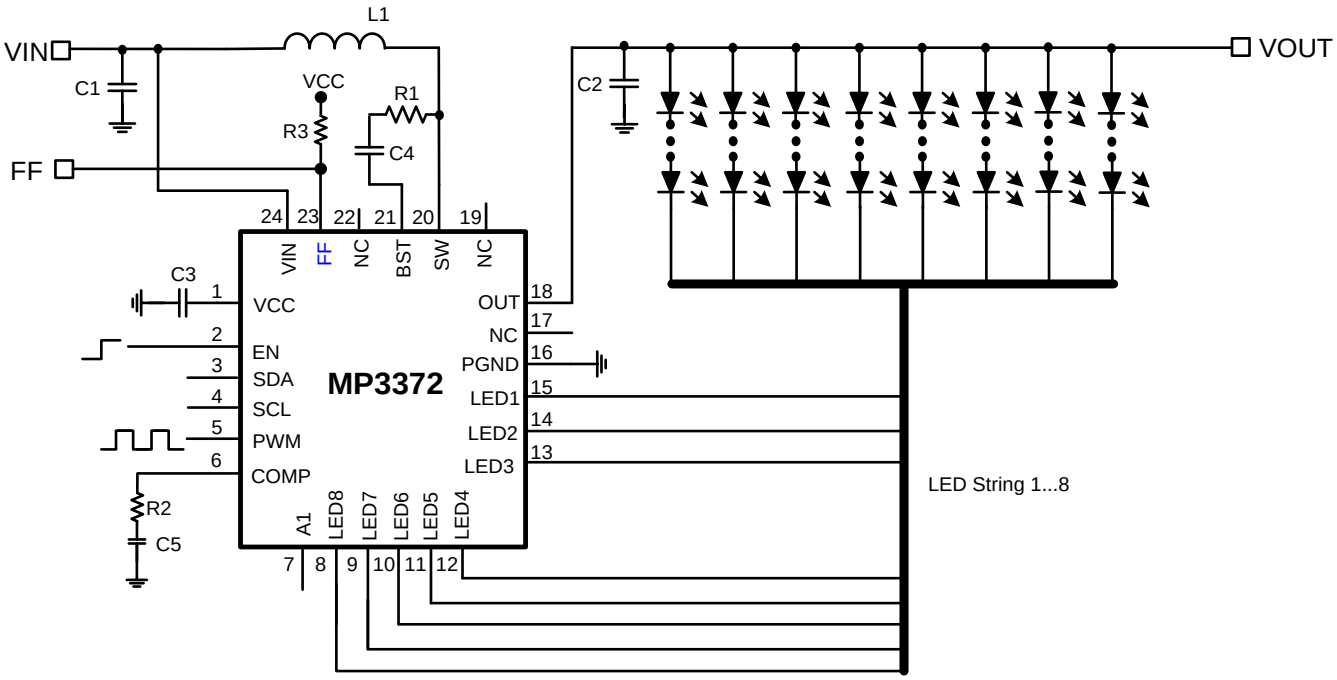


Figure 1: Pull FF to GND when VOUT is Shorted to GND

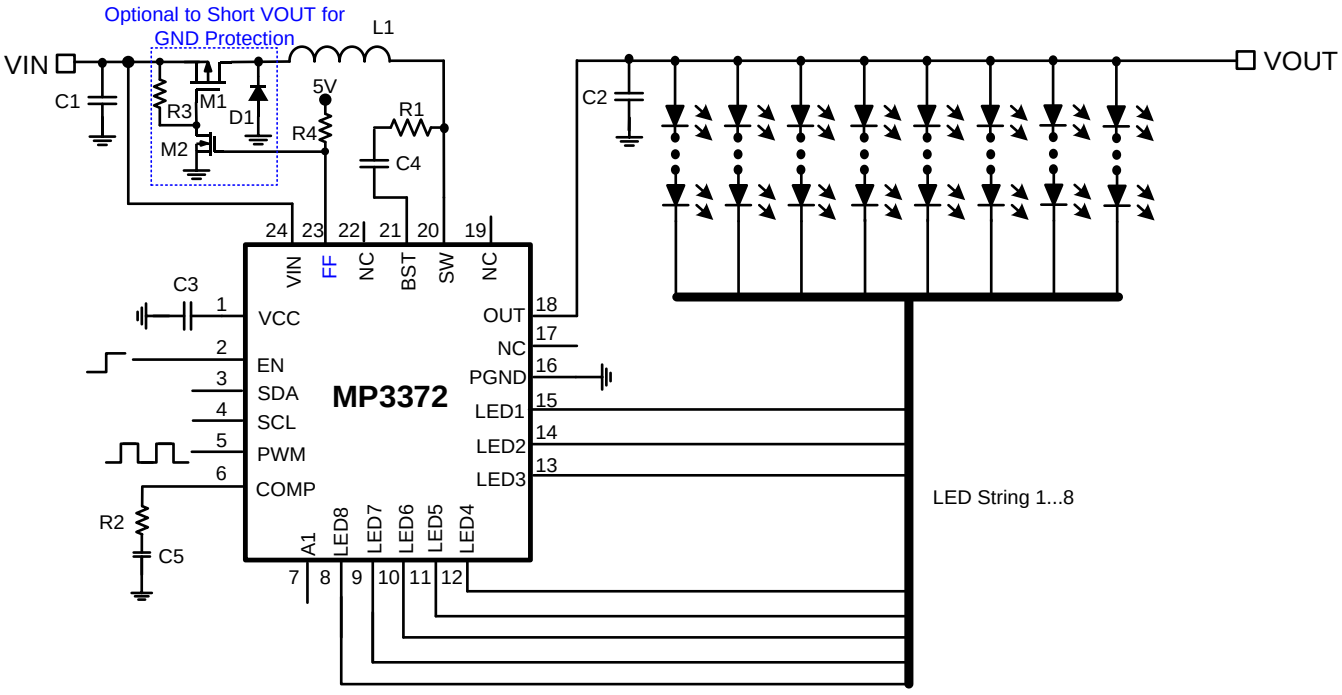


Figure 2: Add External MOSFET to Disconnect VOUT from VIN when VOUT is Shorted to GND

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3372GR-xxxx**	QFN-24 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP3372GR-xxxx–Z).

** "xxxx" is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for a non-default function option. "-0000" is the default function value.

TOP MARKING

MPSYWW

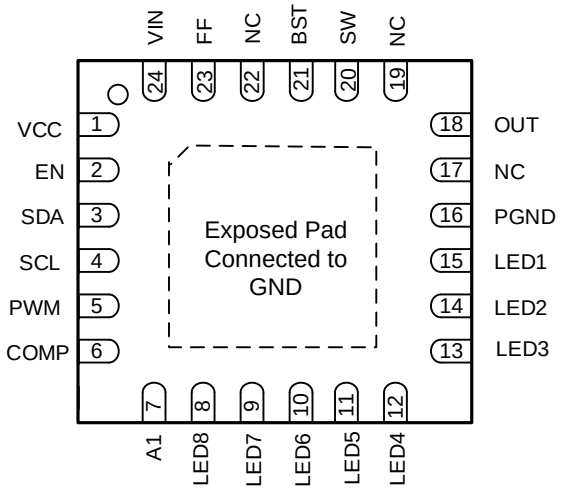
MP3372

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP3372: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**4.9V LDO output.** VCC provides power for the internal logic and gate driver. Place a ceramic capacitor as close to VCC as possible to reduce noise.
2	EN	**IC enable.** Pull EN high to enable the IC; pull EN low to make the IC enter shutdown mode.
3	SDA	**I²C interface data input.** If SDA is not used, pull it high with a pull-up resistor.
4	SCL	**I²C interface clock input.** If SCL is not used, pull it high with a pull-up resistor.
5	PWM	**PWM signal input.** Connect PWM to GND if not used.
6	COMP	**Compensation pin.** Connect a capacitor and resistor to GND.
7	A1	**IC Select.** A1 is pulled high internally. Float A1 for 0x29, and connect A1 to GND for 0x28.
8	LED8	**LED current source 8 output.** If LED8 is unused, tie it to GND.
9	LED7	**LED current source 7 output.** If LED7 is unused, tie it to GND.
10	LED6	**LED current source 6 output.** If LED6 is unused, tie it to GND.
11	LED5	**LED current source 5 output.** If LED5 is unused, tie it to GND.
12	LED4	**LED current source 4 output.** If LED4 is unused, tie it to GND.
13	LED3	**LED current source 3 output.** If LED3 is unused, tie it to GND.
14	LED2	**LED current source 2 output.** If LED2 is unused, tie it to GND.
15	LED1	**LED current source 1 output.** If LED1 is unused, tie it to GND.
16	PGND	**Power ground.**
17, 19, 22	NC	**No connection.**
18	OUT	**Synchronous boost output.**
20	SW	**Switching node.**
21	BST	**Bootstrap capacitor node for the high-side MOSFET.** Connect a 100nF ceramic capacitor and a 10Ω resistor in series between BST and SW for synchronous mode.
23	FF	**Fault flag pin.** The FF pin is an open-drain MOSFET structure. When VOUT is shorted to GND, FF is pulled to GND.
24	VIN	**IC input power.** Place a ceramic capacitor as close to VIN as possible to reduce noise.
	EP	**Exposed pad.** Connect the exposed pad to GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW}, V_{OUT}.....-0.3V to +55V
V_{LEDX} .....-0.3V to +50V
V_{BST} ..... -0.3V to V_{SW} + 5.5V
V_{IN} .....-0.3V to +32V
V_{FF}.....-0.3V to +5V
All other pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to 150°C
Continuous power dissipation T_A = 25°C (2)
QFN-24 (4mmx4mm)..... 2.7W

ESD Ratings

Human body model (HBM)…….. ±2000V
Charged device model (CDM).....±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 30V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4)	***θ_{JA}***	***θ_{JC}***
QFN-24 (4mmx4mm)	46	10

°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 6V, V_{EN} = 2V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}	2.7V has higher V_{LEDX}	2.7		30	V
Quiescent supply current	I_Q	D_{PWM} = 50%, no switching	2.1	2.8	3.5	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 3.7V			1	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge	2.3	2.6	2.9	V
Input UVLO hysteresis				300		mV
LDO output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 30V, 0 < I_{VCC} < 10mA	4.4	4.9	5.4	V
EN on threshold	V_{EN_ON}	V_{EN} rising	1.2			V
EN off threshold	V_{EN_OFF}	V_{EN} falling			0.4	V
EN pull-down resistor	R_{EN}			500		kΩ
A1 low threshold	V_{A_LO}	V_A falling			0.4	V
A1 high threshold	V_{A_HI}	V_A rising	1.2			V
A1 pull-up resistor	R_{P_A}			500		kΩ
Step-Up Converter						
Low-side MOSFET on resistance	R_{DS_LS}	V_{IN} = 6V	120	150	180	mΩ
High-side MOSFET on resistance	R_{DS_HS}	V_{IN} = 6V	190	230	270	mΩ
SW leakage current	I_{SW_LK}	V_{SW} = 50V			1	μA
Switching frequency	f_{SW}	FS2:0 bits = 010b	585	650	715	kHz
Maximum duty cycle	D_{MAX}	Synchronous mode, f_{SW} = 650kHz	91	93.5		%
		Asynchronous mode, f_{SW} = 650kHz	92	94		%
SW current limit	I_{SW_LIMIT}	Duty = 90%, ILIM bit = 1b	2	2.5		A
Zero-current detection	I_{ZCD}			95		mA
COMP source current limit	I_{COMP_SOLI}	1V < COMP < 2.9V	123	153	183	μA
COMP sink current limit	I_{COMP_SILI}	1V < COMP < 2.9V	12.5	18.5	24.5	μA
Current Dimming						
PWM input low threshold	V_{PWM_LO}	V_{PWM} falling			0.4	V
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.2			V
PWM pull-down resistor	R_{PWM}			500		kΩ
Mixed dimming transfer point		DIMT1:0 bits = 00b		6.25		%
Current up/down slope	t_{STEP}	TSLP2:0 bits = 011b		16		μs
I²C-set PWM dimming frequency	f_{PWM}	FPWM3:0 bits = 0110b		26		kHz
Phase shift		8 channels PWM dimming		45		°
LED Current Regulator						
LEDx regulation voltage	V_{HD}	I_{LED} = 20mA		470		mV
Current matching (5)		I_{LED} = 20mA			2.5	%
Full-scale current		ISET7:0 bits = 4Eh	14.93	15.29	15.65	mA

ELECTRICAL CHARACTERISTICS *(continued)*

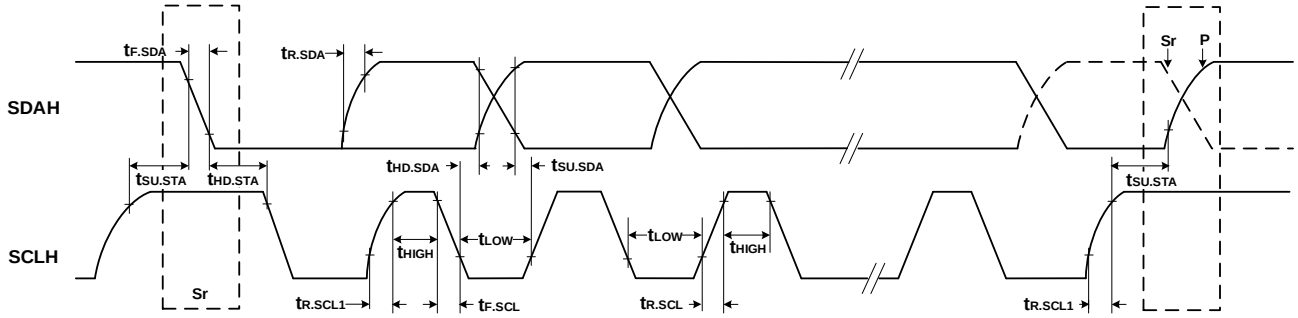
V_{IN} = 6V, V_{EN} = 2V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protection						
Over-voltage protection threshold	V_{OVP}	Rising edge, OVP1:0 bits = 10b	36.5	38	39.5	V
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails	1.12	1.22	1.32	V
LEDx over-voltage threshold	V_{LEDX_OV}	LEDS1:0 bits = 10b		7.5		V
LEDx over-voltage fault timer		f_{SW} = 1.2MHz		6.9		ms
LEDx UVLO threshold	V_{LEDX_UV}		55	80	105	mV
Thermal shutdown threshold	T_{ST}	Rising edge		150		°C
		Hysteresis		20		°C
FF pull-down resistor	R_{FF}			90		Ω
I²C Interface						
Input logic low	V_{IL}				0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				1200	kHz
Set-up time for repeated start condition	$t_{SU.STA}$		160			ns
Hold time for repeated start condition	$t_{HD.STA}$		160			ns
SCLH clock low time	t_{HIGH}		160			ns
SCLH clock high time	t_{LOW}		60			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$		0 (6)		70	ns
SCLH clock rising time	$t_{R.SCL}$		10		40	ns
Rising time of the SCLH clock after a repeated start and acknowledge bit	$t_{R.SCL1}$		10		80	ns
SCLH clock falling time	$t_{F.SCL}$		10		40	ns
SDAH data rising time	$t_{R.SDA}$		10		80	ns
SDAH data falling time	$t_{F.SDA}$		10		80	ns
Set-up time for stop condition	$t_{SU.STO}$		160			ns
Capacitance bus for each bus line	C_B (7)				400	pF

Notes:

5) Matching is defined as the difference between the maximum and minimum currents divided by 2 times the average current.
6) A device must interally provide a data hold time to bridge the undefined part between VIL and VIH of the SCLH signal falling edge. To minimize the hold time, design an input circuit with the lowest possible threshold for the SCLH signal falling edge.
7) If C_B is between 100pF and 400pF for the bus line load, the timing parameters must be increased linearly.

I²C TIMING DIAGRAM



Sr: Repeated Start Condition
P: Stop Condition

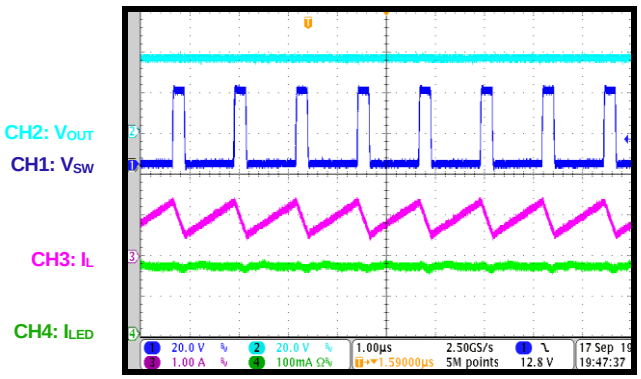
Figure 3: I²C-Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7V, 13 LEDs in series, 8 strings, 20mA/string, L = 10µH, T_A = 25°C, unless otherwise noted.

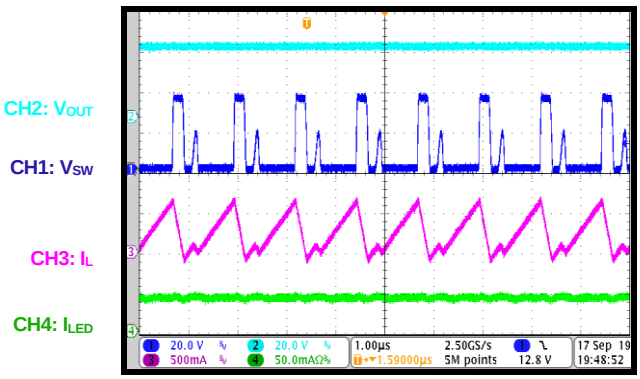
Analog Dimming Mode

Steady state



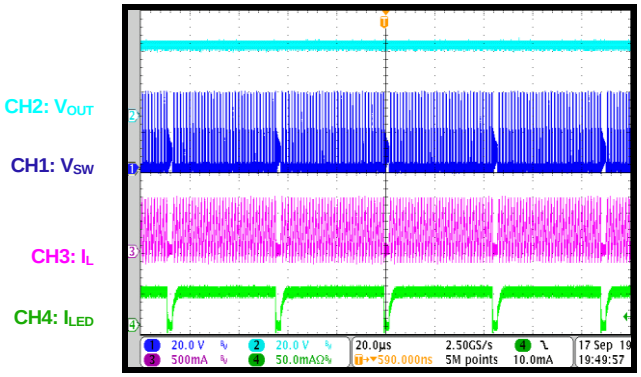
Mixed Dimming Mode

With 25% transfer point, D_{PWM} = 25%

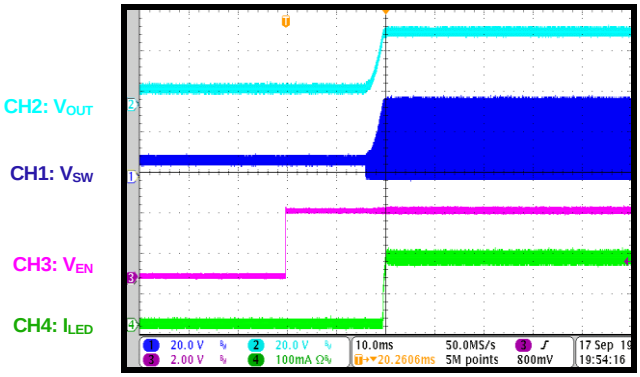


Mixed Dimming Mode

With 25% transfer point, D_{PWM} = 24%

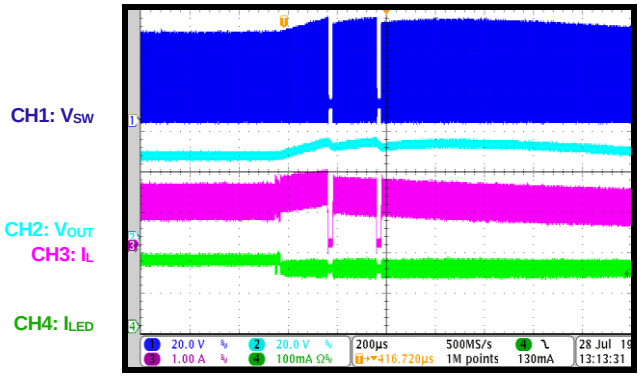


EN Start-Up



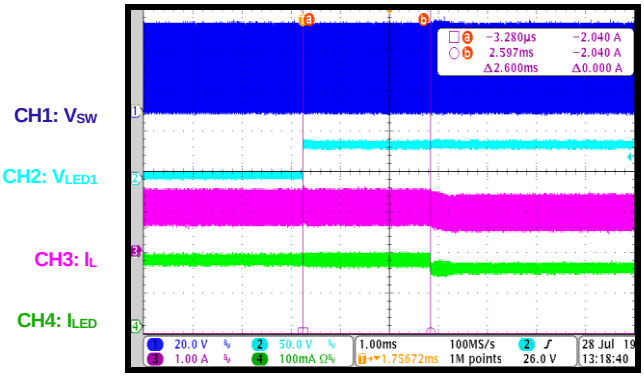
Open LED Protection

V_{OVP} = 45V



Short LED Protection

Short channel LED1

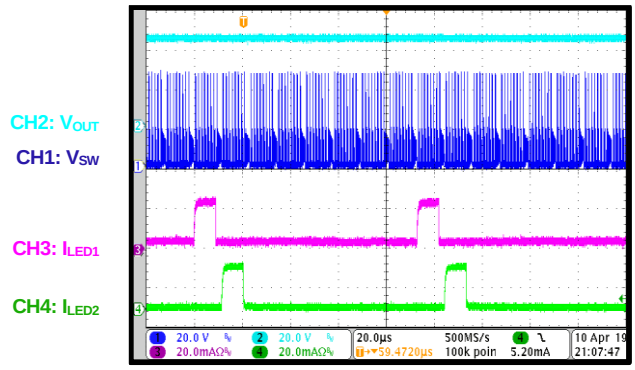


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 7V, 13 LEDs in series, 8 strings, 20mA/string, L = 10µH, T_A = 25°C, unless otherwise noted.

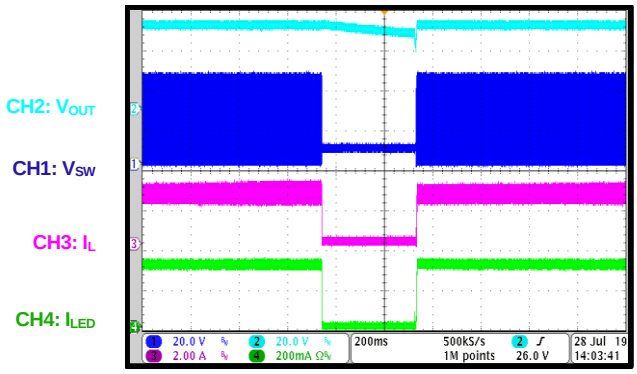
Phase Shift Function

Direct PWM dimming, each channel phase shift, PWM duty = 10%, filed = 10.42kHz

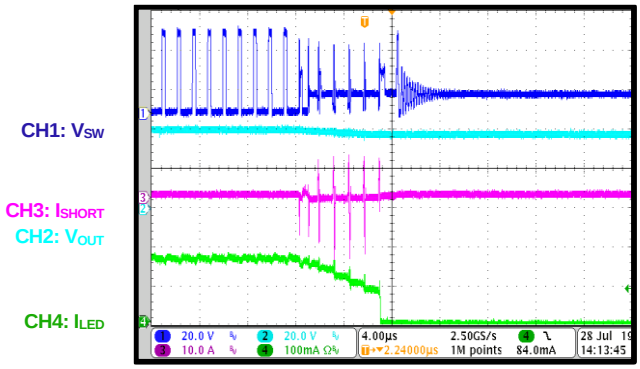


Thermal Protection

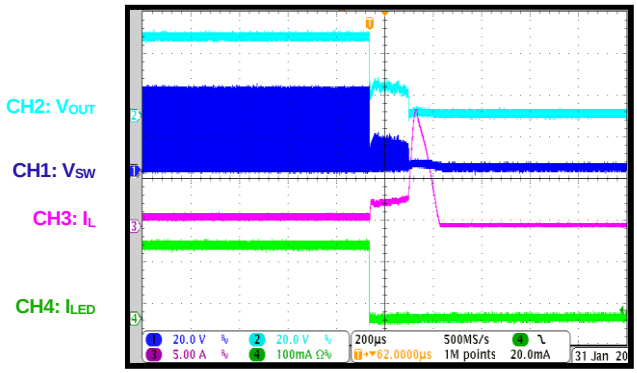
40mA/string



Short Inductor Protection



Short VOUT to GND Protection



FUNCTIONAL BLOCK DIAGRAM

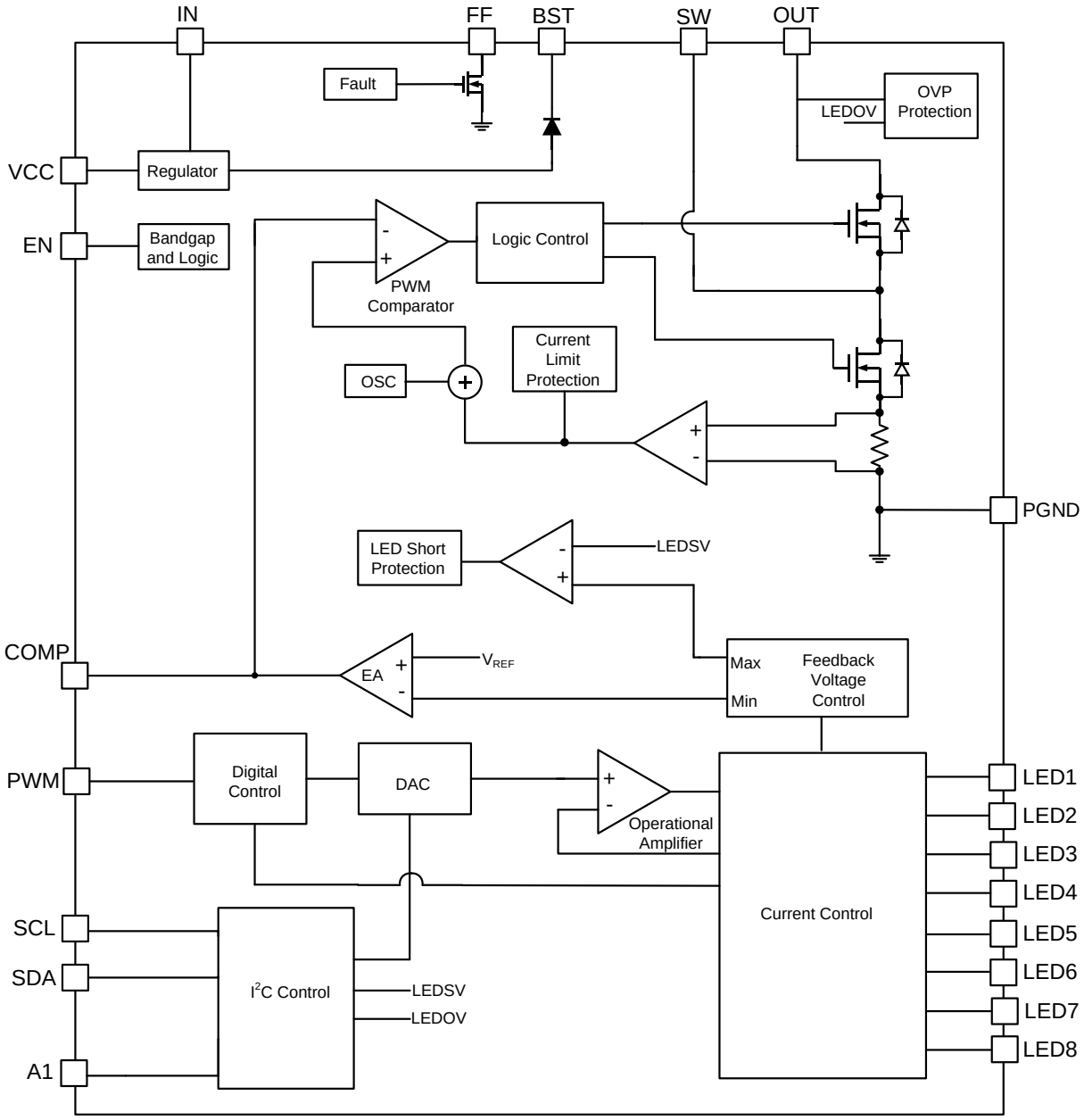


Figure 4: Functional Block Diagram

OPERATION

The MP3372 is a configurable, constant-frequency, peak current mode step-up converter with up to eight channels of regulated current sources to drive an array of white LEDs. The MP3372 provides a fully integrated solution that saves PCB size and total solution cost. For easy use, an I²C interface is integrated into the IC.

Internal 4.9V Regulator

The MP3372 includes an internal linear regulator (VCC). If V_{IN} exceeds 6V, this regulator outputs a 4.9V power supply to the internal MOSFET gate driver and internal control circuitry. V_{CC} drops to 0V when the chip shuts down. The MP3372 is disabled until V_{CC} exceeds the under-voltage lockout (UVLO) threshold.

Internal Clock

The MP3372 has a fixed 10MHz clock for the internal timer and counter to achieve a high dimming resolution.

Boost Converter Switching Frequency

The boost converter switching frequency can be set by FS2:0 (01h, bits[2:0]). It can be set to 350kHz, 500kHz, 650kHz, 800kHz, 950kHz, 1.2MHz, 1.8MHz, or 2.4MHz.

Automatic Switching Frequency

To optimize efficiency in the different loads during analog dimming, the MP3372 can select the switching frequency automatically by comparing the I_{LED} amplitude with the threshold programmed register 06H. If D4~2 = 001, the I²C sets the default f_{SW}, which can have the following values:

- If I_{LED} > 10mA, f_{SW} = 1.2MHz
- If I_{LED} < 10mA, f_{SW} = 650kHz
- If I_{LED} < 5mA, f_{SW} = 350kHz

If f_{SW} is below the f_{SW} set through the automatic switching frequency function, the lower f_{SW} value is maintained.

System Start-Up

When enabled, the MP3372 checks the topology connection. The IC monitors the output voltage (V_{OUT}) to determine if the output is shorted to GND. If the output voltage is below 1.2V, the IC is disabled. The MP3372 continues to check other safety limits, such as LED open and over-voltage protection (OVP). If all protection tests pass, the IC begins boosting the step-up converter with an internal soft start.

The MP3372 can start up properly, regardless of the order in which VIN, PWM, and EN turn on. To achieve a quick response, the recommended start-up sequence is:

- Turn VIN on
- Turn EN on (wait for 2ms)
- Send I²C data (optional)
- PWM dimming signal

If the dimming is set by the I²C interface, the PWM signal can be ignored (see Figure 5).

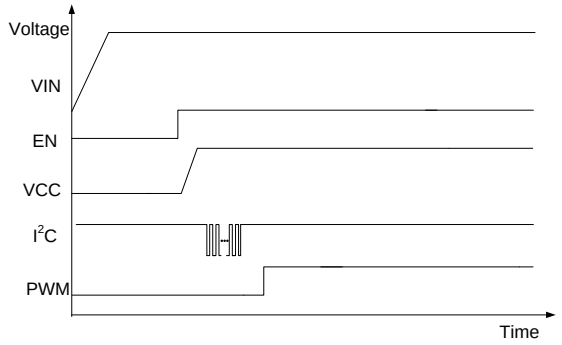


Figure 5: Recommended Start-Up Sequence

Step-Up Converter

The MP3372 uses peak current mode control to regulate the output voltage. At the beginning of each switching cycle, the internal clock turns on the low-side N-channel MOSFET. In normal operation, the minimum turn-on time is around 100ns. A stabilizing ramp is added to the output of the current-sense amplifier to prevent subharmonic oscillations for duty cycles greater than 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage of the error amplifier, the low-side MOSFET turns off.

The output voltage of the error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter automatically chooses the lowest active LEDx voltage as the feedback voltage to

regulate the output voltage high enough to power all of the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. This results in increased current flowing through the MOSFET as well as increased power delivery to the output, which forms a closed loop that regulates the output voltage.

Pulse-Skipping Mode

In light-load operation (especially when V_{OUT} is almost equal to V_{IN}), the converter runs in pulse-skipping mode, in which the MOSFET turns on for a minimum on time. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. When the chip stops switching, the output capacitor discharges to the power LED string. The device begins switching until the output voltage requires another boost.

Full-Scale Current Setting

The LED full-scale current can be set by ISET7:0 (00h, bits[15:8]). It can be set between 0mA and 50mA with 0.196mA per step.

Dimming Control

The MP3372 can provide flexible dimming methods based on the dimming mode setting shown below, including analog dimming, PWM dimming and mixed dimming mode (see Figure 6, Figure 7, and Figure 8). Each mode can control the brightness via the PWM input signal or I²C interface.

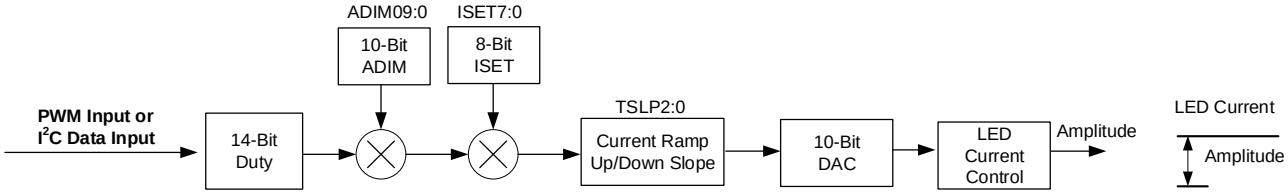


Figure 6: Analog Dimming Mode Flowchart

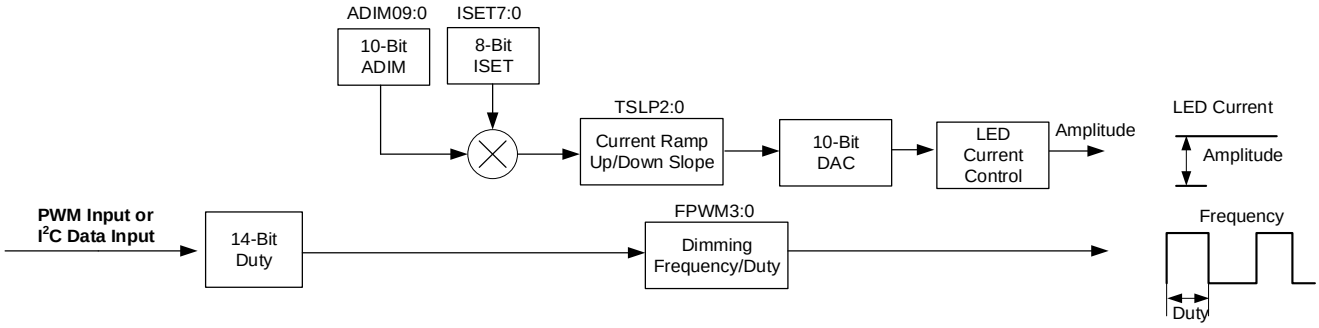


Figure 7: PWM Dimming Mode Flowchart

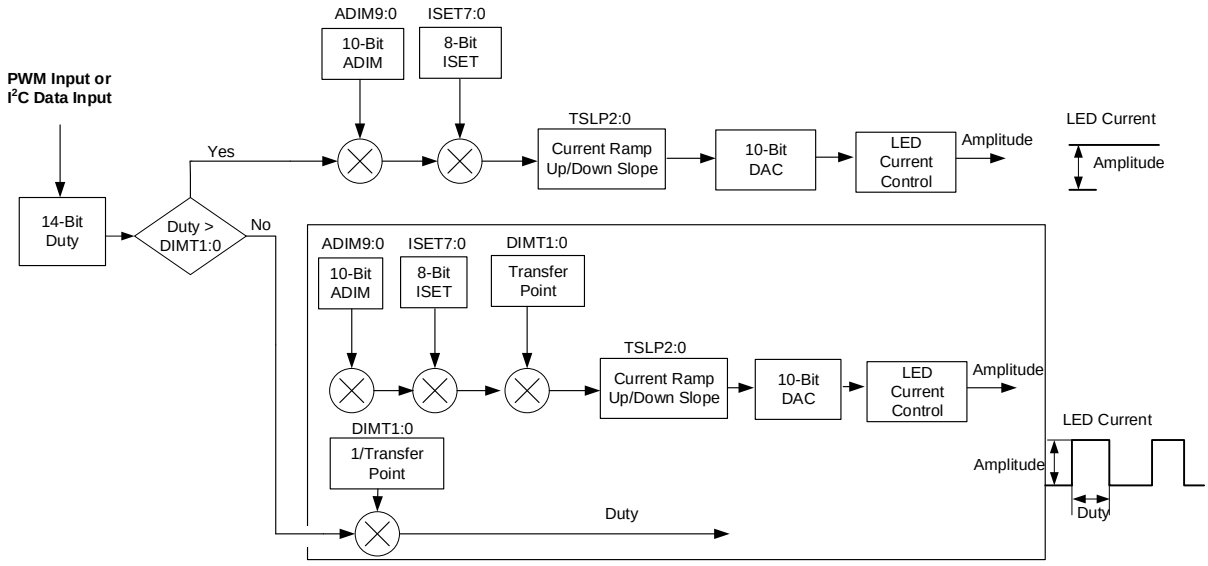


Figure 8: Mixed Dimming Mode Flowchart

The MP3372 has six types of dimming modes, described below.

1. Analog dimming mode from the PWM input: MOD2:0 (01h, bits[6:4]) = 000b. In analog dimming mode, the LED current amplitude depends on the duty cycle of the PWM input signal.

   Note that the current amplitude can be changed via ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 9).

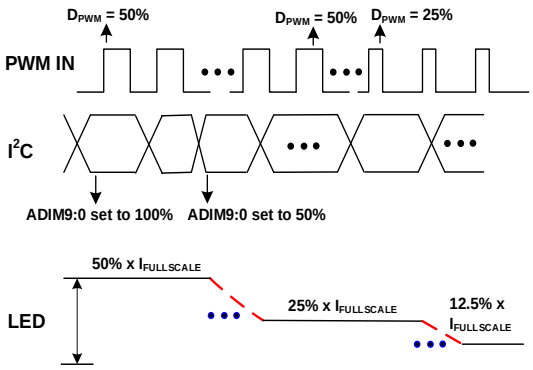


Figure 9: Analog Dimming from PWM Input

2. Analog dimming mode via the I²C interface: MOD2:0 = 001b. In analog dimming mode, the LED current amplitude is set via PWM13:0 (04h, bits[13:0]).

   Note that the current amplitude can be changed via ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 10).

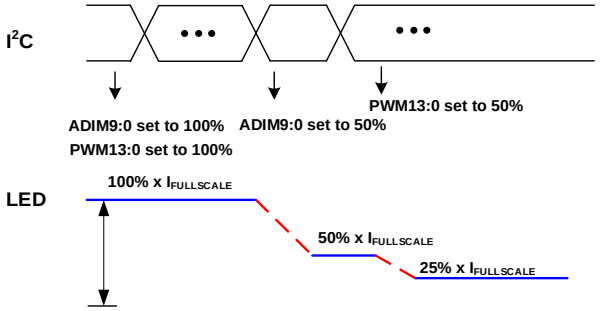


Figure 10: Analog Dimming from I²C Interface

3. PWM dimming mode from the PWM pin: MOD2:0 = 010. In this mode, the LED current is chopped as a PWM waveform. The PWM frequency is set via FPWM3:0 (03h, bits[5:2]). The duty cycle depends on the calculated value from the signal of the PWM pin.

   Note that the current amplitude can be changed via ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 11).

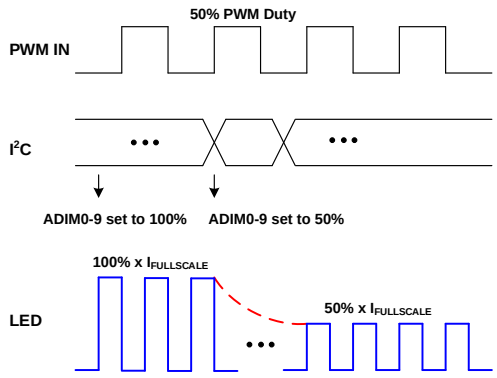


Figure 11: PWM Dimming from PWM Input

4. PWM dimming mode from the register PWM: MOD2:0 = 011. In this mode, the LED current is chopped as a PWM waveform. The PWM frequency is set via FPWM3:0 (03h, bits[5:2]), and the duty cycle is set via PWM13:0 (01h, bits[6:4]).

   Note that the current amplitude can be changed via ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 12).

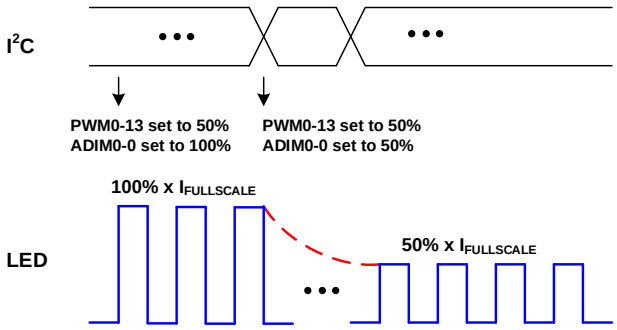


Figure 12: PWM Dimming from I²C Interface

5. Mixed dimming mode from the PWM input: MOD2:0 = 100b. If the duty cycle from the PWM exceeds the threshold set via DIMT1:0 (03h, bits[1:0]) in mixed dimming mode, the IC works in analog dimming mode. The LED current amplitude follows the input duty. If the duty cycle from the PWM input drops below the threshold set via DIMT1:0, the IC works in PWM dimming mode, and the PWM LED current frequency is set by FPWM3:0 (03h, bits[5:2]). The PWM LED current duty is extended according to the selected transfer point.

   For example, if the transfer point is 25%, then the PWM LED current duty = PWM input duty x 1 / (25%). The PWM LED current amplitude is fixed to the value at the transfer point set by DIMT1:0.

   Note that the current amplitude can be changed by register ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 13).

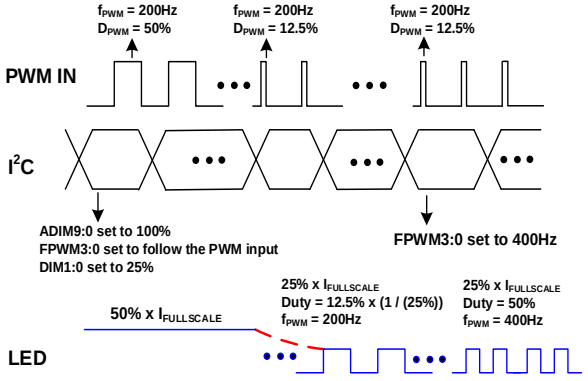


Figure 13: Mixed Dimming from PWM Input

6. Mixed dimming mode from the I²C interface: MOD2:0 = 101b. If the duty cycle from PWM13:0 exceeds the threshold set by DIMT1:0 (03h, bits[1:0]) in mixed dimming mode, the IC works in analog dimming mode. The LED current amplitude follows what is set by PWM13:0 (04h, bits[13:0]). If the duty cycle from PWM13:0 is below the threshold set by DIMT1:0, the IC works in PWM dimming mode and the PWM frequency is set by FPWM3:0 (03h, bits[5:2]). The PWM LED current duty is extended according to the selected transfer point.

   For example, if the transfer point is 25%, then the PWM LED current duty = duty set by PWM13:0 x 1 / (25%). The PWM LED current amplitude is fixed to the value at the transfer point duty set by DIMT1:0.

   Note that the current amplitude can be changed by ADIM9:0 (02h, bits[9:0]) (10-bit value) (see Figure 14).

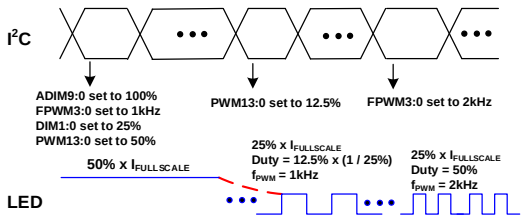


Figure 14: Mixed Dimming from the I²C Interface

Phase Shift PWM Dimming

To reduce inrush current and audible noise during PWM dimming, a phase shift function is integrated in the MP3372.

If the internal PS1:0 register (06h, bits[1:0]) is configured through the I²C, the phase shift function operates in PWM dimming mode (including PWM dimming in mixed dimming mode). The shifted phase can be calculated with Equation (1):

$$\text{Phase}(^\circ) = \frac{360}{n}(^\circ) \quad (1)$$

Where *n* is the number of used LED channels.

The unused LEDx pins should be connected to GND. In phase-shift mode, the unused channels must be disabled in the descending order of channel numbers. For example, if six strings are employed in an application, then channels 8 and 7 should be disabled.

If PS1:0 = 00, then each channel is phase shifted. If all eight channels are used, the shifted phase is 45°. LED2 lags behind LED1 by 45° (see Figure 15).

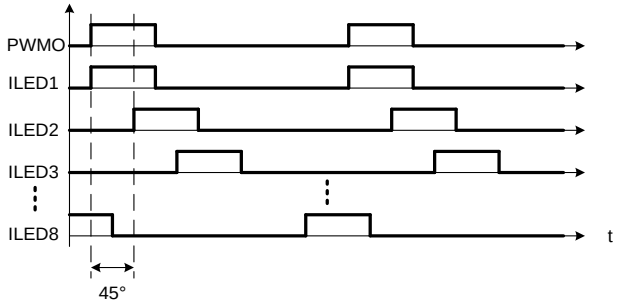


Figure 15: Phase Shift with 8 Channels

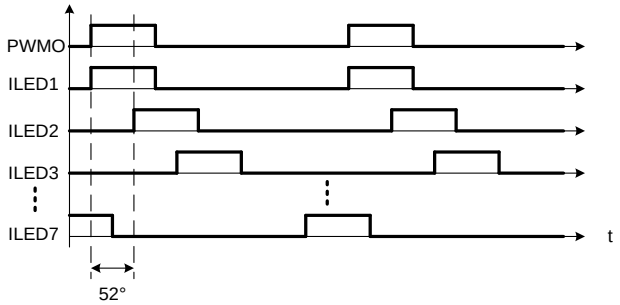


Figure 16: Phase Shift with 7 Channels (Connect LED8 to GND)

If PS1:0 = 10, LED1 and LED2 are tied together, LED3 and LED4 are tied together, and so on. In this mode, LED1 and LED2 have the same phase and connect to one channel. LED1/2 lags behind LED3/4 by 90° if four channels are used (see Figure 17).

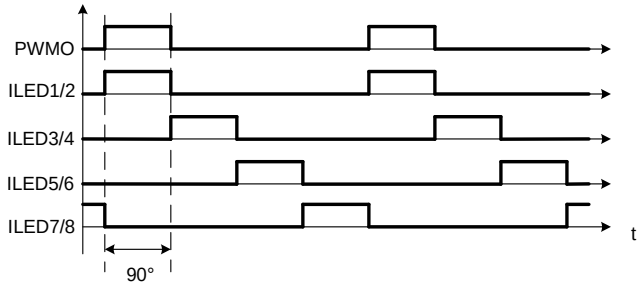


Figure 17: Phase Shift with 4 Channels

Figure 18 shows the phase shift function when 3 channels are enabled. In this case, the shifted phase is 120°.

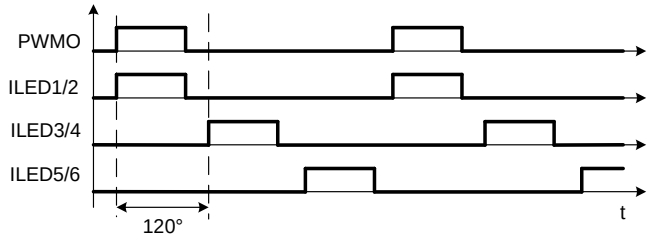


Figure 18: Phase Shift with 3 Channels (Connect LED7/8 to GND)

If PS1:0 (06h, bits[1:0]) = 11, tie LED1–4, then LED5–8 together. In this mode, LED1–4 have the same phase and are connected to one channel. LED1–4 lags behind LED5–8 by 90° if two channels are used (see Figure 19).

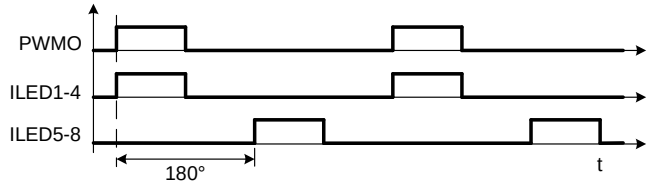


Figure 19: Phase Shift with 2 Channels

Linear Dimming for Fade In/Out

The MP3372 provides linear current rising up or down. The LED current ramps up or down linearly. The current ramp-up or ramp-down slope can be set by TSLP2:0 (03h, bits[10:8]), from 2μs to 128μs (0.049mA for each step).

Deep Dimming Ratio

To provide enough output energy for the LED load when the PWM LED current duty is very small, the MP3372 provides at least four switching cycles to guarantee sufficient output voltage before the next PWM LED current on duty cycle. This way, the MP3372 can achieve a wide dimming ratio range in PWM dimming mode. The dimming ratio depends on the LED current dimming frequency and LED current source turn-on/-off time. The lower the PWM dimming frequency, the deeper the dimming ratio.

For the MP3372, it is recommended that the minimum on time of the LED string exceed 1.5µs to achieve good dimming. The dimming ratio can reach 100:1 at 22kHz in mixed dimming mode.

Unused LED Channel Setting

The MP3372 can detect an unused LED string automatically and remove it from the control loop during start-up by either connecting the unused LEDx pin to GND or by setting CHEN7:0 (00h, bits[7:0]) to 0.

Synchronous Rectifier

To save cost and reduce PCB size, the MP3372 works in synchronous rectifier mode by default. A 100nF ceramic capacitor and a 10Ω resistor in series between BST and SW is the best BST supply choice for the synchronous converter.

If f_{SW} > 950kHz or there is a high output power application, it is recommended to use an external rectifier to improve efficiency and thermal stability. To disable the internal synchronous rectifier, set SYNC (01h, bit[7]) to 0, and tie the SW and BST pins together.

Open-String Protection

Open-string protection is achieved by detecting the voltage on the OUT and LED1–8 pins. If one string is open during normal operation, the respective LEDx pin voltage is pulled low to ground, and the IC continues charging the output voltage until it reaches the over-voltage protection (OVP) threshold (set by OVP1:0 (01h, bits[9:8]). If the OVP point has been triggered, the chip stops switching and marks off the fault string that has an LEDx pin voltage below 80mV. Once marked, the remaining LED strings force the output voltage back to normal regulation. The string with the largest voltage drop determines the output regulation value.

Short String Protection

The MP3372 monitors the LEDx pin voltage to determine whether a short string fault has occurred. If one or more strings are shorted, the respective LEDx pins tolerate high voltage stress. If an LEDx pin voltage exceeds the protection threshold (set by LEDS1:0 (03h, bits[7:6])), an internal counter starts. If this fault condition lasts for 6.9ms (f_{SW} = 1.2MHz), the fault string is marked off and disabled. Once a string is marked off, it is disconnected from the output voltage loop until the part restarts. If all strings are shorted, the MP3372 shuts down the step-up converter until the power is restarted (the VIN supply is turned off and back on) or EN is toggled (EN is switched off then back on).

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding the current stress rating, the IC uses cycle-by-cycle current limit protection. The limit value can be selected by ILIM (01h, bit[3]). If the current exceeds the current limit value, the IC stops switching until the next clock cycle begins.

Latch-Off Current Limit Protection

To avoid device damage caused by a large current rating (such as inductor or diode shorts), the MP3372 uses latch-off current limit protection. This protection is triggered if the current flowing through the low-side MOSFET (LS-FET) reaches the threshold (3.5A) within 200ns and remains for five switching cycles.

Thermal Protection

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented by detecting the silicon die temperature. If the die temperature exceeds the upper threshold (T_{ST}), the MP3372 shuts down. The device resumes normal operation when the die temperature drops below the lower threshold. The typical hysteresis value is 20°C.

I²C Interface Register Description

Read/write the registers after EN has been ready for at least 2ms.

I²C Chip Address

The 7-bit MSB device address is 0x28/0x29. After the start condition is received, the I²C-compatible master sends a 7-bit address followed by an 8th read (1) or write (0) bit (see Figure 20).

The following bit indicates the register address to or from which the data is written or read. The A1 pin can program the IC address. Float A1 for 0x29, or connect A1 to GND for 0x28. This means that two MP3372 chips can share the same I²C interface.

0	1	0	1	0	0	A1	R/W

Figure 20: I²C-Compatible Device Address

REGISTER MAP

Add	D15	D14	D13	D12	D11	D10	D9	D8
00H	ISET7	ISET6	ISET5	ISET4	ISET3	ISET2	ISET1	ISET0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00H	CHEN7	CHEN6	CHEN5	CHEN4	CHEN3	CHEN2	CHEN1	CHEN0

Add	D15	D14	D13	D12	D11	D10	D9	D8
01H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OVP1	OVP0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01H	SYNC	MOD2	MOD1	MOD0	ILIM	FS2	FS1	FS0

Add	D15	D14	D13	D12	D11	D10	D9	D8
02H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADIM9	ADIM8
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02H	ADIM7	ADIM6	ADIM5	ADIM4	ADIM3	ADIM2	ADIM1	ADIM0

Add	D15	D14	D13	D12	D11	D10	D9	D8
03H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TSLP2	TSLP1	TSLP0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
03H	LEDS1	LEDS0	FPWM3	FPWM2	FPWM1	FPWM0	DIMT1	DIMT0

Add	D15	D14	D13	D12	D11	D10	D9	D8
04H	RESERVED	RESERVED	PWM13	PWM12	PWM11	PWM10	PWM9	PWM8
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
04H	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0

Add	D15	D14	D13	D12	D11	D10	D9	D8
05H	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
05H	RESERVED	RESERVED	RESERVED	FT_OTP	FT_OCP	FT_OVP	FT_LEDO	FT_LEDS

Add	D15	D14	D13	D12	D11	D10	D9	D8
06H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Add	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
06H	RESERVED	RESERVED	RESERVED	AFS2	AFS1	AFS0	PS1	PS0

Note:

8) Registers 0x00~0x05 (write) have one-time programmability for customization.

Table 1: Full-Scale and Channel Enable Register

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:8	ISET7:0	R/W	0x62	LED full-scale current-setting bits. These bits set the maximum current for each channel. 0.196mA/step. 0x00: 0mA 0x62: 19.22mA 0x66: 20mA 0xFF: 50mA
7:0	CHEN7:0	R/W	0x3F	LED current source enable bits. These bits control the respective internal LED current sources. CHEN0: 1: LED current source 1 is enabled 0: LED current source 1 is disabled CHEN1: 1: LED current source 2 is enabled 0: LED current source 2 is disabled CHEN2: 1: LED current source 3 is enabled 0: LED current source 3 is disabled CHEN3: 1: LED current source 4 is enabled 0: LED current source 4 is disabled CHEN4: 1: LED current source 5 is enabled 0: LED current source 5 is disabled CHEN5: 1: LED current source 6 is enabled 0: LED current source 6 is disabled CHEN6: 1: LED current source 7 is enabled 0: LED current source 7 is disabled CHEN7: 1: LED current source 8 is enabled 0: LED current source 8 is disabled

Table 2: Dimming Mode and Parameter Setting Register

Addr: 0x01				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:10	RESERVED	R	Reserved	Reserved.
9:8	OVP1:0	R/W	10b	These bits set the output voltage over-voltage protection (OVP) threshold. 00: 24V 01: 31V 10: 37.5V 11: 46V
7	SYNC	R/W	1b	This bit sets the boost converter rectifier operation mode. 0: The IC works in Asynchronous mode 1: The IC works in synchronous mode
6:4	MOD2:0	R/W	100b	These bits set the LED current dimming mode. 000: The MP3372 operates in analog dimming mode through the external PWM input signal. The LED current amplitude changes with the input PWM duty 001: The MP3372 operates in analog dimming mode through the I²C interface. The LED current amplitude changes with PWM13:0 (04h, bits[13:0]) 010: The MP3372 operates in internal PWM dimming mode. The signal from the PWM pin determines the LED current duty cycle 011: The MP3372 operates in internal PWM dimming mode, and the value from PWM13:0 determines the LED current duty cycle 100: The MP3372 operates in mixed dimming mode through the external PWM input signal. If the input PWM duty exceeds the transfer point, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. DIMT1:0 (03h, bits[1:0]) determines the transfer point for mixed dimming mode 101: The MP3372 operates in mixed dimming mode through the I²C interface. If the duty set by PWM13:0 exceeds the transfer point, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. DIMT1:0 determines the transfer point for mixed dimming mode
3	ILIM	R/W	1b	The bit sets the inductor cycle-by-cycle current limit for the converter. 0: 1.8A current limit 1: 2.5A current limit
2:0	FS2:0	R/W	010b	These bits sets the boost converter's switching frequency. 000: 350kHz 001: 500kHz 010: 650kHz 011: 800kHz 100: 950kHz 101: 1.2MHz 110: 1.8MHz 111: 2.4MHz If f_{SW} > 950kHz, use Asynchronous mode.

Table 3: Analog Dimming Register

Addr: 0x02				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:10	RESERVED	R	Reserved	Reserved.
9:0	ADIM9:0	R/W	0x3FF	Analog dimming bits. These bits only control the LED current with 0.098% per step. They are also valid in any dimming mode. 0x000: 0% 0x001: 0.098% … 0x3FF: 100%

Table 4: Slope and PWM Dimming Frequency Register

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:11	RESERVED	R	Reserved	Reserved.
10:8	TSLP2:0	R/W	011b	LED current ramp-up/-down slope bit. 000: 2μs per step 001: 4μs per step 010: 8μs per step 011: 16μs per step 100: 32μs per step 101: 64μs per step 110: 128μs per step 111: N/A
7:6	LEDS1:0	R/W	01b	These bits sets the LED short protection threshold. 00: 2.5V 01: 5V 10: 7.5V 11: 10V
5:2	FPWM3:0	R/W	1010b	These bits set the LED current dimming frequency when the device is in PWM dimming or mixed dimming mode. 0000: Follow external PWM dimming signal (direct PWM dimming) 0001: 200Hz 0010~0101: Reserved 0110: 26.04kHz 0111: 22.32kHz 1000: 19.53kHz 1001: 17.36kHz 1010: 15.63kHz 1011: 14.20kHz 1100: 13.02kHz 1101: 12.02kHz 1110: 11.16kHz 1111: 10.42kHz
1:0	DIMT1:0	R/W	10b	These bits set the transfer point in mixed dimming mode. If the dimming duty exceeds this threshold, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. 00: 6.25% 01: 12.5% 10: 25% 11: 50%

Table 5: Internal I²C Dimming Register

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:14	Reserved	R	Reserved	Reserved.
13:0	PWM13:0	R/W	0x0000	LED current dimming duty setting bits via the I²C interface. This setting controls the LED current dimming duty when MOD2:0 (01h, bits[6:4]) is set to 001b or 101b. 0.006% per step. 0x0000: 0% 0x0001: 0.006% 0x3FFF: 100%

Table 6: ID and Fault Register

Addr: 0x05				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:8	ID7:0	R	00010001b	Device ID bits.
7:5	RESERVED	R	Reserved	Reserved.
4	FT_OTP	R	0b	This bit indicates if an over-temperature protection (OTP) fault has occurred. After it is read, this bit latches off and resets to 0. 0: No OTP fault has occurred 1: An OTP fault has occurred
3	FT_OCP	R	0b	This bit indicates if an over-current protection (OCP) fault has occurred. After it is read, this bit latches off and resets to 0. 0: No OCP fault has occurred 1: An OCP fault has occurred
2	FT_OVP	R	0b	This bit indicates if an over-voltage protection (OVP) fault has occurred. After it is read, this bit latches off and resets to 0. 0: No OVP fault has occurred 1: An OVP fault has occurred
1	FT_LEDO	R	0b	LED current source open fault indication bit. After it is read, this bit latches off and resets to 0. 0: No LED current source open fault has occurred 1: An LED current source open fault has occurred
0	FT_LEDS	R	0b	LED short fault indication bit. After it is read, this bit latches off and resets to 0. 0: No LED shout fault has occurred 1: An LED shout fault has occurred

Table 7: Auto-Switching Register

Addr: 0x06				
Bit	**Bit Name**	**Access**	**Default**	**Description**
15:5	RESERVED	R/W	Reserved	Reserved.
4:2	AFS	R/W	000b	These bits sets the automatic switching frequency adjustment threshold. 000: Disabled 001: 10mA = 650kHz, 5mA = 350kHz (>10mA = 1.2MHz, <5mA = 350kHz, other = 650kHz) 010: 8mA = 650kHz, 3mA = 350kHz 011: 5mA = 650kHz, 2mA = 350kHz 100~111: Reserved
1:0	PS1:0	R/W	00b	Phase shift function setting. 00: No phase shifts 01: Each channel phase shifts 10: Tie LED1/2 , LED3/4, LED5/6, LED7/8 channels together for phase shifting 11: Tie the LED1–4 then LED5–8 channels together for phase shifting

APPLICATION INFORMATION

Selecting the Switching Frequency

The switching frequency of the step-up converter is set by FS2:0 (see Table 2 on page 21).

Setting the LED Current

The LED string full-scale current is set by ISET7:0 (see Table 1 on page 20), between 0mA and 50mA, with 0.196mA per step.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply, as well as the switching noise from the device. The input capacitor impedance at the switching frequency should be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 4.7µF ceramic capacitor is sufficient.

Selecting the Inductor

The MP3372 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger-value inductor results in less ripple current, lower peak inductor current, and reduced stress on the internal N-channel MOSFET. However a larger value inductor also has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance.

Calculate the required inductance value with Equation (2):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (2)$$

Where V_{OUT} is the output voltage, f_{SW} is the switching frequency, D is the switching duty, I_{LOAD} is the LED load current, and η is the efficiency.

The switching duty can be calculated with Equation (3):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (3)$$

Where V_{IN} is the input voltage.

With a given inductor value, the inductor DC current rating should be at least 40% greater than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible to improve efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR. For most applications, a 2.2µF ceramic capacitor is sufficient.

Setting the Over-Voltage Protection (OVP) Threshold

The output over-voltage protection (OVP) threshold is set by OVP1:0 (see Table 2 on page 21).

PCB Layout Guidelines

Careful attention must be given to the PCB layout and component placement. Efficient placement of the high-frequency switching path is critical to prevent noise and electromagnetic interference. For the best results, follow the guidelines below:

1. Keep the loop between SW, PGND, the external diode (D1, if required), and the output capacitor (C1, C2) as short as possible, since the loop flows with a high-frequency pulse current.
2. Place a ceramic capacitor close to the input and VCC, since they are susceptible to noise.

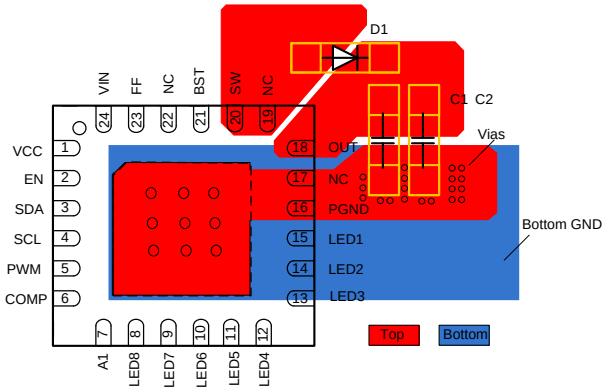


Figure 21: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

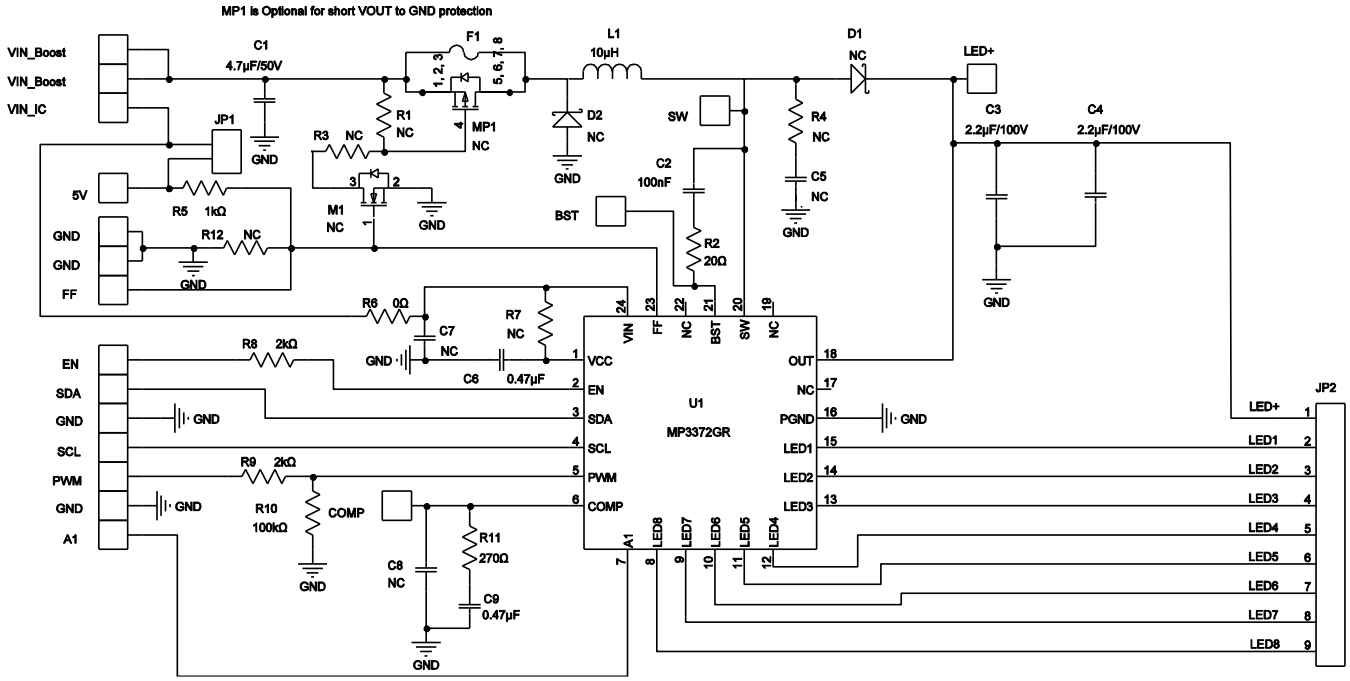


Figure 22: Typical Application Circuit

TYPICAL APPLICATION CIRCUITS *(continued)*

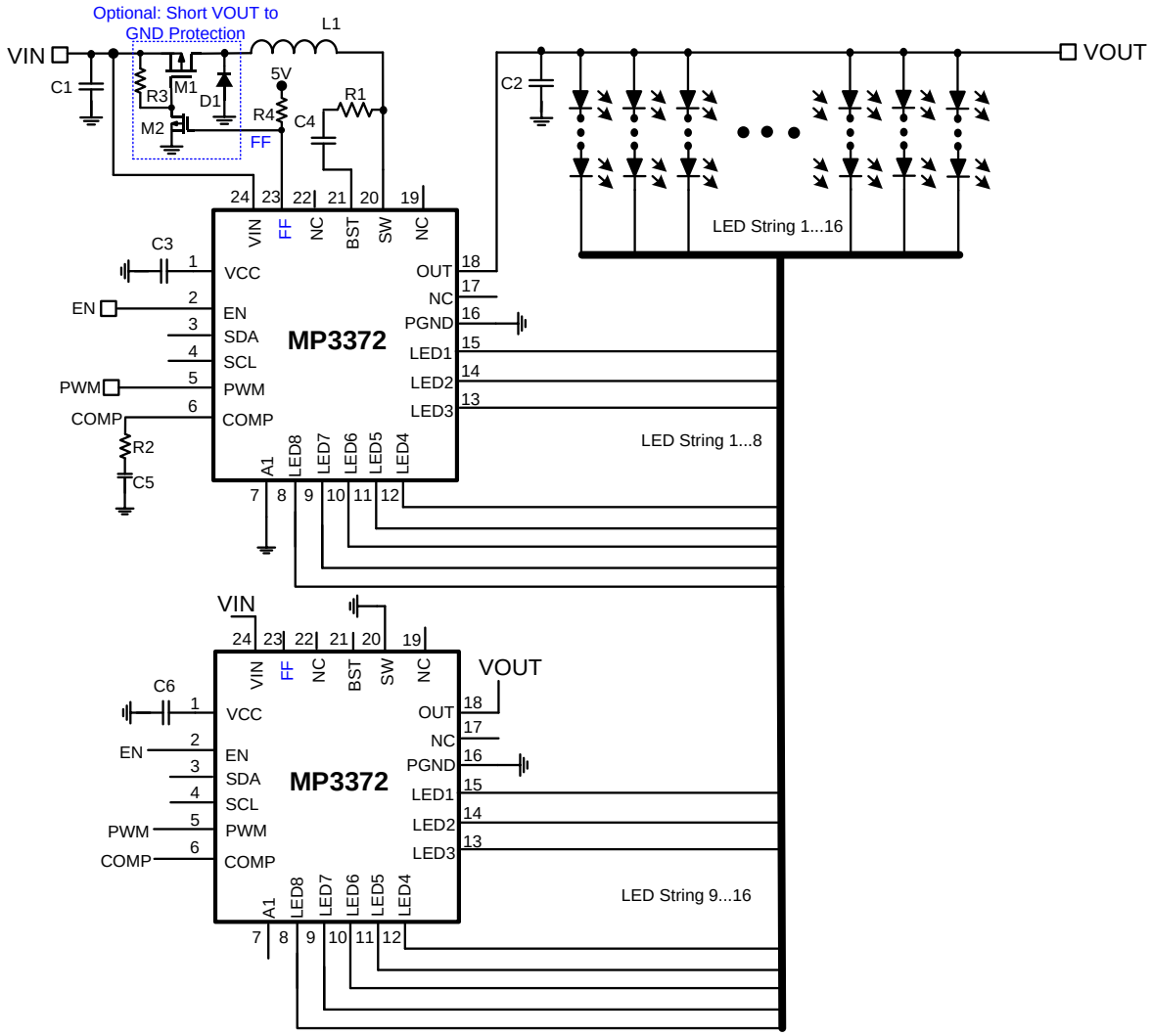
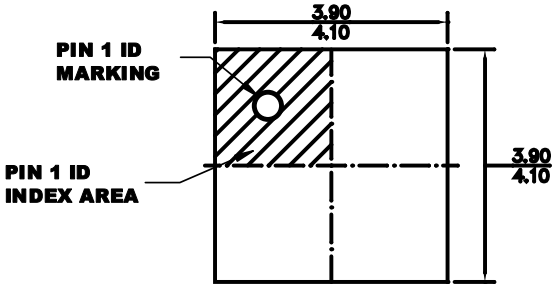


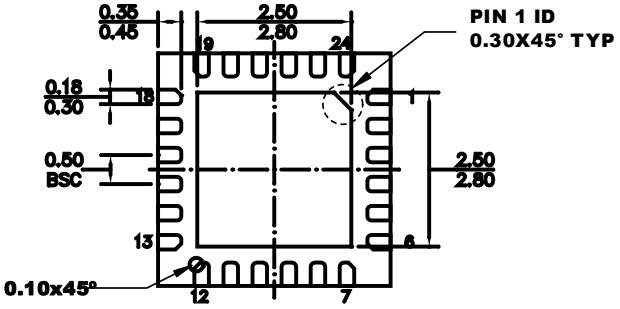
Figure 23: Typical Cascade Application Circuit during Analog Dimming and Direct PWM Dimming

PACKAGE INFORMATION

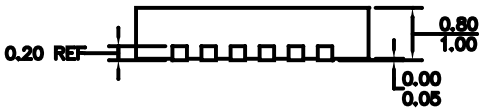
QFN-24 (4mmx4mm)



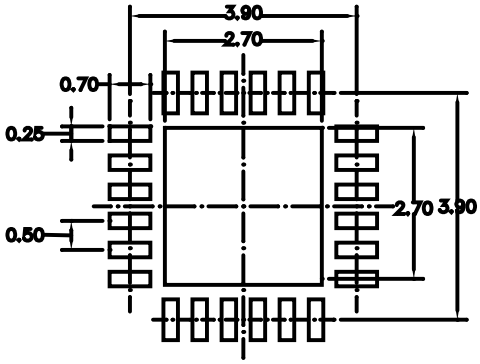
TOP VIEW



BOTTOM VIEW



SIDE VIEW

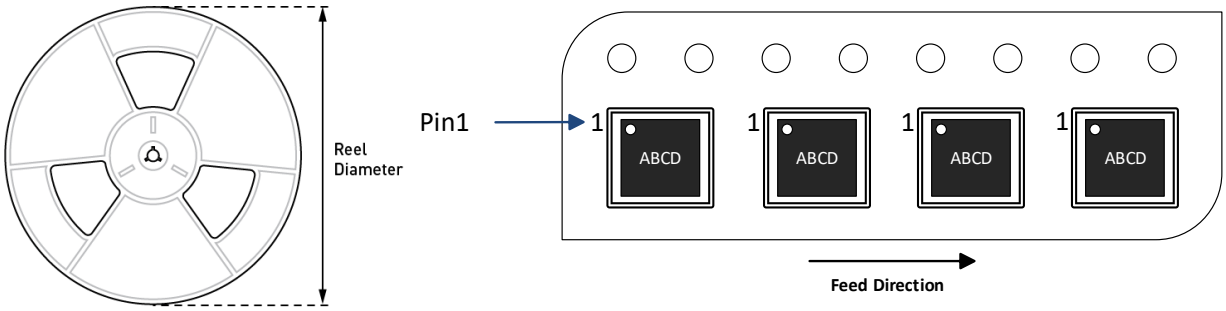


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3372GR-0001-C741–Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	X/XX/XXXX	Initial Release	-