HV7355

8-Channel High-Speed Unipolar 1.5A 150V Ultrasound Pulser

Features

- High-Density Integrated Ultrasound Transmitter
- 0V to +150V Output Voltage
- ±1.5A Minimum Source and Sink Current
- ±300 mA Current in CW Mode
- Up to 18 MHz Operating Frequency
- Matched Delay Times
- Built-in Gate Driver Floating Voltage Regulator
- 2.5V to 3.3V CMOS Logic Interface

Applications

- Portable Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-Destructive Testing
- Pulse Waveform Generator

General Description

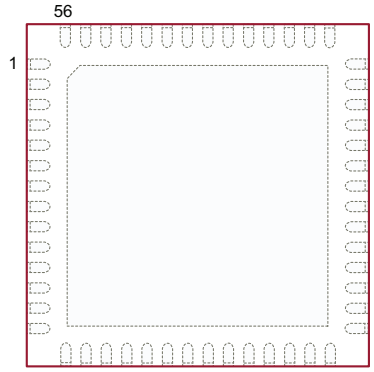
The HV7355 is an 8-channel unipolar high-voltage high-speed pulse generator. It is designed for medical ultrasound applications. This high-voltage and high-speed integrated circuit can also be used for other piezoelectric, capacitive or MEMS sensors in ultrasonic non-destructive detection and sonar ranger applications.

The HV7355 consists of a controller logic interface circuit, level translators, MOSFET gate drivers and high-current P-channel and N-channel MOSFETs as the output stage for each channel.

The output stages of each channel are designed to provide peak output currents of ±1.5A for pulsing, when MC = 1, with up to 150V swings. When MC = 0, all the output stages drop the peak current to ±500 mA for low-voltage CW mode operation to save power. This direct coupling topology of the gate driver not only saves one high-voltage capacitor per channel but also makes the PCB layout easier.

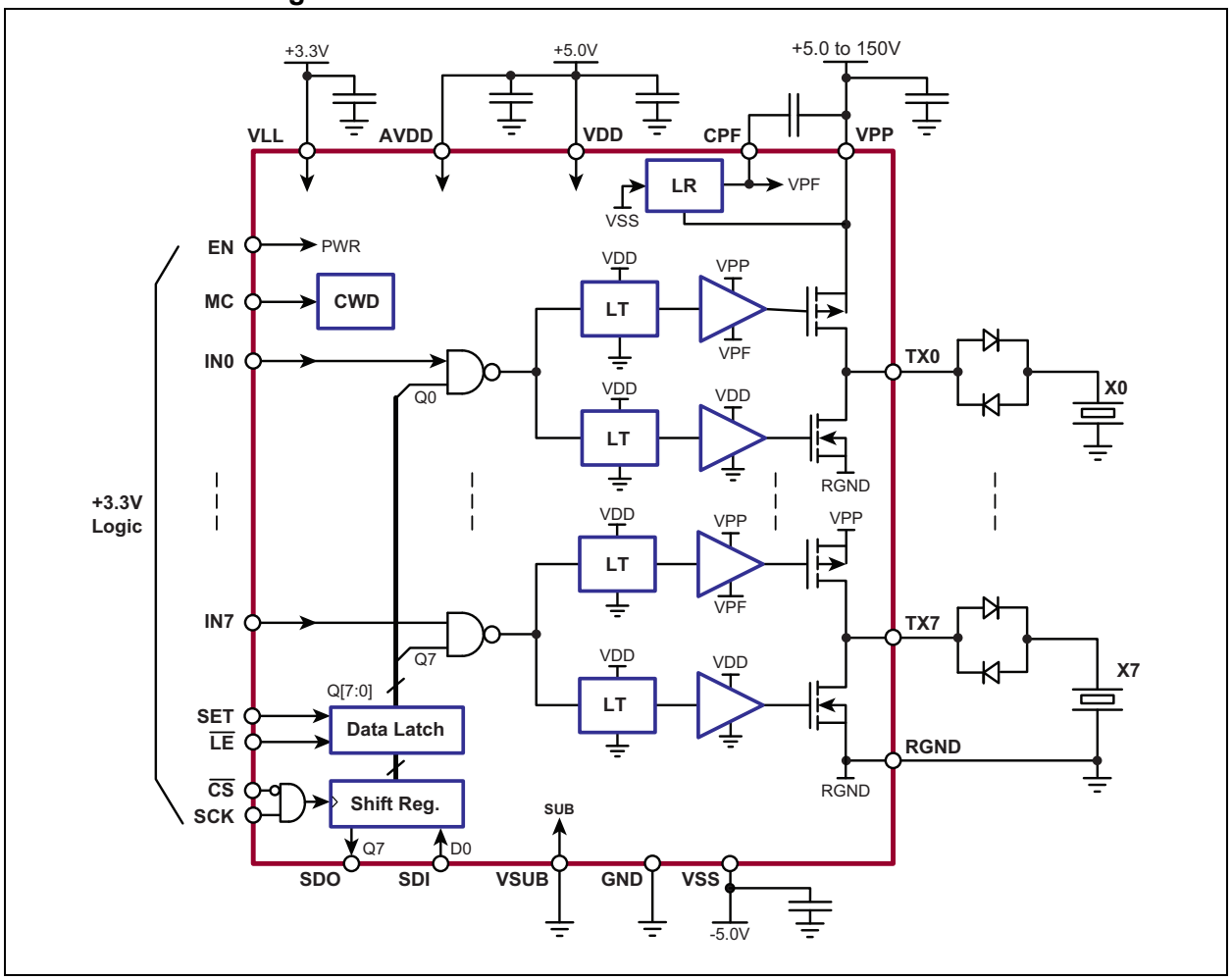
Package Type

56-lead (8 X 8) VQFN
(Top view)

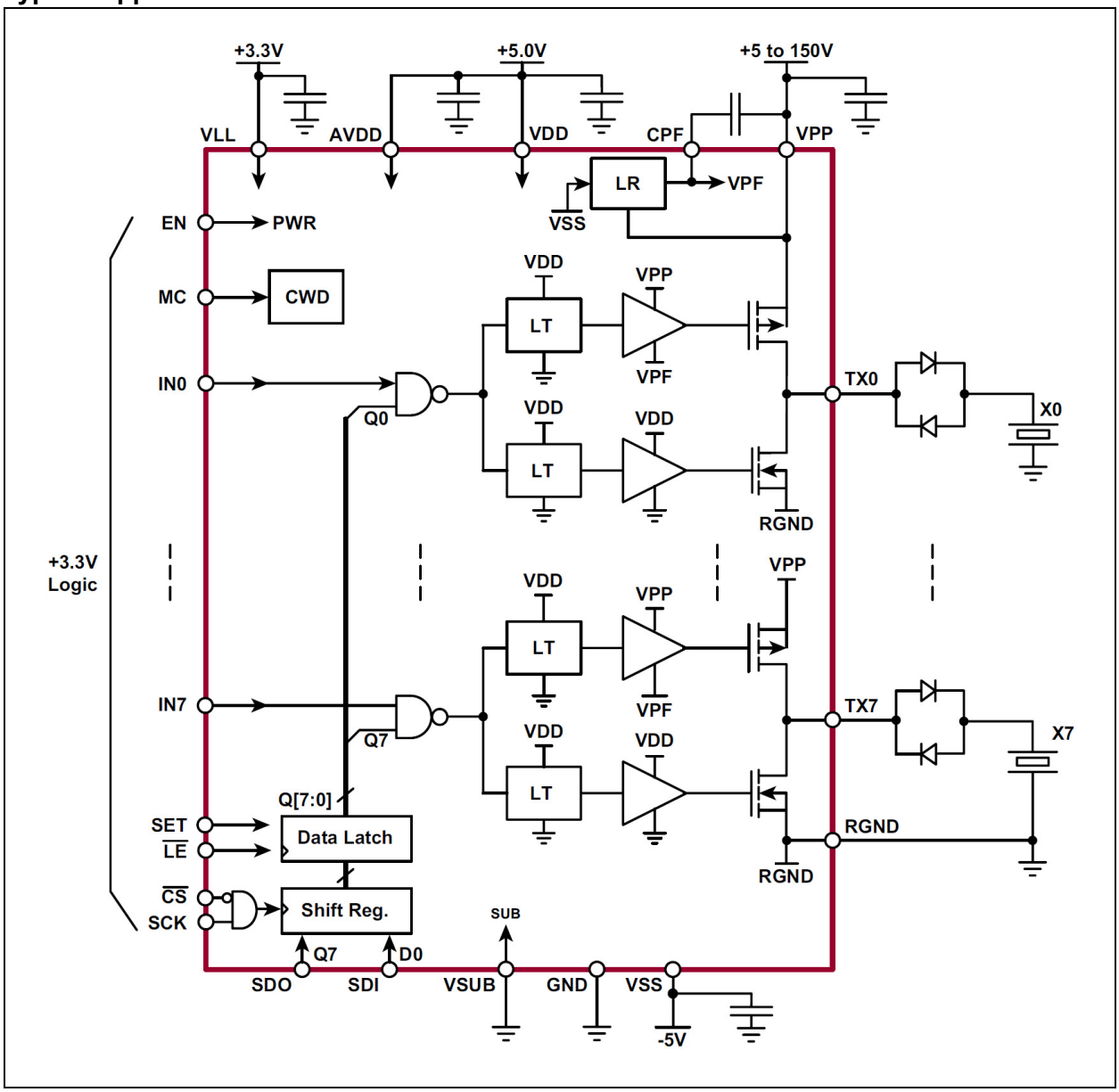


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

GND, RGND, and Substrate Voltage, V_{SUB} 0V
Positive Logic Supply, V_{LL} ..... –0.5V to +7V
Positive Logic and Level Translator Supply, V_{DD} ..... –0.5V to +7V
Negative Level Translator and LR Supply, V_{PP} ..... +0.5V to –7V
High-voltage Positive Supply, V_{PP} ..... –0.5V to +160V
V_{PP}–V_{TXx} Voltage ..... –0.5V to +160V
V_{TXx}–RGND Voltage ..... –0.5V to +160V
All Logic Input PIN_X, NIN_X and EN Voltages ..... –0.5V to +7V
Operating Junction Temperature, T_J ..... –40°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
ESD Rating (**Note 1**) ..... ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

OPERATING SUPPLY VOLTAGES AND CURRENT (EIGHT ACTIVE CHANNELS)

Electrical Specifications: V_{LL} = +3.3V, V_{ADD} = V_{DD} = +5V, V_{SS} = –5V, V_{PP} = +150V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Voltage Reference	V_{LL}	2.37	3.3	3.47	V	
Internal Voltage Supply	V_{DD}	4.5	5	5.5	V	
Positive Gate Driver Supply Voltage	V_{PP}	V_{DD}	—	+150	V	
Negative Low-Voltage Supply Voltage	V_{SS}	–5.5	–5	–4.5	V	
Gate Driver Floating Voltage	V_{PF}	—	5	—	V	
V_{LL} Current EN = Low	I_{LL}	—	2	10	µA	
V_{DD} Current EN = Low	I_{DDQ}	—	50	150	µA	f = 0 MHz
V_{DD} Current EN = High	I_{DDEN}	—	1	4	mA	f = 0 MHz
V_{DD} Current MC = High	I_{DDEN}	—	160	—	mA	f = 5 MHz, continuous, no load
V_{DD} Current MC = Low	I_{DDENCW}	—	12	—	mA	
V_{SS} Current EN = Low	I_{SSQ}	—	5	20	µA	
V_{SS} Current EN = High	I_{SSEN}	—	1	4	mA	f = 0 MHz
V_{SS} Current MC = High	I_{SSEN}	—	95	—	mA	f = 5 MHz, continuous, no load
V_{SS} Current MC = Low	I_{SSENCW}	—	50	—	mA	
V_{PP} Current EN = Low	I_{PPQ}	—	2	10	µA	
V_{PP} Current EN = High	I_{PPEN}	—	200	450	µA	f = 0 MHz
V_{PP} Current MC = High	I_{PPEN}	—	370	—	mA	f = 5 MHz, continuous, no load
V_{PP} Current MC = Low	I_{PPENCW}	—	300	—	mA	

UNDERVOLTAGE AND OVERTEMPERATURE PROTECTION

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Threshold	V_{UVDD}	3.4	—	4.4	V	Internal only
V_{LL} Threshold	V_{UVLL}	—	1.7	—	V	Internal only
V_{PP}–V_{PF} Threshold	V_{UVPF}	2.5	—	3.8	V	Internal only

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{LL} = +3.3V, V_{ADD} = V_{DD} = +5V, V_{SS} = –5V, V_{PP} = +150V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
P-CHANNEL MOSFET OUTPUT, TX0-7						
Output Saturation Current	I_{OUT}	1.4	1.6	—	A	MC = 1
Channel Resistance	R_{ON}	—	8	—	Ω	I_{SD} = 100 mA
Output Saturation Current	I_{OUT}	0.5	—	—	A	MC = 0
Channel Resistance	R_{ON}	—	18	—	Ω	I_{SD} = 100 mA
N-CHANNEL MOSFET OUTPUT, TX0-7						
Output Saturation Current	I_{OUT}	1.5	1.7	—	A	MC = 1
Channel Resistance	R_{ON}	—	3	—	Ω	I_{SD} = 100 mA
Output Saturation Current	I_{OUT}	0.5	—	—	A	MC = 0
Channel Resistance	R_{ON}	—	18	—	Ω	I_{SD} = 100 mA
LOGIC INPUT						
Input Logic High Voltage	V_{IH}	(V_{LL}–0.4)	—	V_{LL}	V	
Input Logic Low Voltage	V_{IL}	0	—	0.4	V	
Input Logic High Current	I_{IH}	—	—	1	µA	
Input Logic Low Current	I_{IL}	–1	—	—	µA	
Input Logic Capacitance	C_{IN}	—	—	5	pF	**Note 1**

Note 1: For design guidance only

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{LL} = +3.3V, V_{ADD} = V_{DD} = +5V, V_{SS} = –5V, V_{PP} = +150V, T_A = 25°C unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Data Rise or Fall Maximum Time	t_{inrf}	—	—	10	ns	**Note 1**
Output Rise Time	t_r	—	24	—	ns	330 pF//2.5 kΩ load (See **Timing Waveforms**.)
Output Fall Time	t_f	—	24	—	ns	
Output Frequency Range	f_{OUT}	—	—	18	MHz	100Ω resistor load, V_{PP} = +90V (**Note 1**)
Initial Enable Time	t_{EN-ON}	—	150	200	µs	2 µF on each CPF pin to 90% of V_{CPF}
Output Disable Time	t_{EN-OFF}	—	2	5	µs	At 5 MHz CW
Delay Time on Inputs Rise	t_{dr}	—	5	—	ns	V_{PP} = 25V 1Ω resistor load, 50% to 50% (See **Timing Waveforms**.)
Delay Time on Inputs Fall	t_{df}	—	5	—	ns	
Delay on Mode Change	t_{dm}	—	50	70	ns	
Delay Time Matching	Δt_{DELAY}	—	±2	—	ns	P to N, channel to channel
Delay Jitter on Rise or Fall	t_j	—	15	—	ps	(**Note 1**)

Note 1: For design guidance only

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{LL} = +3.3V, V_{ADD} = V_{DD} = +5V, V_{SS} = –5V, V_{PP} = +150V, T_A = 25°C unless otherwise indicated.

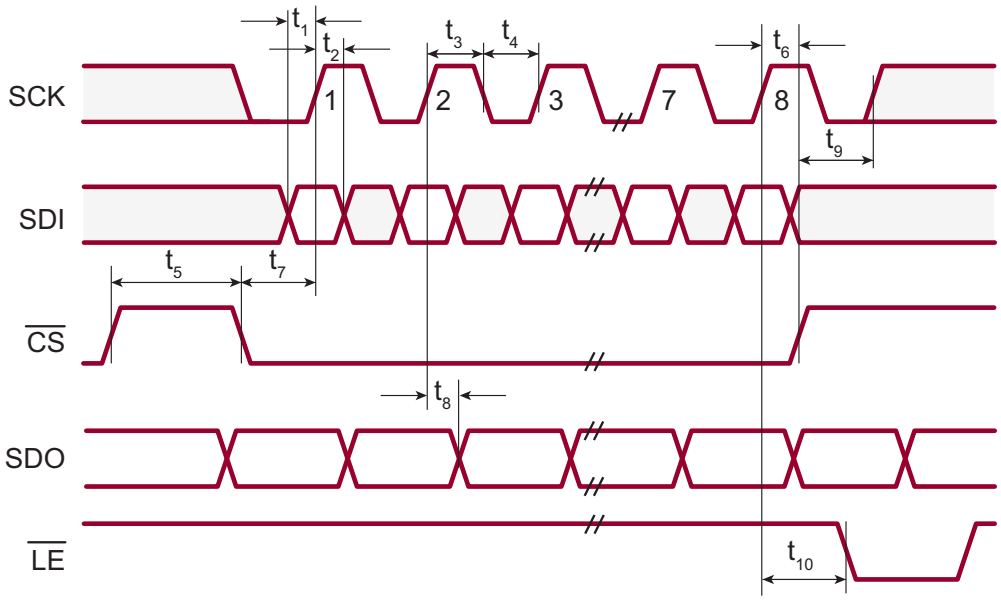
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
SERIAL DATA INTERFACE TIMING CHARACTERISTICS						
Serial Clock Maximum Frequency	f_{SCK}	25	—	—	MHz	All from/to 50% rise or fall edges (See **Timing Waveforms**.) (**Note 1**)
SDI Valid to SCK Setup Time	t_1	0	2	—	ns	
SDI Valid to SCK Hold Time	t_2	4	—	—	ns	
SCK High Time	t_3	9	—	—	ns	
SCK Low Time	t_4	9	—	—	ns	
$\overline{CS}$ Pulse Width	t_5	9	—	—	ns	
SCK High to $\overline{CS}$ High	t_6	7	—	—	ns	
$\overline{CS}$ Low to SCK High	t_7	7		—	ns	
SDO Delay from SCK Rise Edge	t_8	—	6.5	—	ns	SDO with 100 pF to GND
$\overline{CS}$ High to SCK Rise Edge	t_9	7	—	—	ns	All from/to 50% rise or fall edges (See **Timing Waveforms**.) (**Note 1**)
SCK High to $\overline{LE}$ Low	t_{10}	7	—	—	ns	

Note 1: For design guidance only

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
56-lead (8 X 8) VQFN	θ_{JA}	—	21	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV7355 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	IN0	Input control for channels 0 to 7
2	IN1	
3	IN2	
4	IN3	
5	IN4	
6	IN5	
7	IN6	
8	IN7	
9	$\overline{CS}$	Serial interface enable, active low
10	SDI	Serial Shift register data input, MSB(D7) first, LSB(D0) last
11	$\overline{LE}$	Latch enable, active low
12	SCK	Serial Shift register clock
13	SDO	Serial Shift register data output
14	SET	Set latch data Q[7:0] = 1, regardless the Shift register inputs or LE, active high
15	MC	Output Current mode control pin (See Table 3-3.)
16	VLL	Logic high-voltage reference input (+3.3V)
17	VSS	Negative power supply(–5V)
18	CPF	Gate driver floating voltage decoupling capacitor to VPP
19	VPP	Positive high-voltage power supply (+150V)
20	VPP	Positive high-voltage power supply (+150V)
21	VPP	Positive high-voltage power supply (+150V)
22	VPP	Positive high-voltage power supply (+150V)
23	VDD	Positive voltage supply for gate drivers (+5V)
24	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
25	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
26	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
27	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
28	TX7	Output for channels 0 to 7
29	TX7	
30	TX6	
31	TX6	
32	TX5	
33	TX5	
34	TX4	
35	TX4	
36	TX3	
37	TX3	
38	TX2	
39	TX2	
40	TX1	
41	TX1	
42	TX0	
43	TX0	
44	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
45	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
46	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
47	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
48	VDD	Positive voltage supply for gate drivers (+5V)
49	VPP	Positive high-voltage power supply (+150V)
50	VPP	Positive high-voltage power supply (+150V)
51	VPP	Positive high-voltage power supply (+150V)
52	VPP	Positive high-voltage power supply (+150V)
53	CPF	Gate driver floating voltage decoupling capacitor to VPP
54	GND	Logic input reference ground, 0V
55	AVDD	Positive internal voltage supply (+5V)
56	EN	Chip power enable, active high
VSUB (Thermal Pad)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to GND (0V) externally.

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV7355:

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	V_{SS}	1	EN and logic signal low
2	V_{LL} with logic signal low	2	V_{PP}
3	V_{DD}	3	V_{DD}
4	V_{PP}	4	V_{LL}
5	EN and logic signal go to high	5	V_{SS}

Note: Powering up or powering down in any arbitrary sequence will not damage the device. The power-up sequence and power-down sequence are only recommended to minimize possible inrush current.

TABLE 3-2: TRUTH FUNCTION TABLE (MC = X)

Logic Inputs			Output
EN	**Q[7:0]**	**IN0–7**	**TX0–7**
1	1111,1111	0	GND
1	1111,1111	1	VPP
1	0	X	GND
0	X	X	High-Z

TABLE 3-3: DRIVE MODE CONTROL TABLE

MC	I_{SC} (A)	R_{onP}	R_{onN}
0	0.5	18	13
1	1.6	8	3

Note: V_{PP} = +150V, V_{DD} = +5V, V_{LL} = +3.3V, V_{SS} = –5V, V_{SUB} = 0V

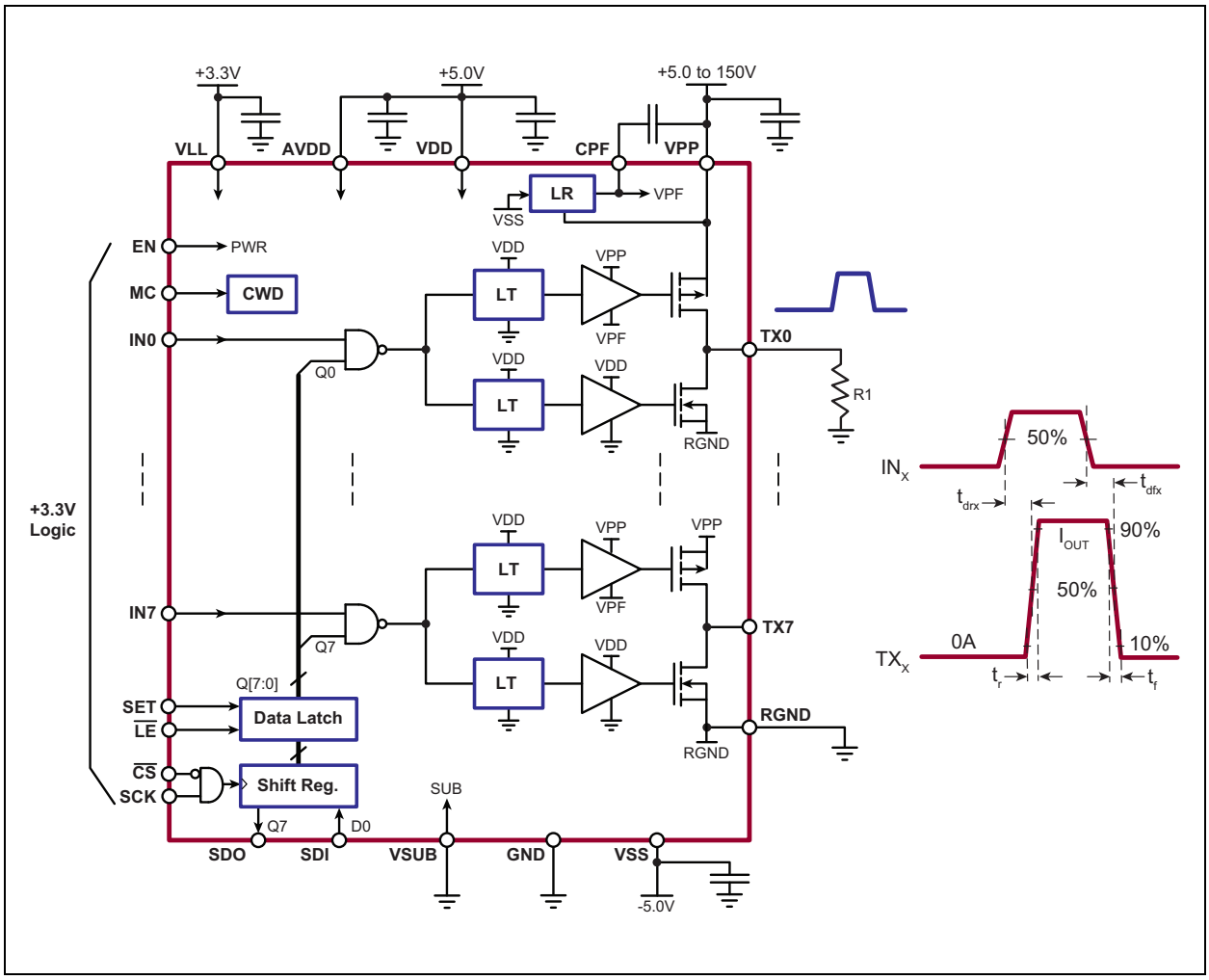


FIGURE 3-1: *Output Timing Test Diagram.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

56-lead QFN

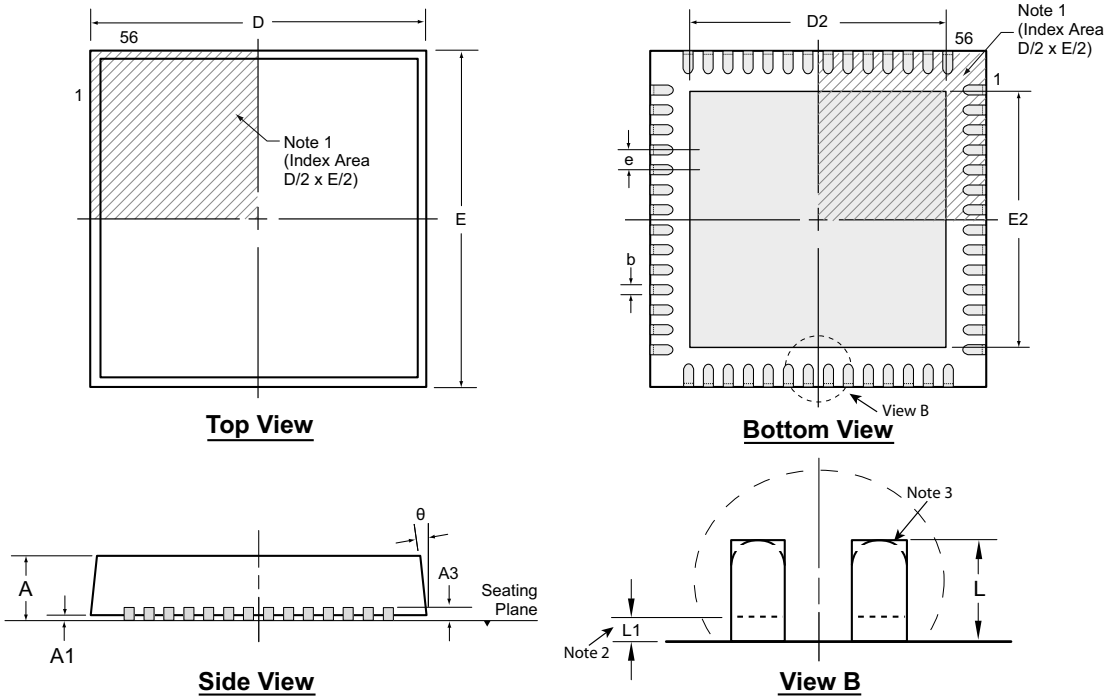
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

56-Lead QFN Package Outline (K6)

8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (November 2018)

- Converted Supertex Doc# DSFP-HV7355 to Microchip DS20005896A
- Removed “HVCMOS® Technology for high performance” in the Features section
- Changed the package marking format
- Removed the 56-lead QFN K6 M937 media type
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV7355	=	8-Channel High-Speed Unipolar 1.5A 150V Ultrasound Pulser
Package:	K6	=	56-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	250/Tray for a K6 Package

Example:

a) HV7355K6-G: 8-Channel High-Speed Unipolar 1.5A 150V Ultrasound Pulser, 56-lead VQFN, 250/Tray

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