DRV612 2-Vrms DirectPath™ Line Driver With Programmable-Fixed Gain

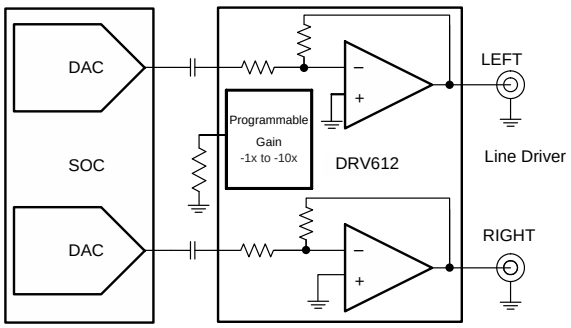
1 Features

- DirectPath™
  - Eliminates Pops and Clicks
  - Eliminates Output DC-Blocking Capacitors
  - 3-V to 3.6-V Supply Voltage
- Low Noise and THD
  - SNR > 105 dB at –1× Gain
  - Vn < 12 μVms, 20 Hz to 20 kHz at –1× Gain (Typical)
  - THD+N < 0.003% at 10-kΩ Load and –1× Gain
- 2-Vrms Output Voltage Into 600-Ω Load
- Single-Ended Input and Output
- Programmable Gain Select Reduces Component Count
  - 13× Gain Values
- Active Mute With More Than 80-dB Attenuation
- Short-Circuit and Thermal Protection
- ±8-kV HBM ESD-Protected Outputs

2 Applications

- PDP and LCD TVs
- DVD Players
- Mini and Micro Combo Systems
- Soundcards

Functional Block Diagram



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3 Description

The DRV612 is a single-ended, 2-Vrms stereo line driver designed to reduce component count, board space, and cost. It is ideal for single-supply electronics where size and cost are critical design parameters.

The DRV612 does not require a power supply greater than 3.3 V to generate its 5.6-V_{PP} output, nor does it require a split-rail power supply.

The DRV612 device is designed using TI's patented DirectPath technology, which integrates a charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased output. The DRV612 is capable of driving 2 Vms into a 600-Ω load. DirectPath technology also allows the removal of the costly output dc-blocking capacitors.

The device has fixed-gain single-ended inputs with a gain-select pin. Using a single resistor on this pin, the designer can choose from 13 internal programmable gain settings to match the line driver with the codec output level. The device also reduces the component count and board space.

Line outputs have ±8-kV HBM ESD protection, enabling a simple ESD protection circuit. The DRV612 has built-in active mute control with more that 80-dB attenuation for pop-free mute on/off control.

The DRV612 is available in a 14-pin TSSOP and 16-pin VQFN. For a footprint-compatible stereo headphone driver, see the TPA6139A2.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV612	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2011) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 1

Changes from Revision A (February 2011) to Revision B — **Page**

- Changed R_{IN} = 10 kΩ, R_{fb} = 20 kΩ To Gain = -2V/V in the Typical Characteristics condition text ... 7
- Changed R_{IN} = 10 kΩ, R_{fb} = 20 kΩ To Gain = -2V/V in the Typical Characteristics condition text ... 8

Changes from Original (December 2010) to Revision A — **Page**

- Added the QFN pinout drawing ... 3
- Added the QFN device to the Pin Functions table ... 3
- Changed minimum storage temperature from –40°C to –65°C ... 4
- Changed the Gain resistor 2% tolerance values in the Programmable Gain Settings table for Gain Steps and Input Impedance ... 6
- Changed Note 1 of the PROGRAMMABLE GAIN SETTINGS table From: If pin 12, GAIN, is left floating To: If the GAIN pin is left floating ... 6
- Changed From: C_{PUMP} = $C_{(VSS)}$ = 10 µF To: C_{PUMP} = $C_{(VSS)}$ = 1 µF in the Typical Characteristics condition text ... 7
- Changed From: C_{PUMP} = $C_{(VSS)}$ = 10 µF To: C_{PUMP} = $C_{(VSS)}$ = 1 µF in the Typical Characteristics condition text ... 8
- Changed the Gain_set RESISTOR values in Table 2 ... 14
- Changed the Gain_set RESISTOR values in Table 3 ... 15
- Removed references to DRV614 from the FOOTPRINT COMPATIBLE WITH TPA6139A2 section ... 16

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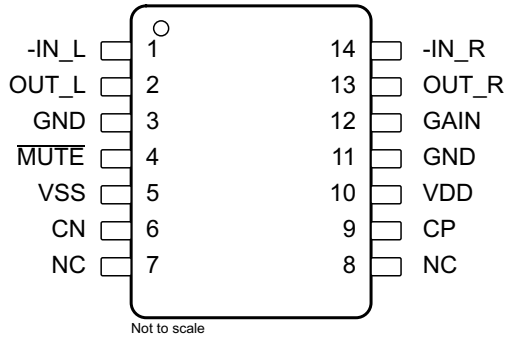
5 Device Comparison Table

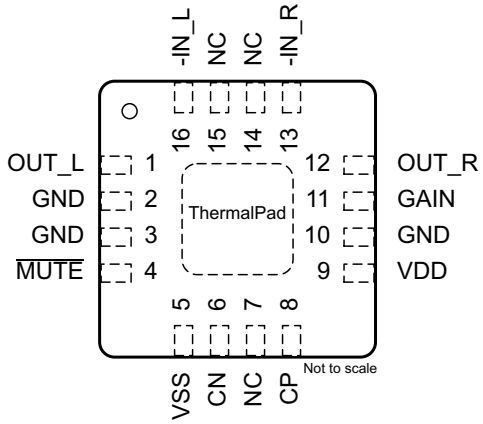
	GAIN	INPUT OFFSET (±) (uV)	Vmax (V)	Vmin (V)	PACKAGE (PIN)
DRV603	Adjustable	1000	5.5	3	TSSOP (14)
DRV604	Adjustable	500	3.7	3	HTSSOP (28)
DRV612	Adjustable	1000	4	3	TSSOP (14), VQFN (16)
DRV632	Adjustable	1000	4	3	TSSOP (14)

6 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	VQFN		
–IN_L	1	16	I	Negative input, left channel
–IN_R	14	13	I	Negative input, right channel
CN	6	6	I/O	Charge Pump flying capacitor negative connection
CP	9	8	I/O	Charge Pump flying capacitor positive connection
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See Table 2 for recommended resistor values.
GND	3, 11	2, 3, 10	P	Ground
$\overline{\text{MUTE}}$	4	4	I	MUTE, active low
NC	7, 8	7, 14, 15	—	No internal connection
OUT_L	2	1	O	Output, left channel
OUT_R	13	12	O	Output, right channel
Thermal Pad	—	Thermal Pad	P	Connect to ground
VDD	10	9	P	Supply voltage, connect to positive supply
VSS	5	5	O	Change Pump negative supply voltage

(1) I = Input, O = Output, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_I	VSS – 0.3	VDD + 0.3	V
	VDD to GND	–0.3	4	
	$\overline{\text{MUTE}}$ to GND	–0.3	VDD + 0.3	
Temperature	Maximum operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
DRV612 in the PW Package				
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except Pins 2 and 13	±4000	V
		Pins 2 and 13	±8000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
DRV612 in the RGT Package				
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except Pins 1 and 12	±4000	V
		Pins 1 and 12	±8000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

		MIN	NOM	MAX	UNIT
VDD	Supply voltage, DC	3	3.3	3.6	V
R_L	Load resistance	600	10000		Ω
V_{IL}	Low-level input voltage, $\overline{\text{MUTE}}$	38%	40%	43%	VDD
V_{IH}	High-level input voltage, $\overline{\text{MUTE}}$	57%	60%	66%	VDD
T_A	Free-air temperature	0	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		DRV612		UNIT
		PW (TSSOP)	RGT (VQFN)	
		14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	52	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49	71	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62	26	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

VDD = 3.3 V, R_{LD} = 5 kΩ, T_A = 25°C, and charge pump (C_{CP}) = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	VDD = 3.3 V, input ac-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
Vuvp_on	VDD, undervoltage detection				2.8	V
Vuvp_hysteresis	VDD, undervoltage detection, hysteresis			200		mV
F_{CP}	Charge-pump switching frequency			350		kHz
$\|I_{IH}\|$	High-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IH} = VDD			1	µA
$\|I_{IL}\|$	Low-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IL} = 0 V			1	µA
$I_{(VDD)}$	Supply current, no load	VDD, $\overline{\text{MUTE}}$ = 3.3 V		18		mA
	Supply current, MUTED	VDD = 3.3 V, $\overline{\text{MUTE}}$ = GND		18		mA
T_{SD}	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C

7.6 Electrical Characteristics, Line Driver

VDD = 3.3 V, R_{LOAD} = 10 kΩ, T_A = 25°C, charge pump (C_{CP}) = 1 µF, and 1× gain select (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, outputs in phase	1% THD+N, f = 1 kHz, 10 -kΩ load		2.2		V_{rms}
THD+N	Total harmonic distortion plus noise	f = 1 kHz, 10-kΩ load, V_O = 2 V_{rms}		0.007%		
SNR	Signal-to-noise ratio	A-weighted, AES17 filter, 2 V_{rms} ref		105		dB
DNR	Dynamic range	A-weighted, AES17 filter, 2 V_{rms} ref		105		dB
Vn	Noise voltage	A-weighted, AES17 filter		12		µV
Zo	Output impedance when muted	$\overline{\text{MUTE}}$ = GND		0.07	1	Ω
	Input-to-output attenuation when muted	1 Vrms, 1-kHz input		80		dB
	Slew rate			4.5		V/µs
G_{BW}	Unity-gain bandwidth			8		MHz
	Crosstalk, line L-R and R-L	10-kΩ load, V_O = 2 Vrms		–91		dB
I_{limit}	Current limit	VDD = 3.3 V		25		mA

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7.7 Programmable Gain Settings

VDD = 3.3 V, R_{load} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_Tol	Gain programming resistor tolerance				2%	
ΔA_V	Gain matching	Between left and right channels		0.25		dB
	Gain step tolerance			0.1		dB
	Gain steps, gain resistor 2% tolerance	249k or higher		–2		V/V
		82k5		–1		
		51k1		–1.5		
		34k8		–2.3		
		27k4		–2.5		
		20k5		–3		
		15k4		–3.5		
		11k5		–4		
		9k09		–5		
		7k50		–5.6		
		6k19		–6.4		
		5k11		–8.3		
		4k22		–10		
	Input impedance, gain resistor 2% tolerance	249k or higher		37		kΩ
		82k5		55		
		51k1		44		
		34k8		33		
		27k4		31		
		20k5		28		
		15k4		24		
		11k5		22		
		9k09		18		
		7k50		17		
		6k19		15		
		5k11		12		
		4k22		10		

(1) If the GAIN pin is left floating, an internal pullup sets the gain to –2×.
(2) Gain setting is latched during power up.

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7.8 Typical Characteristics

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 1 µF, and Gain = –2 V/V (unless otherwise noted)

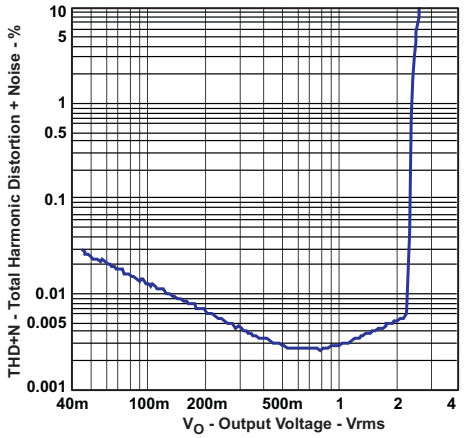


Figure 1. THD+N vs Output Voltage 3.3 V, 10 kΩ, 1 kHz

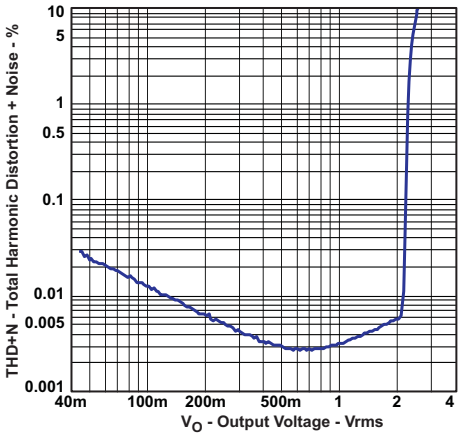
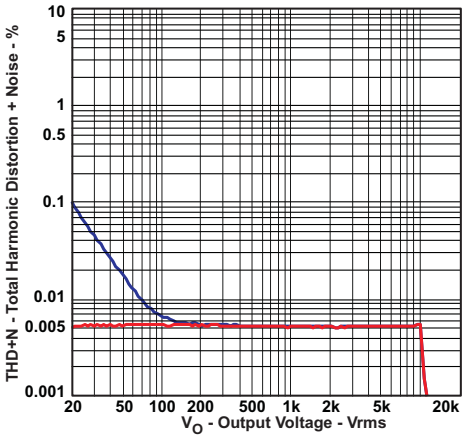
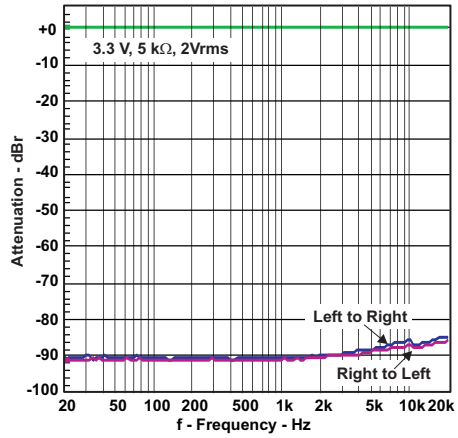


Figure 2. THD+N vs Output Voltage 3.3 V, 600-Ω Load, 1 kHz



Blue: 10-µF ceramic AC-coupling capacitor.
Red: 10-µF electrolytic AC-coupling capacitor.

Figure 3. THD+N vs Frequency 3.3 V, 10-kΩ Load, 2 Vrms



Blue: L to R
Red: R to L

Figure 4. Channel Separation 3.3 V, 5-kΩ Load, 2 Vrms

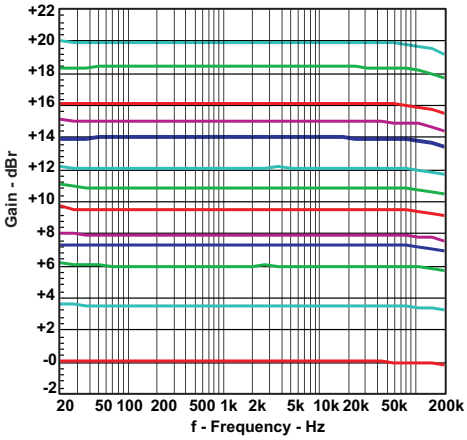


Figure 5. Gain vs Frequency for the Different Gain Settings

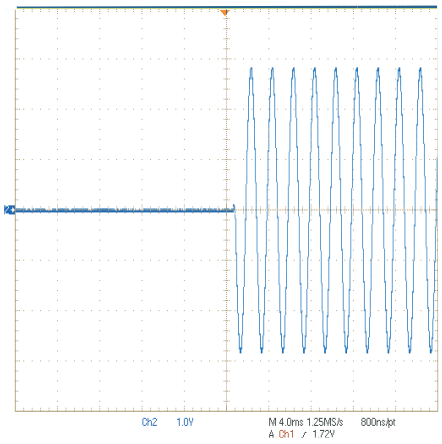


Figure 6. Mute to Play

Typical Characteristics (continued)

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 1 µF, and Gain = –2 V/V (unless otherwise noted)

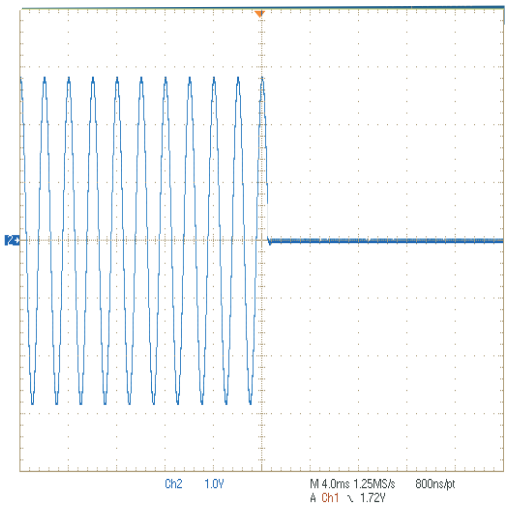


Figure 7. Play to Mute

8 Parameter Measurement Information

All parameters are measured according to the conditions described in *Specifications*.

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9 Detailed Description

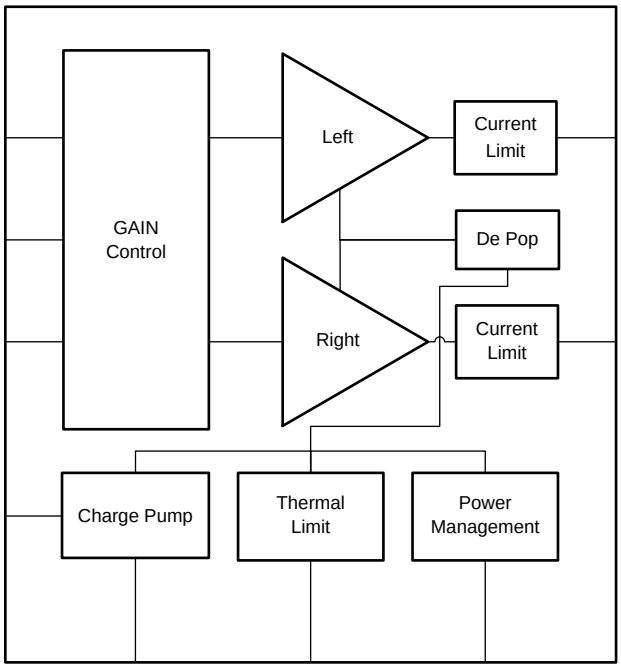
9.1 Overview

The DRV612 is a DirectPath stereo line driver that requires no output DC-blocking capacitors and is capable of delivering 2 Vrms into a 600-Ω load. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on and turn-off. The amplifier outputs have short-circuit protection.

The DRV612 gain is controlled by an external resistors RGAIN, see *Gain-Setting* for recommended values.

The DRV612 operates from a single 3-V to 3.6-V supply, as it uses a built-in charge pump to generate a negative voltage supply for the line driver.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Line Driver Amplifiers

Single-supply line driver amplifiers typically require DC-blocking capacitors. The top drawing in Figure 8 illustrates the conventional line driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

Feature Description (continued)

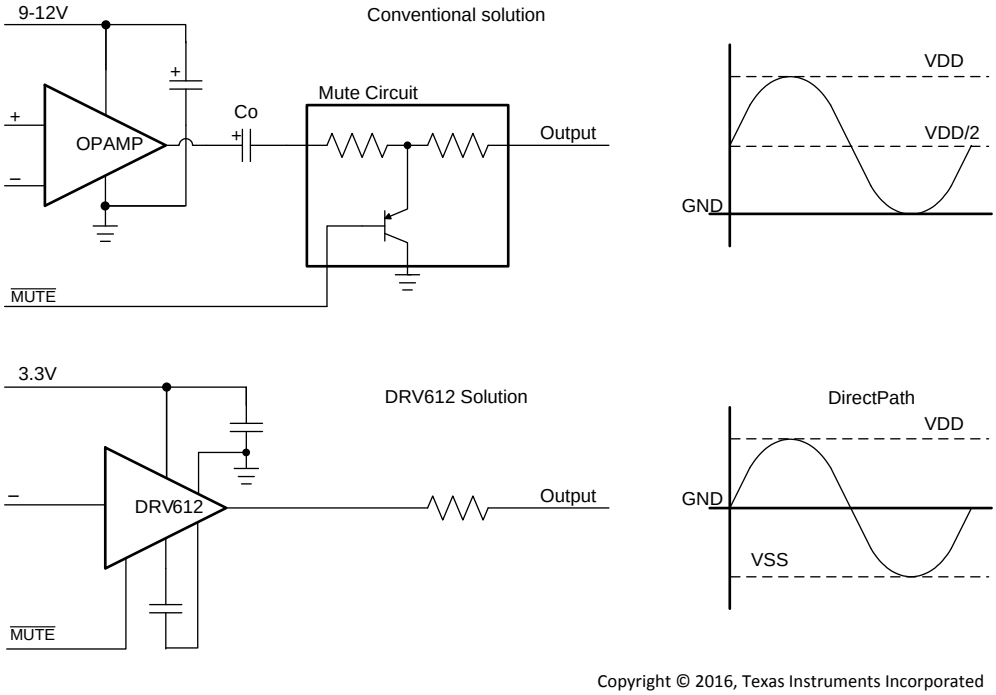

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Figure 8. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click- and pop-reduction circuit, the DirectPath amplifier requires no output dc-blocking capacitors.

The bottom block diagram and waveform of Figure 8 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV612.

9.4 Device Functional Modes

9.4.1 Internal Undervoltage Detection

The DRV612 contains an internal precision band-gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8 V with 200-mV hysteresis.

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Device Functional Modes (continued)

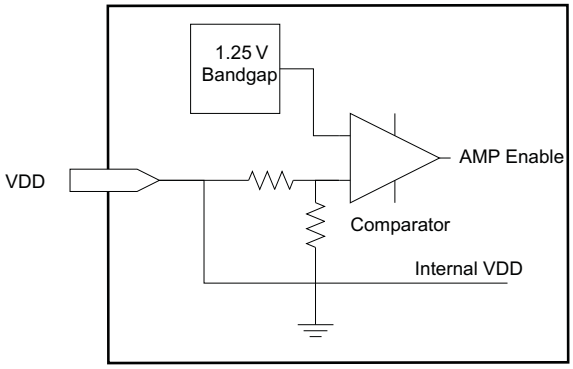

Figure 9. UVP Internal Comparator

9.4.2 Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ pin low during power-supply ramp-up and ramp-down. The pins should be kept low until the input ac-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high, this way proper pre-charge of the ac-coupling is performed and pop-less power up is achieved. Figure 10 illustrates the preferred sequence.

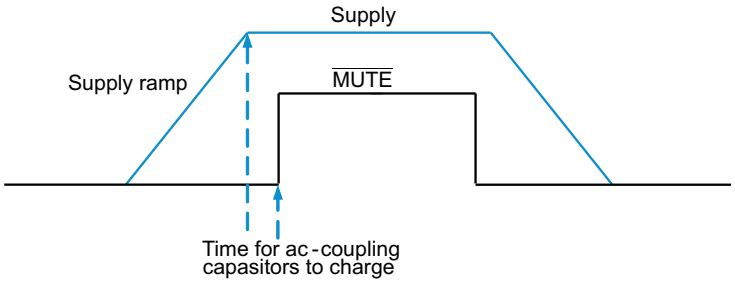

Figure 10. Power-Up and Power-Down Sequence

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DRV612 starts its operation by asserting the MUTE pin to logic 1. The device enters in mute mode when pulling low MUTE pin. The charge pump generates a negative supply voltage. The charge pump flying capacitor connected between CP and CN transfers charge to generate the negative supply voltage. The output voltages are capable of positive and negative voltage swings and are centered close to 0 V, eliminating the need for output capacitors. Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range.

This typical connection diagram highlights the required external components and system level connections for proper operation of the device in popular use case. Any design variation can be supported by TI through schematic and layout reviews. Visit e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.1.1 Capacitive Load

The DRV612 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

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10.2 Typical Application

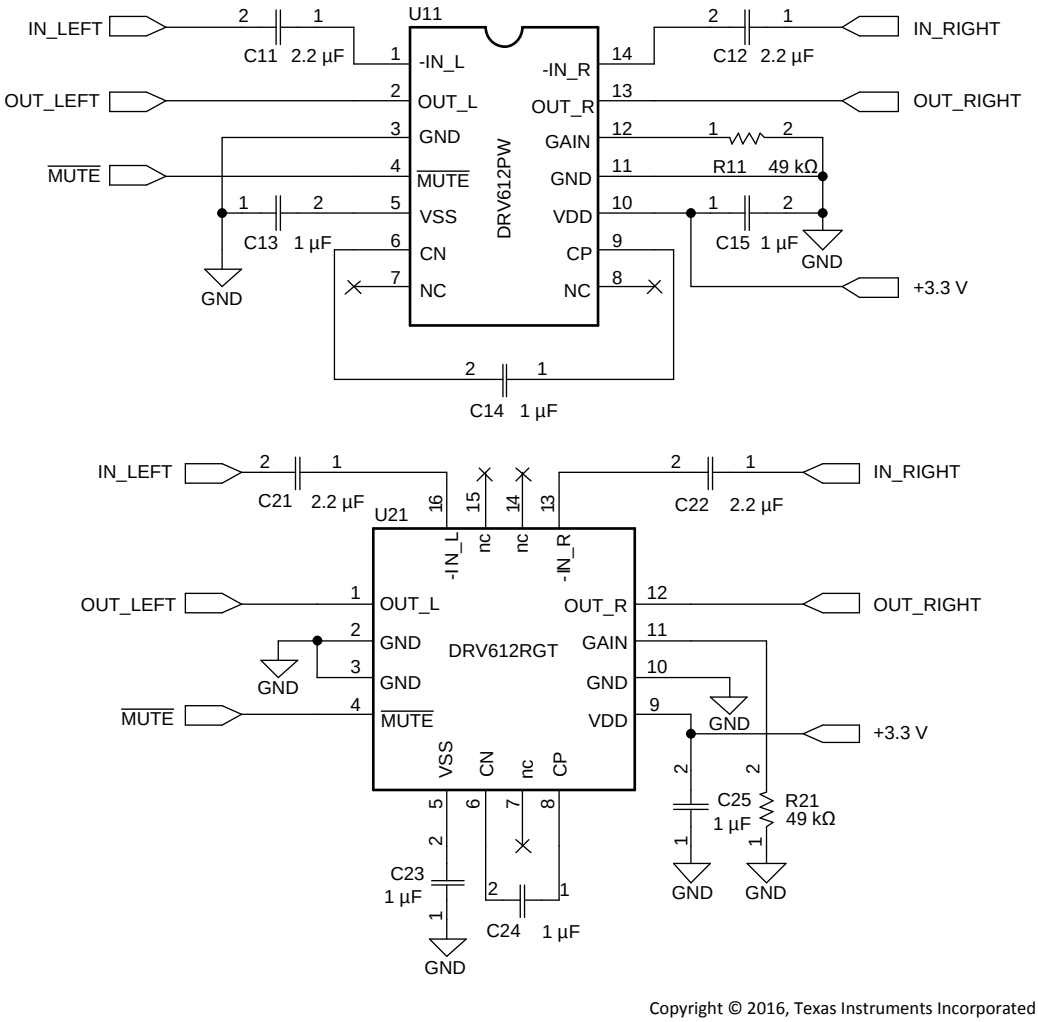

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Figure 11. Single-Ended Input and Output, Gain Set to –1.5×

10.2.1 Design Requirements

Table 1 lists the design parameters for this application example.

Table 1. Typical Application Design Requirements

PARAMETER	VALUE
Input voltage supply	3 V to 3.6 V
Current	130 mA
Load impedance	32 Ω

10.2.2 Detailed Design Procedure

10.2.2.1 Component Selection

10.2.2.1.1 Charge Pump Flying Capacitor and VSS Capacitor

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 µF is typical.

10.2.2.1.2 Decoupling Capacitors

The DRV612 is a DirectPath line-driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV612 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

10.2.2.1.3 Gain-Setting

The gain setting is programmed with the GAIN pin. Gain setting is latched during power on. Table 2 lists the gain settings.

NOTE

If gain pin is left unconnected (open) default gain of –2× is selected.

Table 2. Gain Settings

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE
249 kΩ or higher	–2×	6	37 kΩ
82k5	–1×	0	55 kΩ
51k1	–1.5×	3.5	44 kΩ
34k8	–2.3×	7.2	33 kΩ
27k4	–2.5×	8	31 kΩ
20k5	–3×	9.5	28 kΩ
15k4	–3.5×	10.9	24 kΩ
11k5	–4.0×	12	22 kΩ
9k09	–5×	14	18 kΩ
7k5	–5.6×	15	17 kΩ
6k19	–6.4×	16.1	15 kΩ
5k11	–8.3×	18.4	12 kΩ
4k22	–10×	20	10 kΩ

10.2.2.1.4 Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV612. These capacitors block the dc portion of the audio source and allow the DRV612 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the dc gain to 1, limiting the dc-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 3. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad or \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{1}$$

For a fixed cutoff frequency of 2 Hz, the size of the input capacitance is shown in Table 3 with the capacitors rounded up to nearest E6 values. For 20-Hz cutoff, simply divide the capacitor values with 10; for example, for 1× gain, 150 nF is needed.

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Table 3. Input Capacitor for Different Gain and Cutoff

Gain_set RESISTOR	GAIN (dB)	INPUT RESISTANCE	2-Hz CUTOFF
249 kΩ	–2× (6)	37 kΩ	2.2 µF
82k5	–1× (0)	55 kΩ	1.5 µF
51k1	–1.5× (3.5)	44 kΩ	2.2 µF
34k8	–2.3× (7.2)	33 kΩ	3.3 µF
27k4	–2.5× (8)	31 kΩ	3.3 µF
20k5	–3× (9.5)	28 kΩ	3.3 µF
15k4	–3.5× (10.9)	24 kΩ	3.3 µF
11k5	–4× (12)	22 kΩ	4.7 µF
9k09	–5× (14)	18 kΩ	4.7 µF
7k5	–5.6× (15)	17 kΩ	4.7 µF
6k19	–6.4× (16.1)	15 kΩ	6.8 µF
5k11	–8.3× (18.4)	12 kΩ	6.8 µF
4k22	–10× (20)	10 kΩ	10 µF

10.2.3 Application Curves

The characteristics of this design are shown in Table 4.

Table 4. Table of Graphs

	FIGURE
THD+N vs Output Voltage 3.3 V, 10 kΩ, 1 kHz	Figure 1
THD+N vs Output Voltage 3.3 V, 600-Ω Load, 1 kHz	Figure 2
THD+N vs Frequency 3.3 V, 10-kΩ Load, 2 Vrms	Figure 3
Channel Separation 3.3 V, 5-kΩ Load, 2 Vrms	Figure 4
Gain vs Frequency for the Different Gain Settings	Figure 5
Mute to Play	Figure 6
Play to Mute	Figure 7

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11 Power Supply Recommendations

The device is designed to operate form an input voltage supply from 3 V to 3.6 V. Therefore, the output voltage range of power supply should be within this range and well regulated. TI recommends placing decoupling capacitors in every voltage source pin. Place these decoupling capacitors as close as possible to the DRV612.

12 Layout

12.1 Layout Guidelines

A proposed layout for the DRV612 can be seen in the *DRV612EVM User's Guide*, and the Gerber files can be downloaded from focus.ti.com. To access this information, open the DRV612 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. The VDD and VSS decoupling capacitors and the charge-pump capacitors must be connected with short traces.

12.1.1 Footprint Compatible With TPA6139A2

The DRV612 stereo line driver is pin compatible with the headphone amplifier TPA6139A2. Therefore, a single PCB layout can be used with stuffing options for different board configurations.

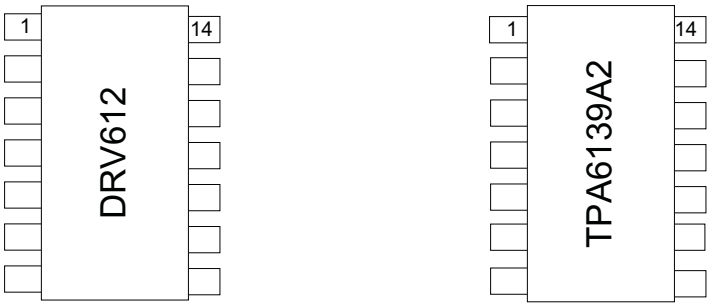

Figure 12. DRV612 and TPA6139A2 Pin Compatibility

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12.2 Layout Examples

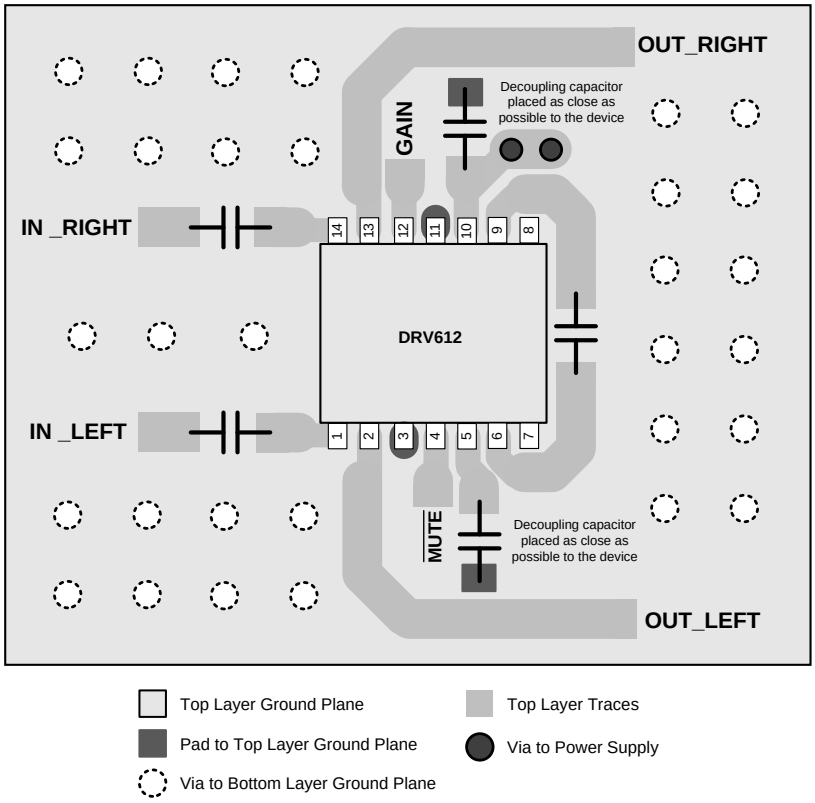

Figure 13. TSSOP Package Layout

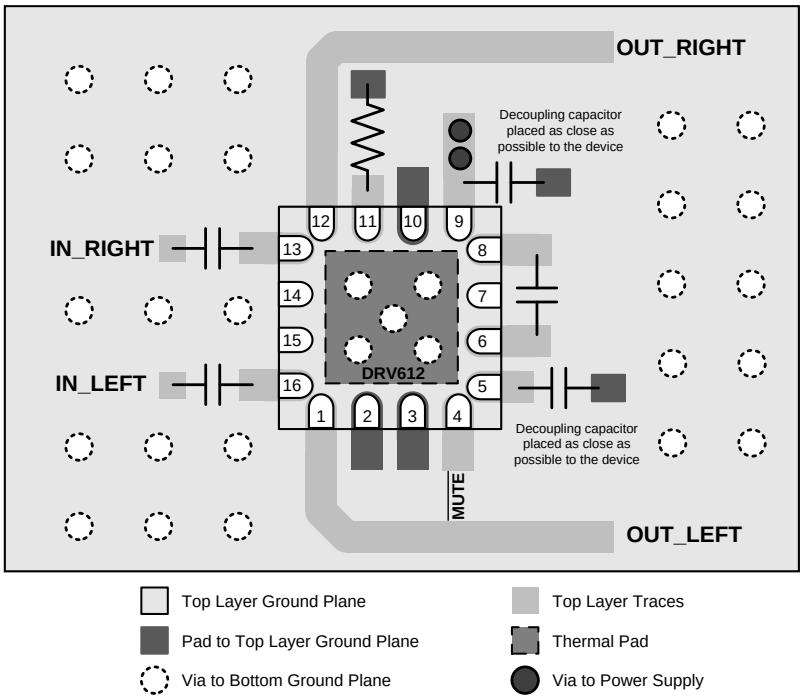

Figure 14. VQFN Package Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

For development support, see the following:

TPA6139A2

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

DRV612EVM User's Guide (SLOU248)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

DirectPath, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV612PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612	Samples
DRV612PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612	Samples
DRV612RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612	Samples
DRV612RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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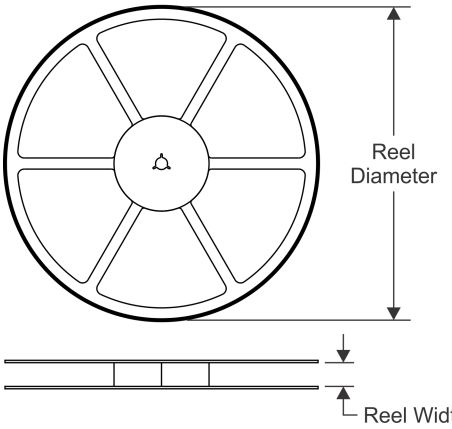
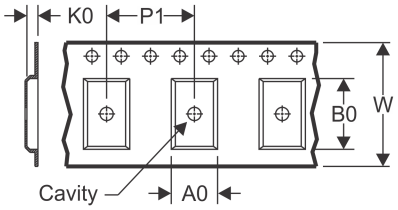
TAPE AND REEL INFORMATION

REEL DIMENSIONS

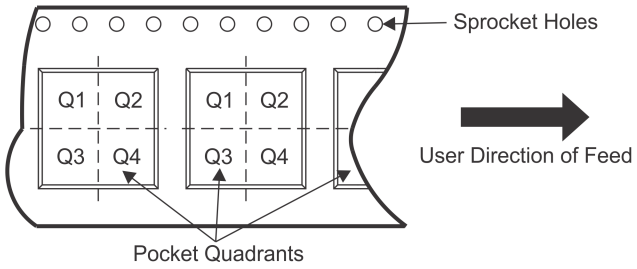


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

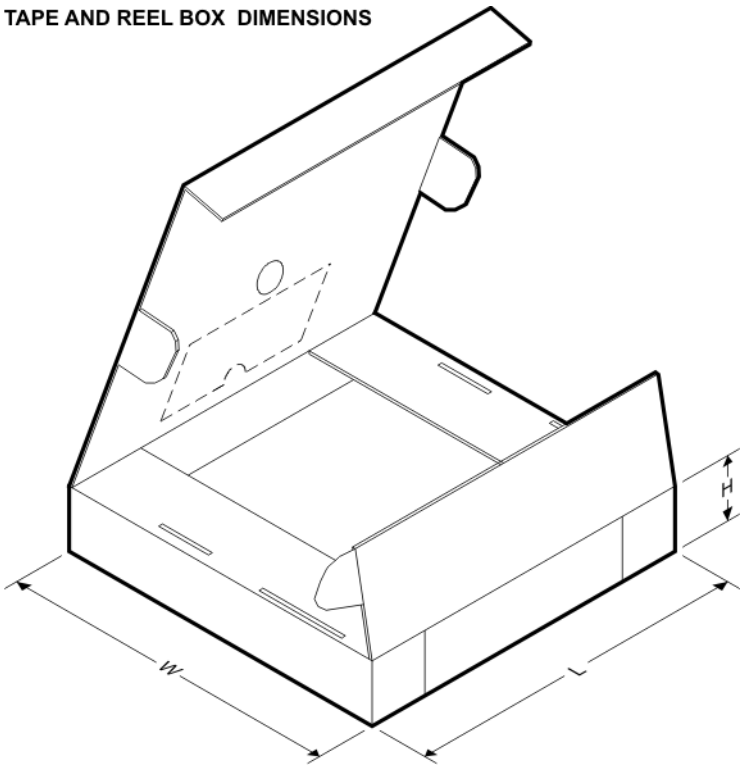
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV612PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV612RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DRV612RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

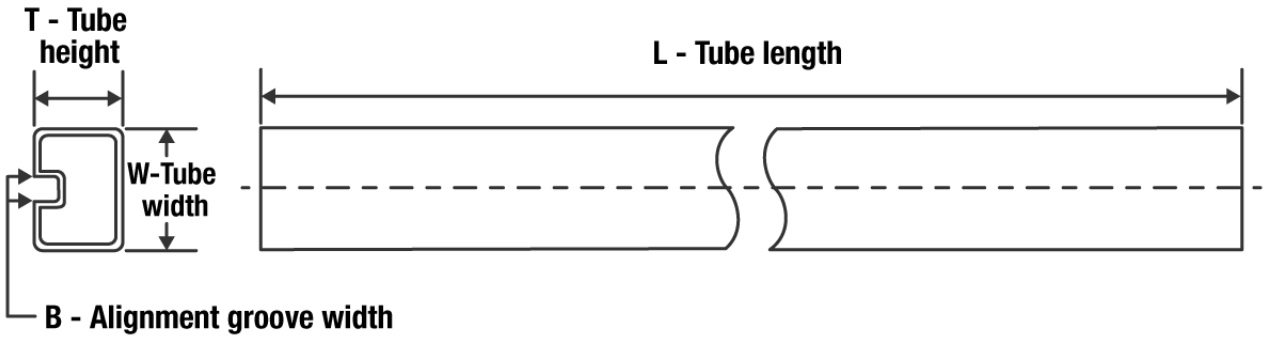
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV612PWR	TSSOP	PW	14	2000	350.0	350.0	43.0
DRV612RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
DRV612RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

TUBE

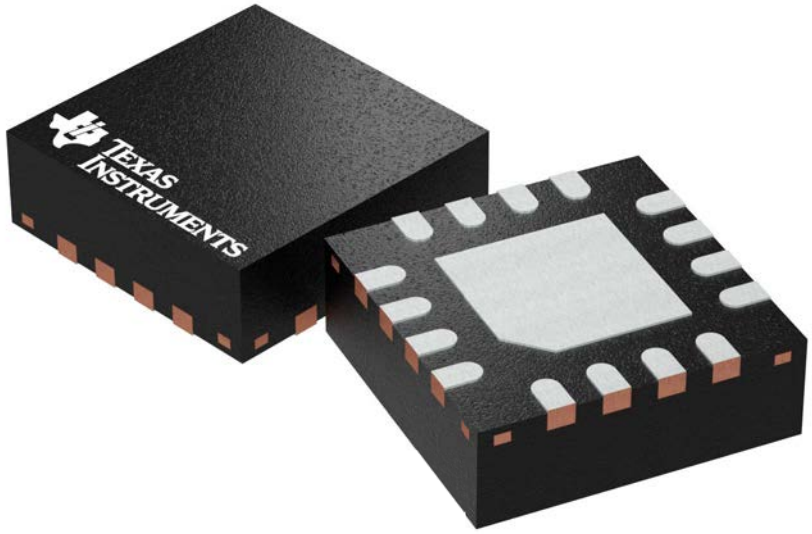


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV612PW	PW	TSSOP	14	90	530	10.2	3600	3.5

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



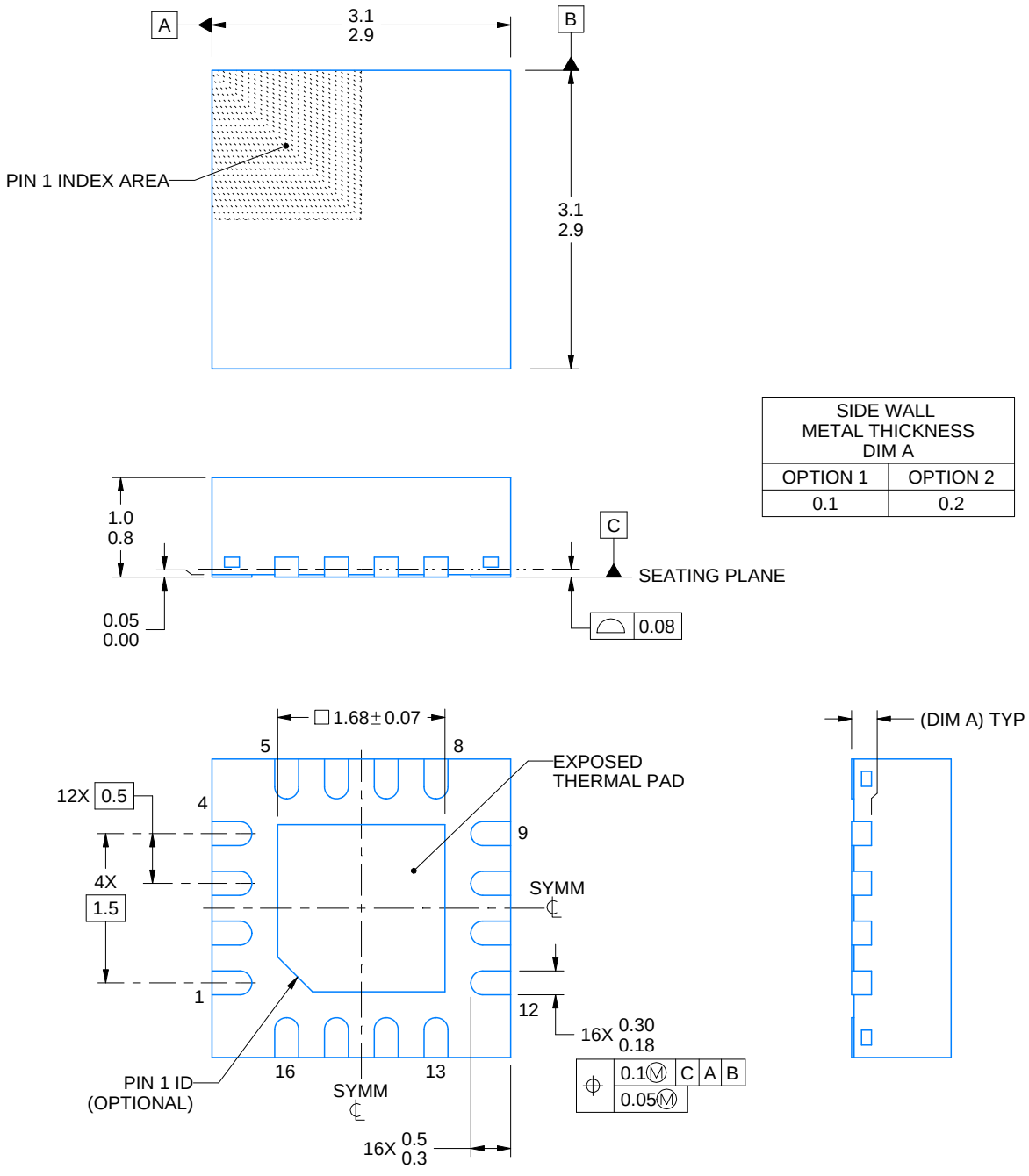
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

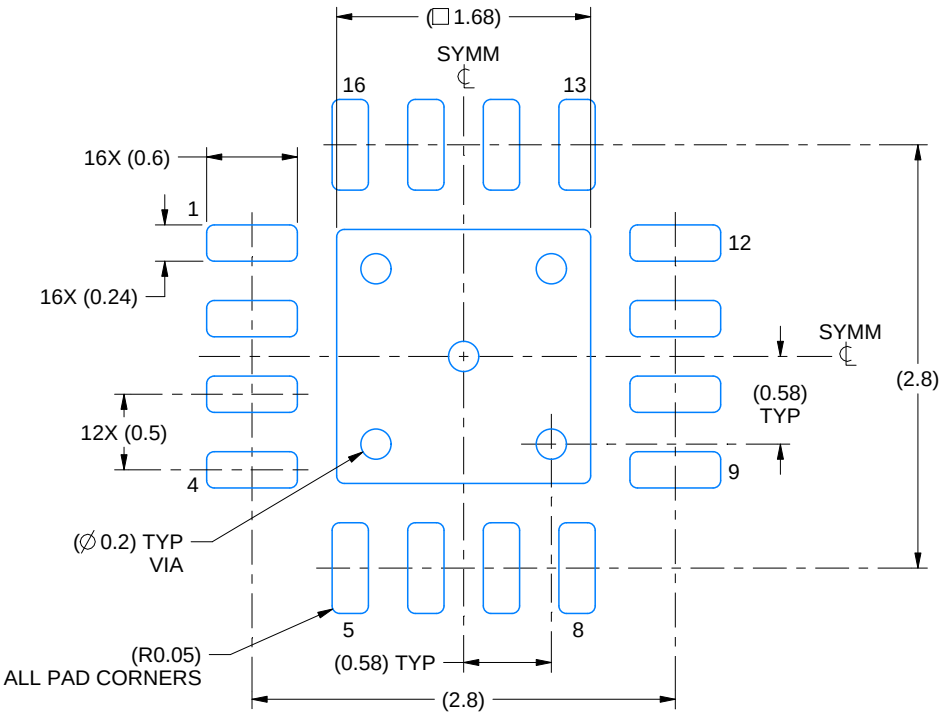
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

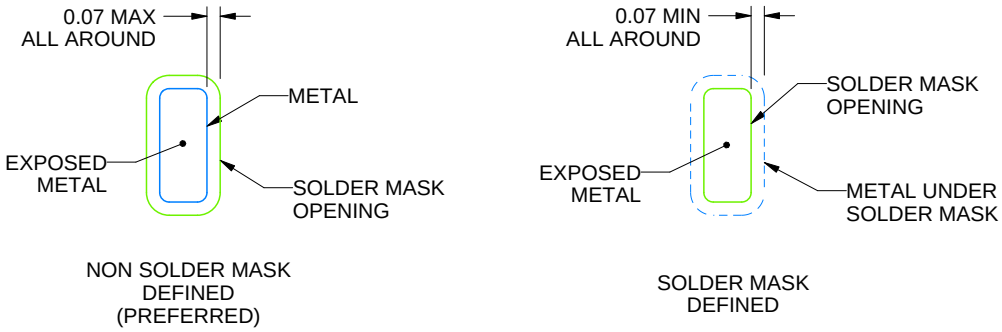


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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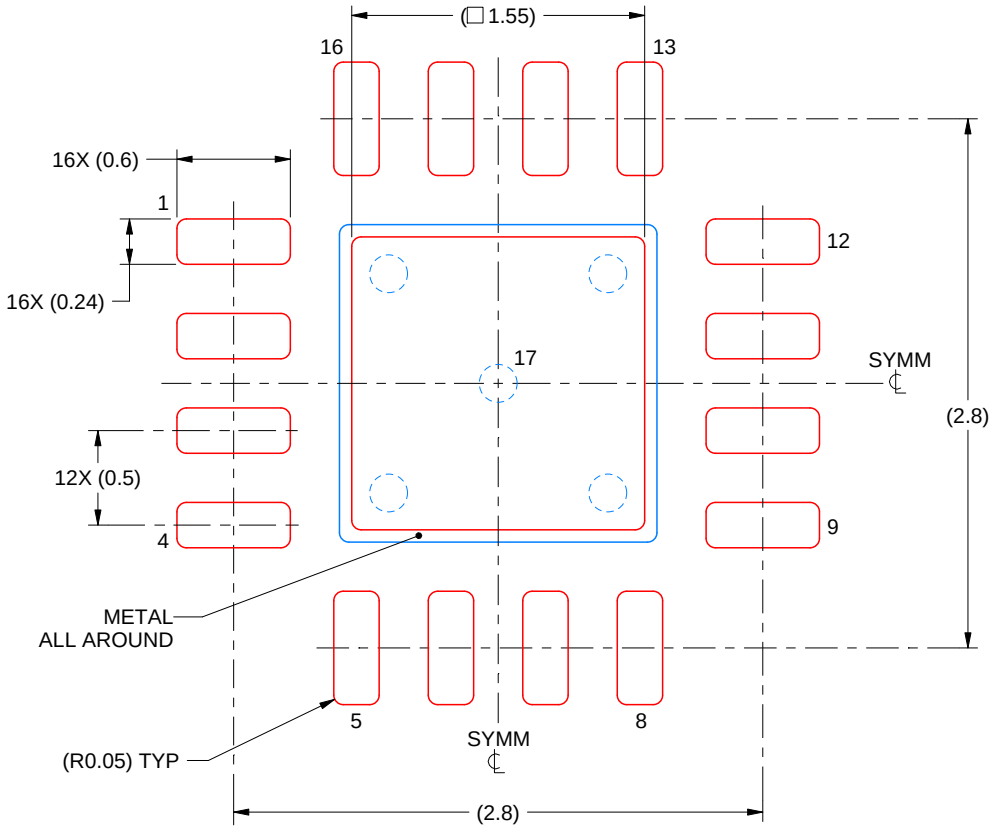
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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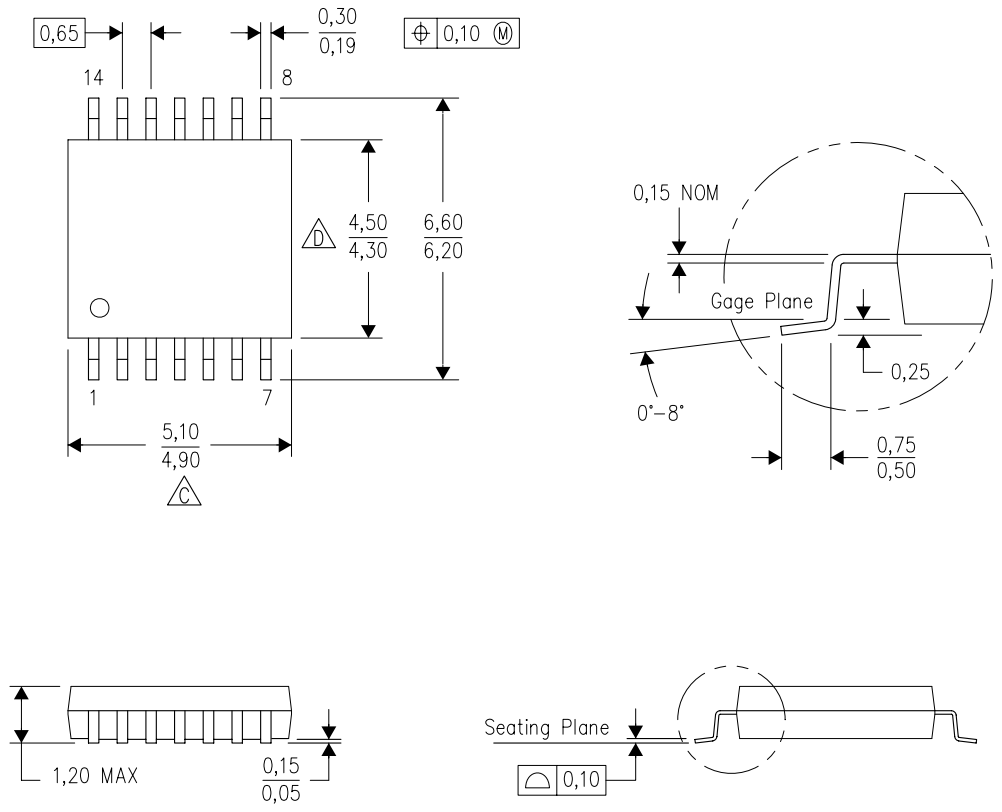
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

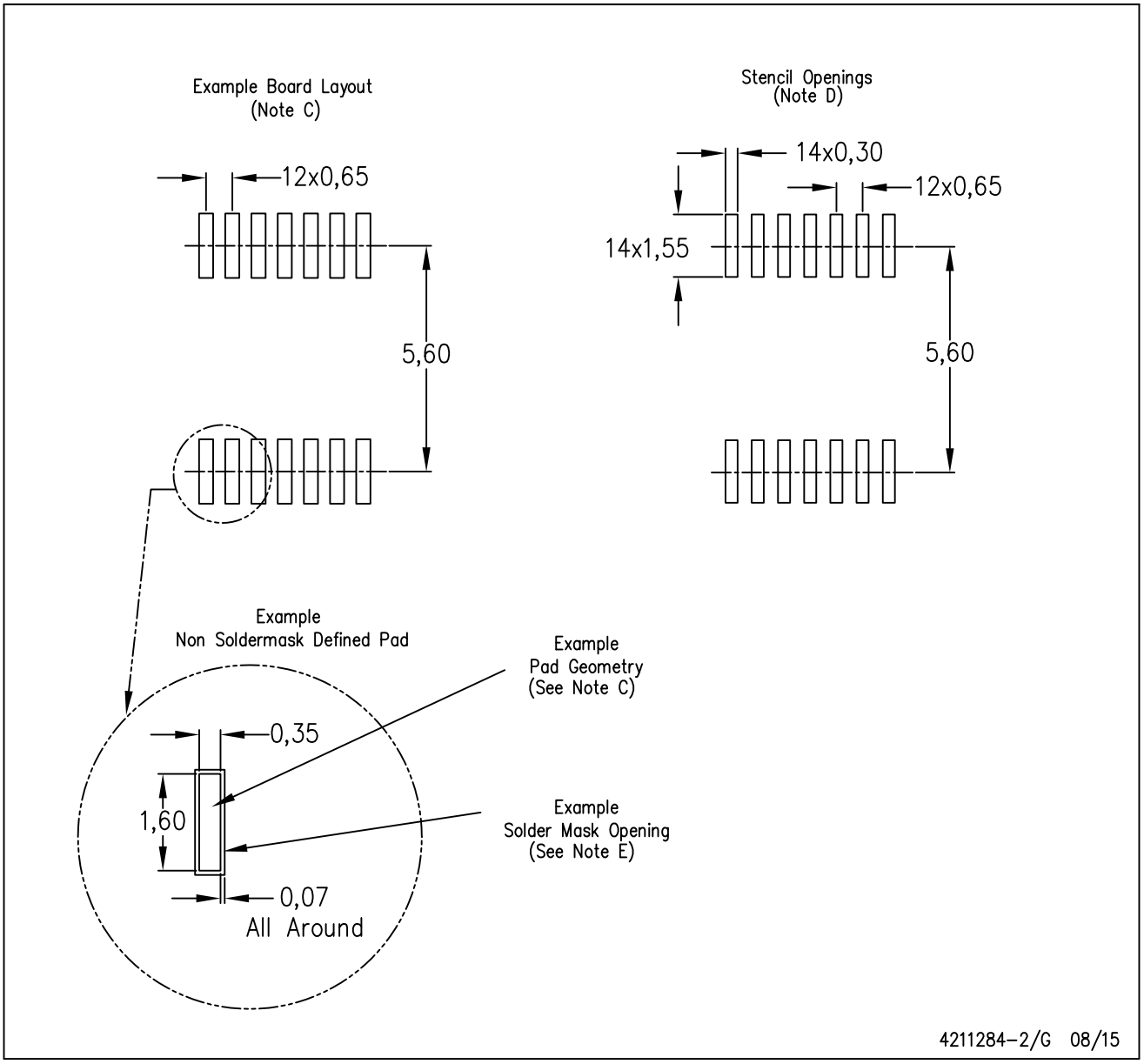
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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