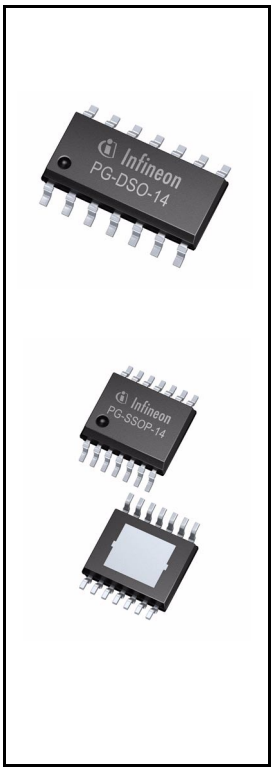
OPTIREG™ Linear TLE42994V33

3.3 V low drop fixed voltage regulator

AEC Qualified

RoHS



1 Overview

Features

- Output voltage 3.3 V ± 2%
- Output current up to 150 mA
- Extreme low current consumption in ON state
- Enable function: Below 1 µA current consumption In OFF state
- Early warning
- Power-on and undervoltage reset with programmable delay time
- Reset low down to V_Q = 1 V
- Adjustable reset threshold
- Very low dropout voltage
- Output current limitation
- Reverse polarity protection
- Overtemperature protection
- Suitable for use in automotive electronics
- Wide temperature range from -40°C up to 150°C
- Input voltage range from 4.4 V to 45 V
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The TLE42994V33 is a monolithic integrated low dropout voltage regulator, especially designed for automotive applications that need to be in ON state during the car's engine is turned off. An input voltage up to 45 V is regulated to an output voltage of 3.3 V. The component is able to drive loads up to 150 mA. It is short-circuit protected by the implemented current limitation and has an integrated overtemperature shutdown. A

reset signal is generated for an output voltage $V_{Q,rt}$ of typically 3.10 V. This threshold can be decreased by an external resistor divider. The power-on reset delay time can be programmed by the external delay capacitor. The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low. Additionally, an enable function permitting enabling/disabling the regulator is also included. In case the regulator is disabled it consumes less current than 1 µA.

Dimensioning information on external components

The input capacitor C_I is recommended for compensation of line influences. The output capacitor C_Q is necessary for the stability of the control loop.

Circuit description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

Type	Package	Marking
TLE42994EV33	PG-SSOP-14 Exposed Pad	42994V33
TLE42994GMV33	PG-DSO-14	42994V33

2 Block diagram

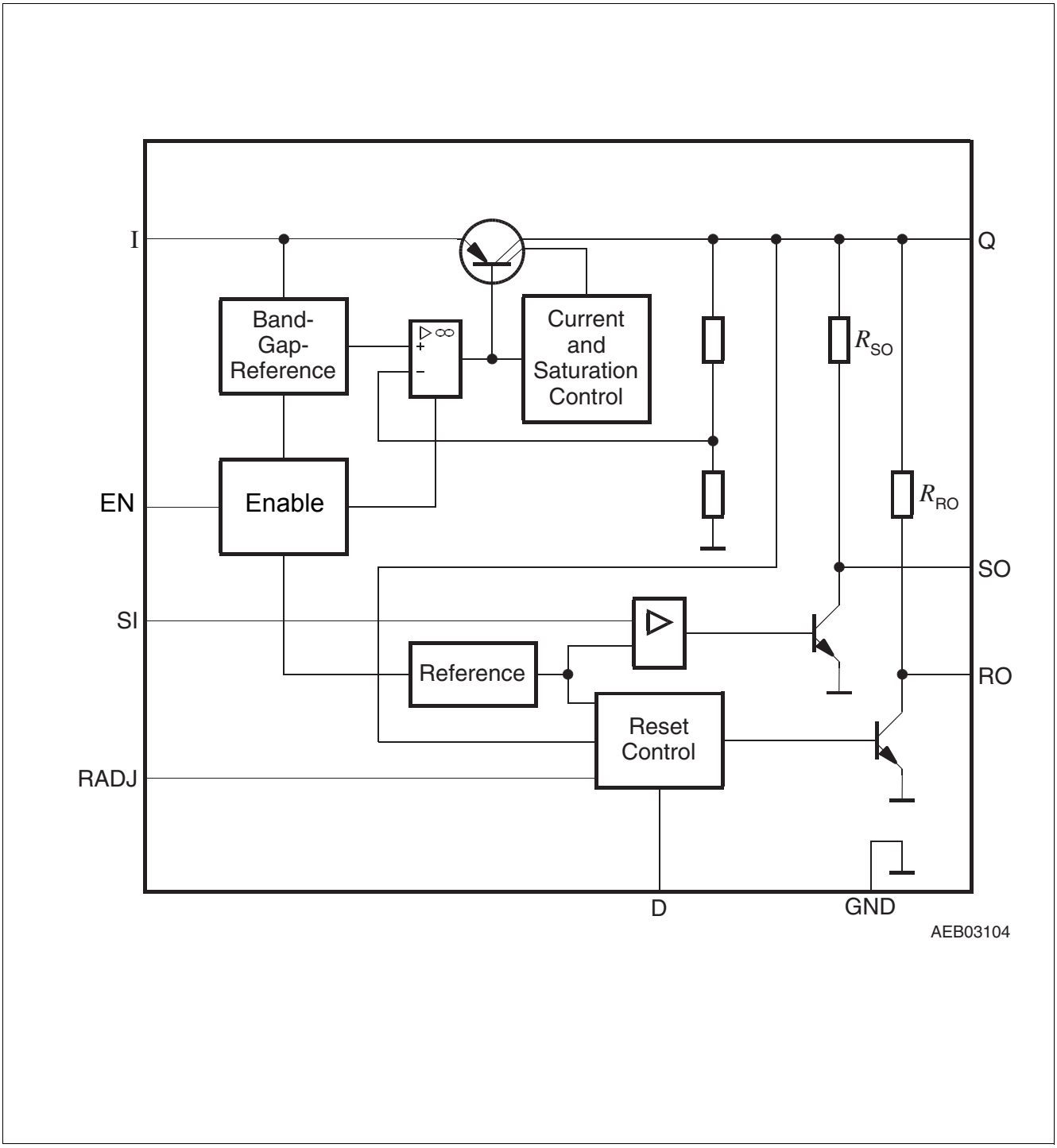


Figure 1 Block diagram

3 Pin configuration

3.1 Pin assignment

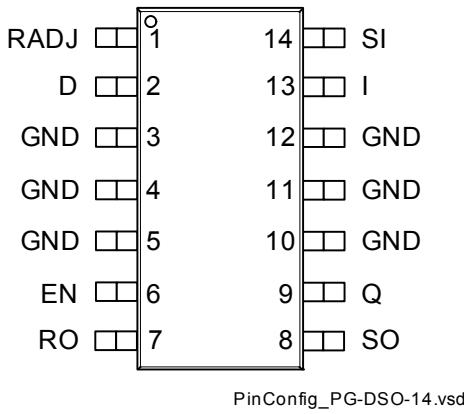


Figure 2 Pin configuration (top view)

3.2 Pin definitions and functions TLE42994GMV33 (PG-DSO-14)

Pin	Symbol	Function
1	RADJ	**Reset threshold adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2	D	**Reset delay timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
3, 4, 5	GND	**Ground** connect all pins to PCB and heatsink area
6	EN	**Enable** high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	**Reset output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	**Sense output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **“Functional range” on Page 9**
10, 11, 12	GND	**Ground** connect all pins to PCB and heatsink area

Pin configuration

Pin	Symbol	Function
13	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
14	SI	**Sense input** connect the voltage to be monitored; connect to Q if the sense comparator is not needed

3.3 Pin assignment TLE42994EV33 (PG-SSOP-14 Exposed Pad)

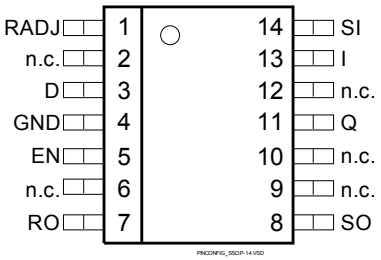


Figure 3 Pin configuration (top view)

3.4 Pin definitions and functions TLE42994EV33 (PG-SSOP-14 Exposed Pad)

Pin	Symbol	Function
1	RADJ	**Reset threshold adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2, 6	n.c.	**Not connected** leave open or connect to GND
3	D	**Reset delay timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
4	GND	**Ground** connect all pins to PCB and heatsink area
5	EN	**Enable** high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	**Reset output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	**Sense output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9, 10, 12	n.c.	**Not connected** leave open or connect to GND
11	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **“Functional range” on Page 9**
13	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended

Pin configuration

Pin	Symbol	Function
14	SI	**Sense input** connect the voltage to be monitored; connect to Q if the sense comparator is not needed
PAD	–	**Exposed pad** attach the exposed pad on package bottom to the heatsink area on circuit board; connect to GND

4 General product characteristics

4.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

-40 °C ≤ T_j ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, enable Input EN, sense input SI							
Voltage	V_I, V_{EN}, V_{SI}	-40	–	45	V	–	P_4.1.1
Output Q, reset output RO, sense output SO							
Voltage	V_Q, V_{RO}, V_{SO}	-0.3	–	7	V	–	P_4.1.2
Reset delay D, reset threshold RADJ							
Voltage	V_D, V_{RADJ}	-0.3	–	7	V	–	P_4.1.3
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD absorption							
ESD absorption	$V_{ESD,HBM}$	-2	–	2	kV	Human body model (HBM)[2)]	P_4.1.6
ESD absorption	$V_{ESD,CDM}$	-500	–	500	V	Charge device model (CDM)[3)]	P_4.1.7
ESD absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge device model (CDM)[3)] at corner pins	P_4.1.8

1) Not subject to production test, specified by design
2) ESD susceptibility human body model “HBM” according to AEC-Q100-002 - JESD22-A114
3) ESD susceptibility charged device model “CDM” according to ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	4.4	–	45	V	–	P_4.2.1
Output capacitor's requirements for stability	C_Q	22	–	–	µF	–[1)]	P_4.2.2
Output capacitor's requirements for stability	$ESR(C_Q)$	–	–	3	Ω	–[2)]	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) Relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal resistance

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TLE42994GMV33 (PG-DSO-14)							
Junction to Soldering Point[1]	R_{thJSP}	–	–	30	K/W	measured to pin 5	P_4.3.1
Junction to Ambient[1]	R_{thJA}	–	63	–	K/W	FR4 2s2p board[2]	P_4.3.2
Junction to Ambient[1]	R_{thJA}	–	112	–	K/W	FR4 1s0p board, footprint only[3]	P_4.3.3
Junction to Ambient[1]	R_{thJA}	–	73	–	K/W	FR4 1s0p board, 300mm^2 heatsink area on PCB[3]	P_4.3.4
Junction to Ambient[1]	R_{thJA}	–	65	–	K/W	FR4 1s0p board, 600mm^2 heatsink area on PCB[3]	P_4.3.5
TLE42994EV33 (PG-SSOP-14 Exposed Pad)							
Junction to Soldering Point[1]	R_{thJSP}	–	10	–	K/W	measured to all GND pins	P_4.3.6
Junction to Ambient[1]	R_{thJA}	–	47	–	K/W	FR4 2s2p board[2]	P_4.3.7
Junction to Ambient[1]	R_{thJA}	–	140	–	K/W	FR4 1s0p board, footprint only[3]	P_4.3.8
Junction to Ambient[1]	R_{thJA}	–	63	–	K/W	FR4 1s0p board, 300mm^2 heatsink area on PCB[3]	P_4.3.9
Junction to Ambient[1]	R_{thJA}	–	53	–	K/W	FR4 1s0p board, 600mm^2 heatsink area on PCB[3]	P_4.3.10

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Block description and electrical characteristics

5.1 Voltage regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional range" on Page 9** have to be maintained. For details see also the typical performance graph **"Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ" on Page 14**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor C_I is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

To avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42994V33 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

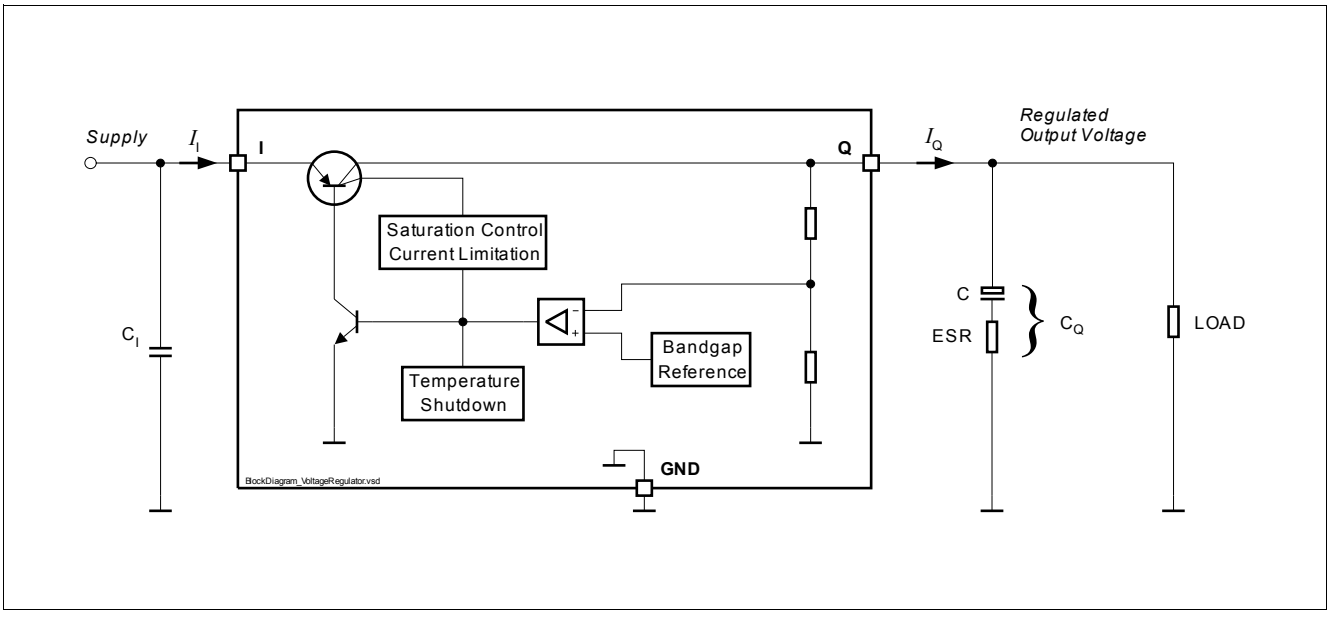


Figure 4 Voltage regulator

Table 4 Electrical characteristics voltage regulator

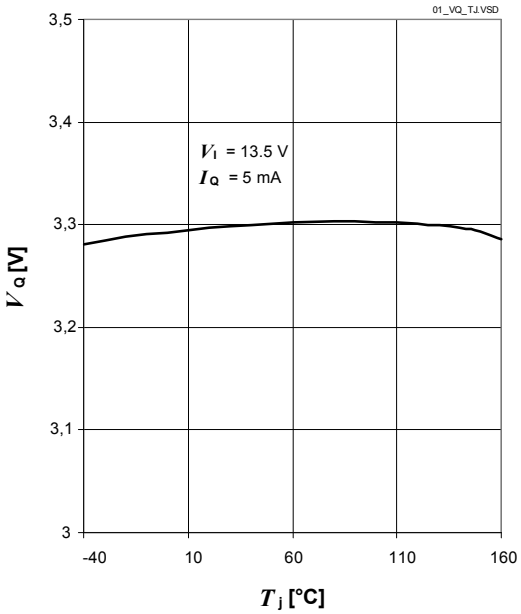
V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	3.23	3.30	3.37	V	100 µA < I_Q < 100 mA 5.5 V < V_I < 18 V	P_5.1.1
Output voltage	V_Q	3.20	3.30	3.40		100 µA < I_Q < 150 mA 5.5 V < V_I < 18 V	P_5.1.2
Output current limitation	$I_{Q,max}$	150	400	500	mA		P_5.1.3
Load regulation steady-state	$\Delta V_{Q,\,load}$	-30	-5	–	mV	I_Q = 1 mA to 100 mA V_I = 6 V	P_5.1.4
Line regulation steady-state	$\Delta V_{Q,\,line}$	–	10	25	mV	V_I = 6 V to 32 V I_Q = 1 mA	P_5.1.5
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[1)]	P_5.1.7
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	°C	T_j decreasing[1)]	P_5.1.8
Power supply ripple rejection[1)]	*PSRR*	–	66	–	dB	f_{ripple} = 100 Hz V_{ripple} =1 V_{pp} I_Q = 100 mA	P_5.1.9

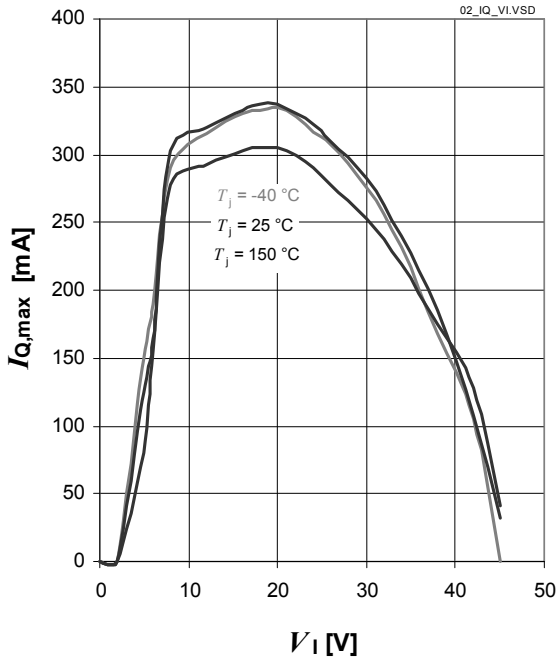
1) Not subject to production test, specified by design

5.2 Typical performance characteristics voltage regulator

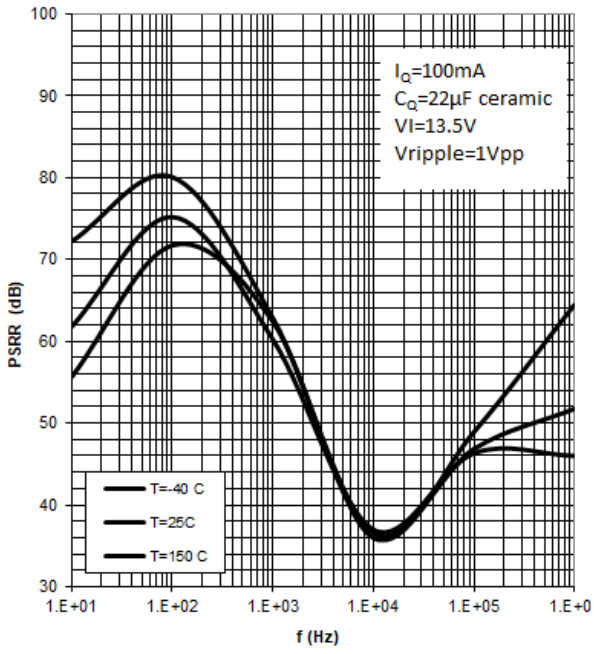
Output Voltage V_Q versus Junction Temperature T_J



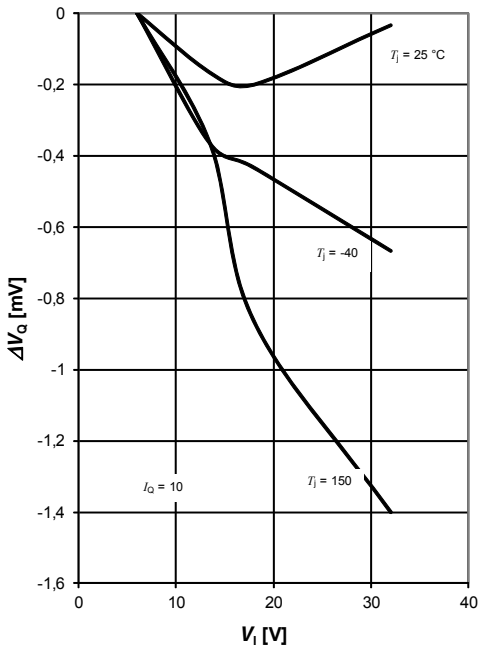
Output Current I_Q versus Input Voltage V_I



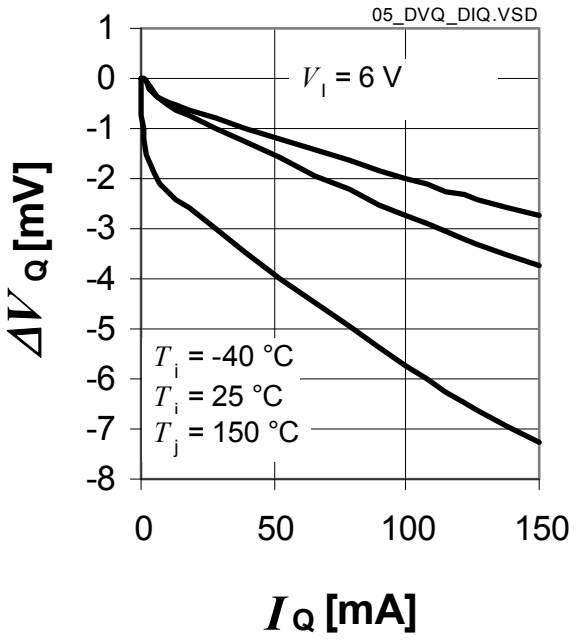
Power Supply Ripple Rejection *PSRR* versus ripple frequency f_r



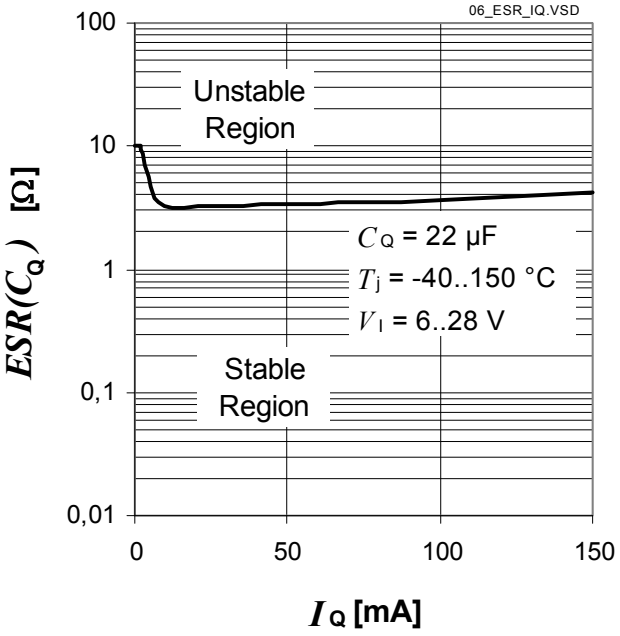
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage Change ΔV_I



Load Regulation $\Delta V_{Q,load}$ versus Output Current Change ΔI_Q



Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



5.3 Current consumption

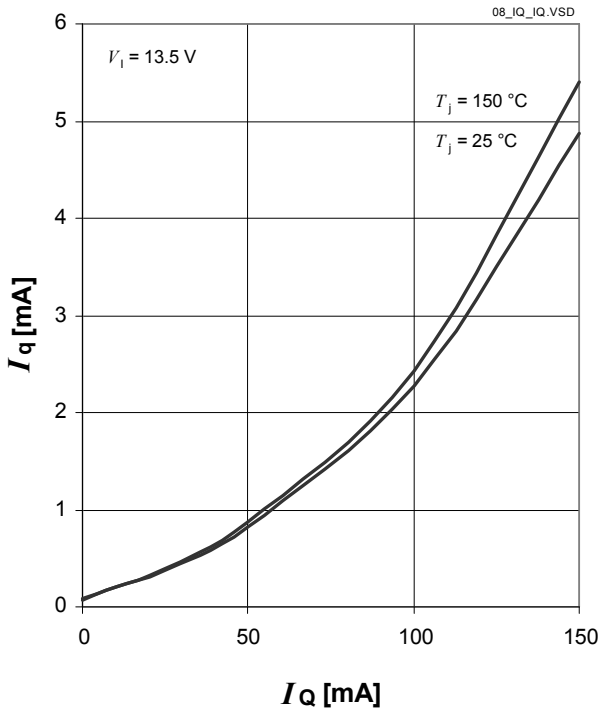
Table 5 Electrical characteristics voltage regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

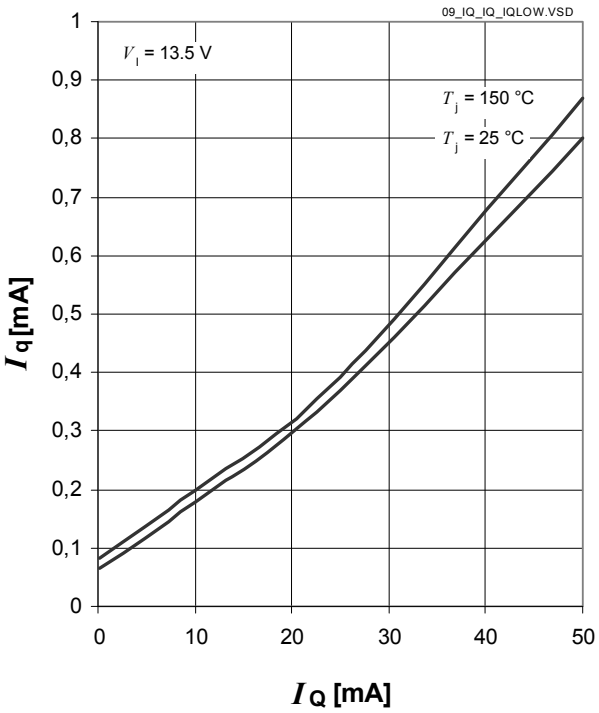
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I - I_Q$	I_q	–	–	1	µA	V_{EN} = 0 V T_j = 25 °C	P_5.4.1
Current consumption $I_q = I_I - I_Q$	I_q	–	65	100	µA	Enable HIGH I_Q = 100 µA, T_j = 25 °C	P_5.4.2
Current consumption $I_q = I_I - I_Q$	I_q	–	65	105	µA	Enable HIGH I_Q = 100 µA, T_j ≤ 85 °C	P_5.4.3
Current consumption $I_q = I_I - I_Q$	I_q	–	0.17	0.5	mA	Enable HIGH I_Q = 10 mA	P_5.4.4
Current consumption $I_q = I_I - I_Q$	I_q	–	0.7	2	mA	Enable HIGH I_Q = 50 mA	P_5.4.5

5.4 Typical performance characteristics current consumption

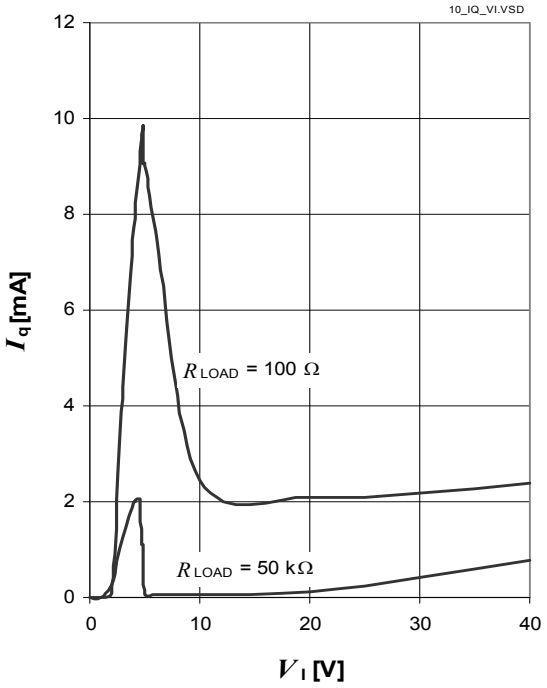
Current consumption I_q versus output current I_Q



Current consumption I_q versus output current I_Q (I_Q low)



Current consumption I_q versus input voltage V_I



5.5 Enable function

Table 6 Electrical characteristics voltage regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable OFF voltage range	$V_{EN,OFF}$	–	–	0.8	V	–	P_5.6.1
Enable ON voltage range	$V_{EN,ON}$	3.5	–	–	V	–	P_5.6.2
Enable OFF input current	$I_{EN,OFF}$	–	0.5	2	µA	V_{EN} = 0 V	P_5.6.3
Enable ON input current	$I_{EN,ON}$	–	3	5	µA	V_{EN} = 5 V	P_5.6.4

5.6 Reset function

The reset function provides several features:

Output undervoltage reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-on reset delay time:

The power-on reset delay time *t*rd allows a microcontoller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

If the application needs a power-on reset delay time *t*rd different from the value given in **Power-on reset delay time**, the delay capacitor’s value can be derived from the specified values in **Power-on reset delay time** and the desired power-on delay time:

(5.1)

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100\,nF$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd}: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

Reset reaction time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction rime t_{rr} considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction time becomes:

(5.2)

$$t_{rr} = t_{rd,int} + t_{rr,d}$$

with

- t_{rr}: reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

Optional reset output pull-up resistor $R_{RO,ext}$:

The Reset Output RO is an open collector output with an integrated pull-up resistor. If needed, an external pull-up resistor to the output Q can be added. In **Table 7 “Electrical characteristics reset function” on Page 20** a minimum value for the external resistor $R_{RO,ext}$ is given.

Reset adjust function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

(5.3)

$$V_{RT,\,new} = \frac{R_{ADJ,\,1} + R_{ADJ,\,2}}{R_{ADJ,\,2}} \times V_{RADJ,\,th}$$

with

- $V_{RT,new}$: the desired new reset switching threshold
- R_{ADJ1}, R_{ADJ2}: resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjust switching threshold given in **Table 7 "Electrical characteristics reset function" on Page 20**

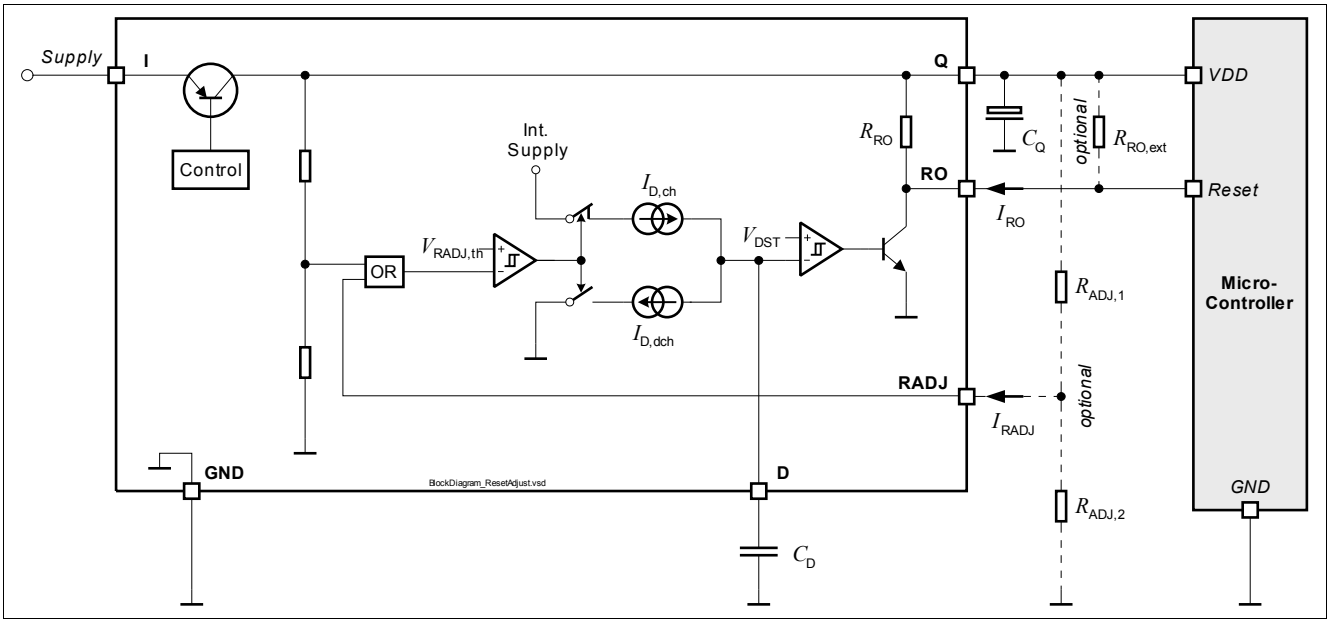


Figure 5 Block diagram reset function

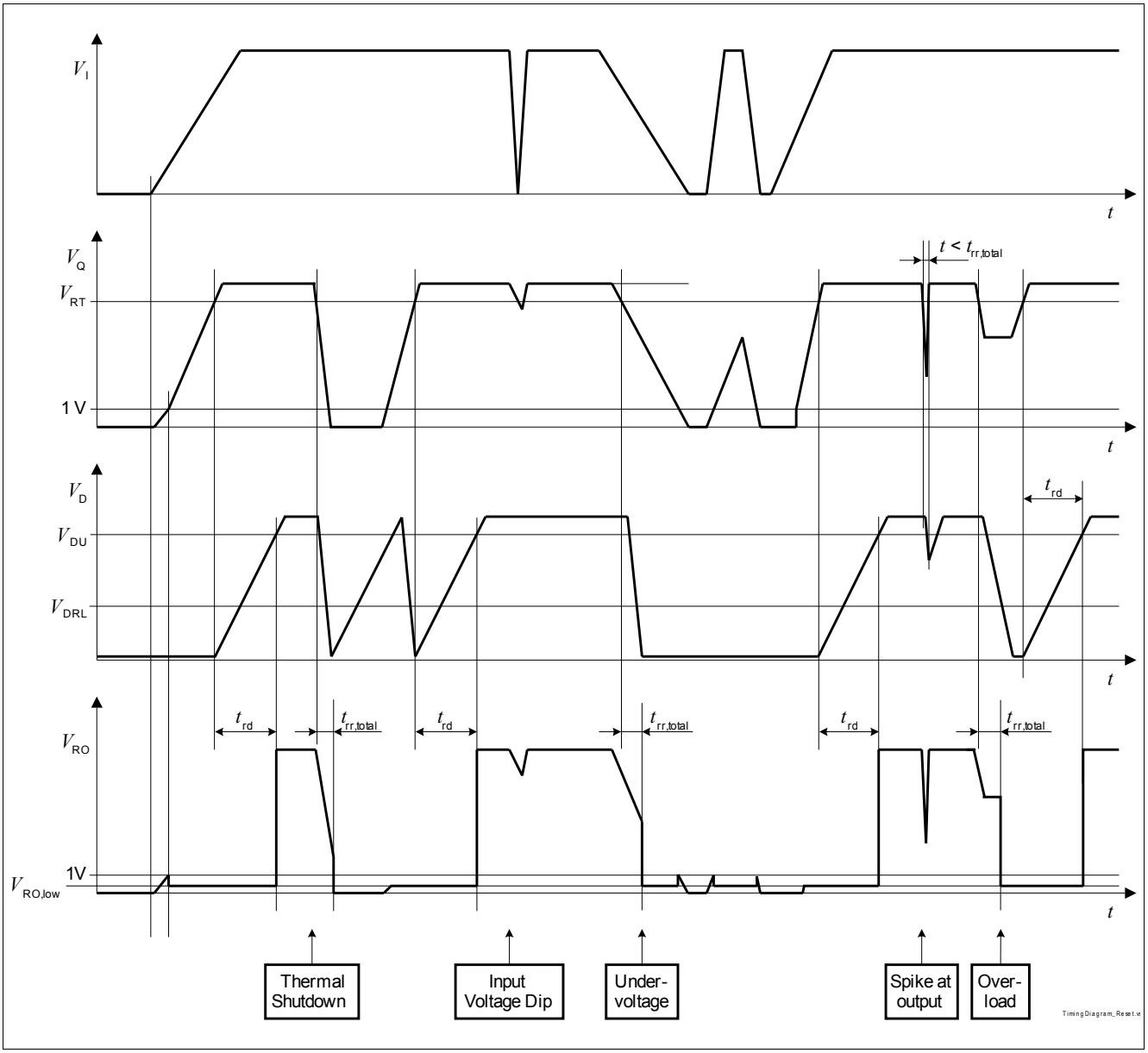


Figure 6 Timing diagram reset

Table 7 Electrical characteristics reset function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

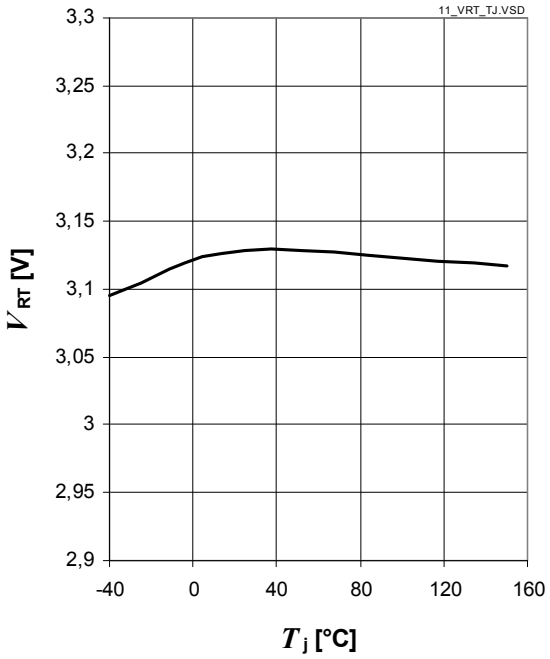
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset							
Default output undervoltage reset Switching thresholds	V_{RT}	3.00	3.10	3.20	V	V_Q decreasing	P_5.7.1
Output undervoltage reset headroom	V_{RH}	50	200	300	mV	–	
Output undervoltage reset threshold adjustment							
Reset adjust Switching threshold	$V_{RADJ,th}$	1.26	1.36	1.44	V	V_Q > 2.5 V	P_5.7.2
Reset adjustment range[1)]	$V_{RT,range}$	2.50	–	3.10	V	–	P_5.7.3
Reset output RO							
Reset output low voltage	$V_{RO,low}$	–	0.1	0.4	V	1 V ≤ V_Q ≤ V_{RT} no external $R_{RO,ext}$	P_5.7.4
Reset output internal Pull-up resistor to V_Q	R_{RO}	10	20	40	kΩ	–	P_5.7.5
Optional reset output external Pull-up resistor to V_Q	$R_{RO,ext}$	5.6	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V	P_5.7.6
Reset delay Ttming							
Delay pin output voltage	V_D	–	–	5	V	–	P_5.7.7
Power-on reset delay time	t_{rd}	36	51	60	ms	C_D = 100 nF Calculated value: $t_{rd} = C_D * V_{DU} / I_{D,ch}$	P_5.7.8
Upper delay Switching threshold	V_{DU}	–	1.85	–	V	–	P_5.7.9
Lower delay Switching threshold	V_{DL}	–	0.50	–	V	–	P_5.7.10
Delay capacitor Charge current	$I_{D,ch}$	–	3.5	–	µA	V_D = 1 V	P_5.7.11
Delay capacitor Reset discharge current	$I_{D,dch}$	–	70	–	mA	V_D = 1 V	P_5.7.12
Delay capacitor Discharge time	$t_{rr,\,d}$	–	1.7	3.0	µs	Calculated Value: $t_{rr,\,d} = C_D*(V_{DU} - V_{DL})/ I_{D,dch}$ C_D = 100 nF	P_5.7.13
Internal reset reaction time	$t_{rr,\,int}$	–	20	25	µs	C_D = 0 nF [2)]	P_5.7.14
Reset reaction time	$t_{rr,\,total}$	–	21.7	28	µs	Calculated value: $t_{rr,\,total} = t_{rr,\,int} + t_{rr,d}$ C_D = 100 nF	P_5.7.15

1) V_{RT} is scaled linearly, in case the Reset Switching Threshold is modified

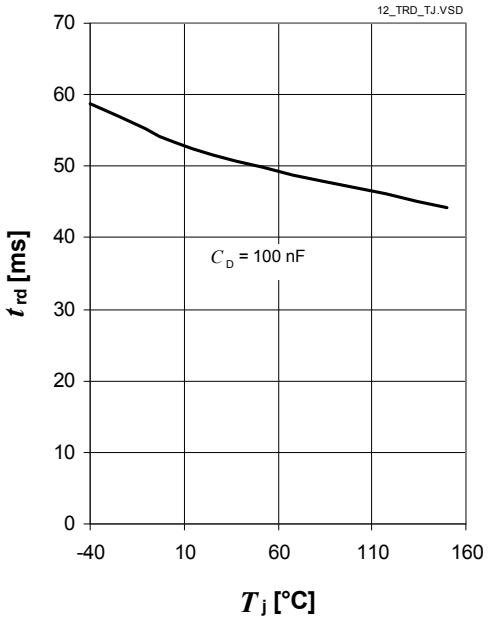
2) Parameter not subject to production test; specified by design

5.7 Typical performance characteristics reset

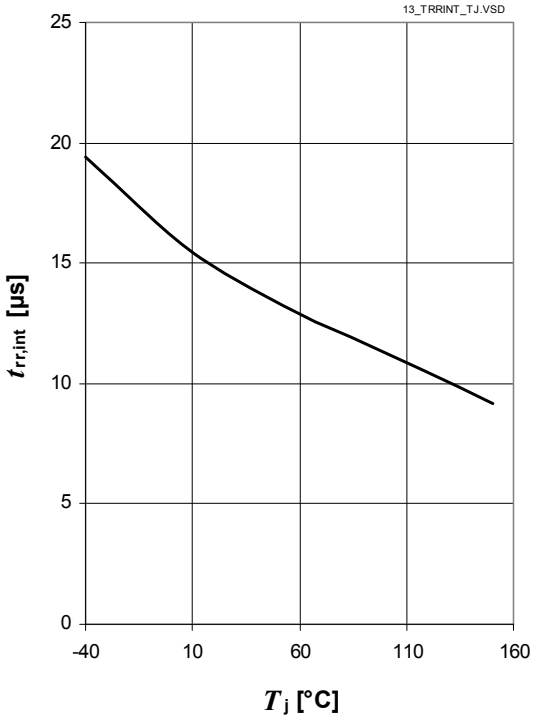
Undervoltage reset switching threshold V_{RT} versus junction temperature T_j



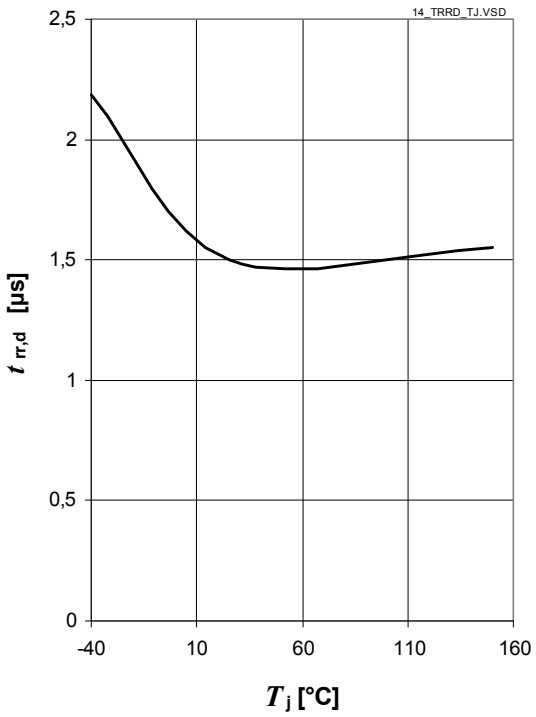
Power-on reset delay time t_{rd} versus junction temperature T_j



Internal reset reaction time $t_{rr,int}$ versus junction temperature T_j



Delay capacitor discharge time $t_{rr,d}$ versus junction temperature T_j



5.8 Early warning function

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low.

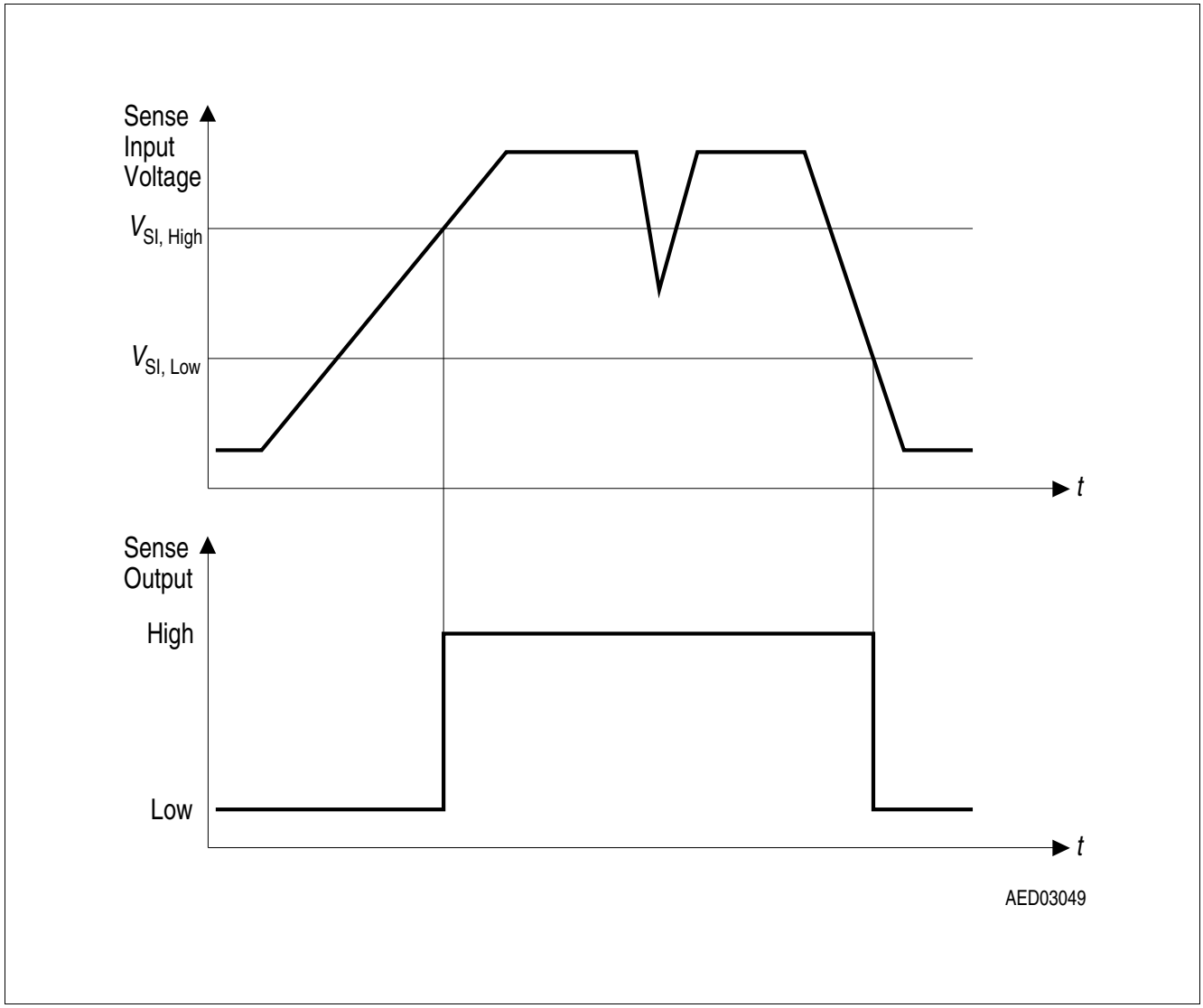


Figure 7 Sense timing diagram

Table 8 Electrical characteristics early warning function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sense comparator input							
Sense threshold high	$V_{SI,high}$	1.34	1.45	1.54	V	–	P_5.9.1
Sense threshold low	$V_{SI,low}$	1.26	1.36	1.44	V	–	P_5.9.2
Sense switching hysteresis	$V_{SI,hy}$	50	90	130	mV	$V_{SI,hy} = V_{SI,high} - V_{SI,low}$	P_5.9.3
Sense input current	I_{SI}	-1	-0.1	1	µA	–	P_5.9.4

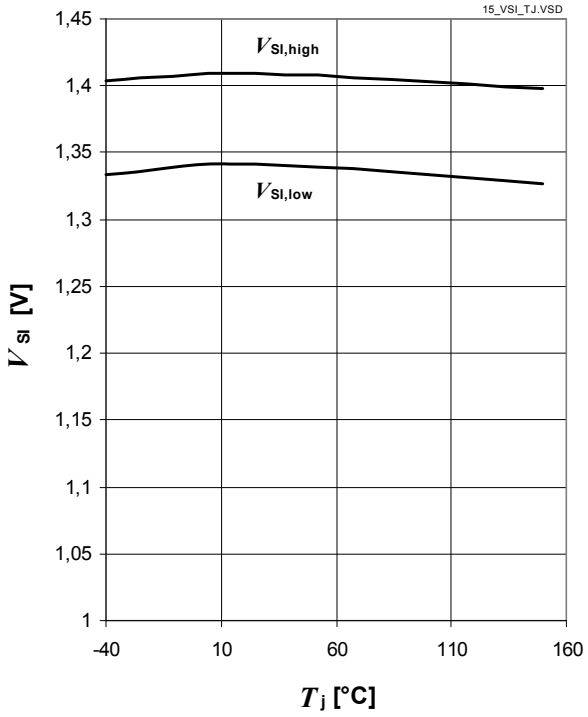
Table 8 Electrical characteristics early warning function (cont'd)

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sense comparator output							
Sense output low voltage	$V_{SO,low}$	–	0.1	0.4	V	$V_{SI} < V_{SI,low}$ $V_I > 4.4$ V no external $R_{SO,ext}$	P_5.9.5
Sense output internal Pull-up resistor to V_Q	R_{SO}	10	20	40	kΩ	–	P_5.9.6
Optional sense output external pull-up resistor to V_Q	$R_{SO,ext}$	5.6	–	–	kΩ	$V_I > 4.4$ V $V_{SO} \leq 0.4$ V	P_5.9.7

5.9 Typical performance characteristics early warning

Sense thresholds $V_{SI,high}$, $V_{SI,low}$ versus junction temperature T_j



6 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application diagram

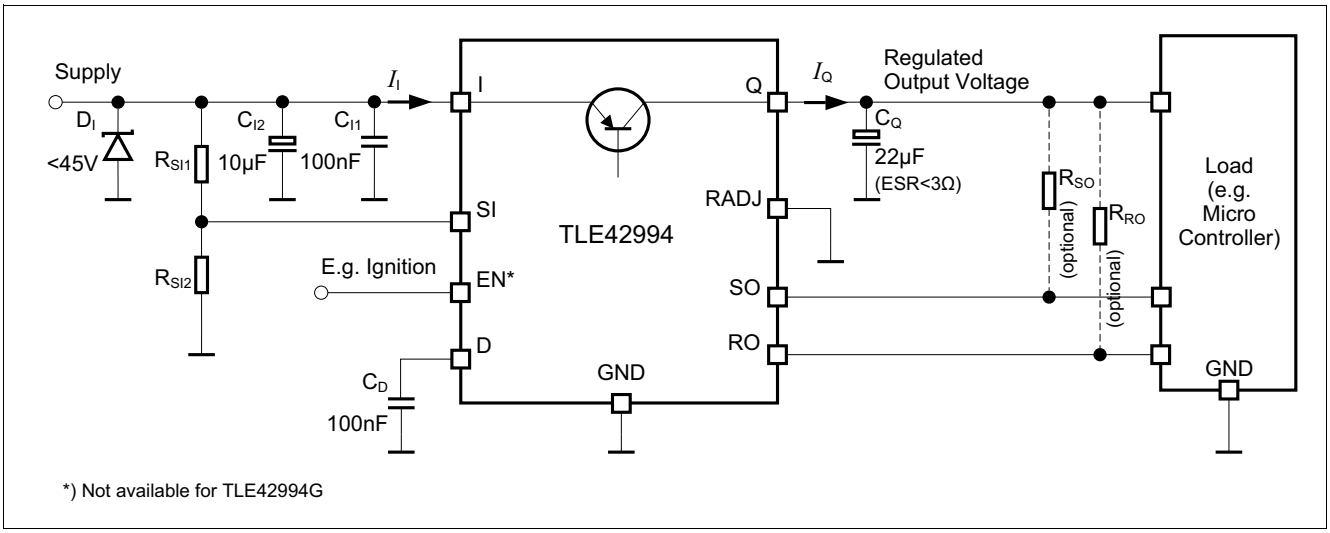


Figure 8 Application diagram with selecting default reset thresholds

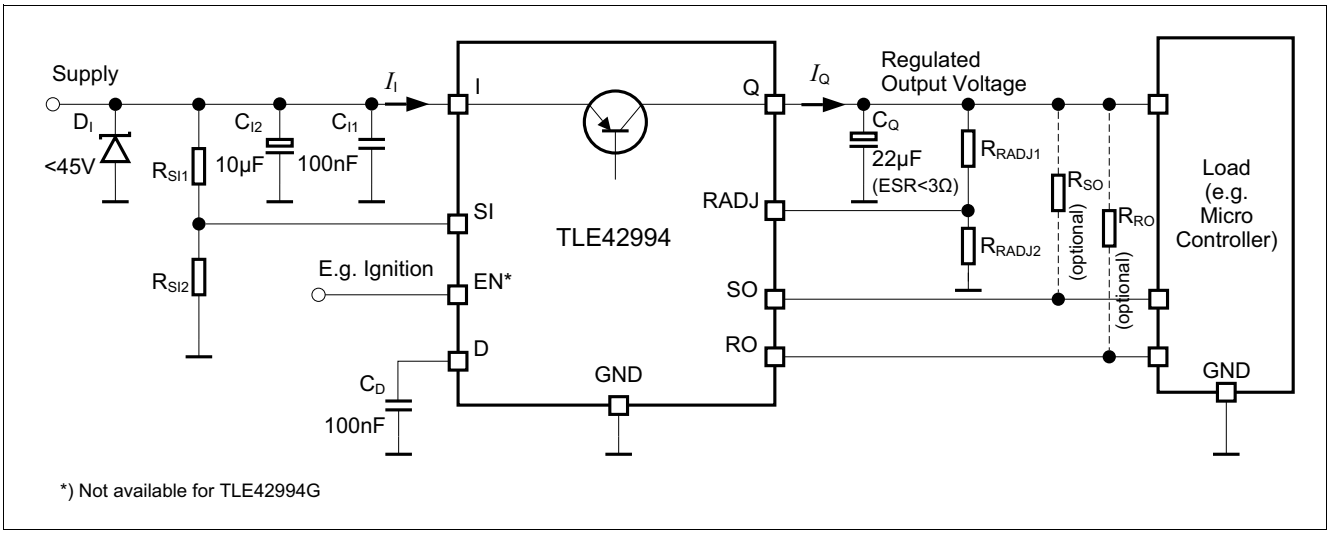


Figure 9 Application diagram with reset thresholds adjustment

6.2 Selection of external components

6.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

6.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional range” on Page 9**. The graph shows the stable operation range of the device.**“Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ” on Page 14**

TLE42994 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

6.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

(6.1)

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

(6.2)

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **“Thermal resistance” on Page 10**.

Example

Application conditions:

V_I= 13.5 V

V_Q= 3.3 V

I_Q= 50 mA

T_a= 105°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \bullet I_Q + V_I \bullet I_q$
$= (13.5\ V - 3.3\ V) \bullet 50\ mA + 13.5\ V \bullet 2\ mA$
$0.510\ W + 0.027\ W$
$= 0.537\ W$

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$
$= (150°C - 105°C) / 0.537\ W$
$= 83.8\ K/W$

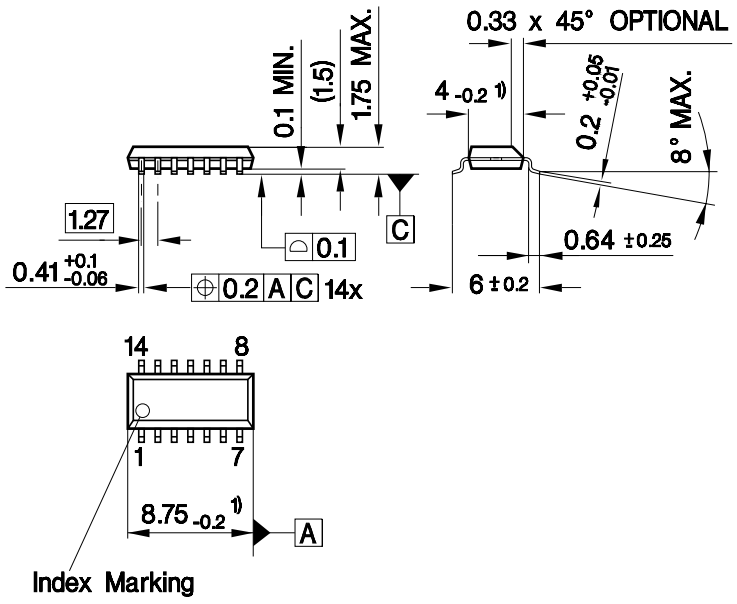
As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 55.3 K/W. By considering TLE42994E (PG-SSOP-14 EP package) and according to **“Thermal resistance” on Page 10**, at least 600 mm² heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

6.4 Reverse polarity protection

TLE42994 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 8** must be kept.

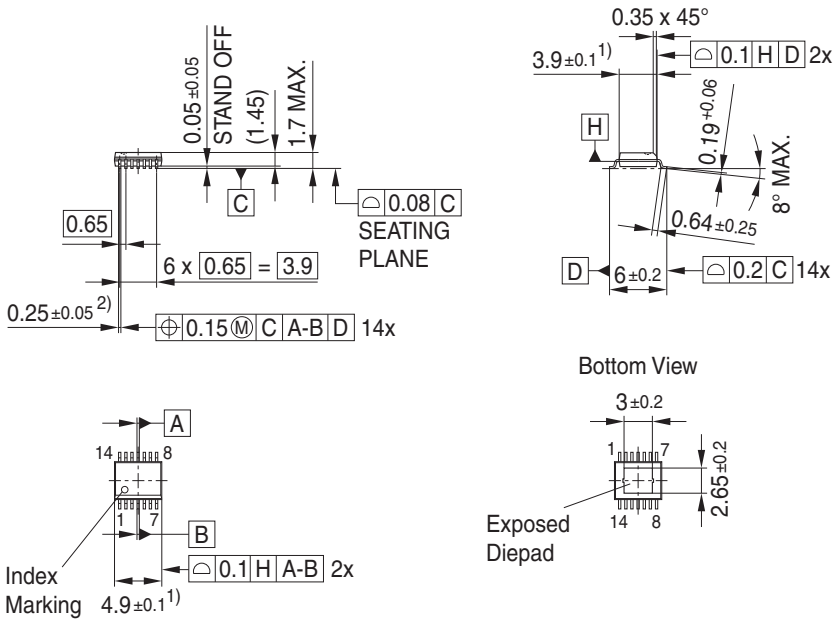
The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

7 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 10 PG-DSO-14[1)]



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

Figure 11 PG-SSOP-14 Exposed Pad[1)]

1) Dimensions in mm

Package information

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

8 Revision History

Revision	Date	Changes
1.2	2018-11-22	Updated layout Updated package drawing “PG-DSO-14” Editorial changes
1.01	2010-10-14	Page 10. pos. 5.1.1: editorial change typ 3.0 V corrected 3.30 V
1.0	2010-10-01	Initial version Data Sheet

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