THS4281 Very Low-Power, High-Speed, Rail-to-Rail Input and Output Voltage-Feedback Operational Amplifier

1 Features

- Very Low Quiescent Current: 750 µA (at 5 V)
- Rail-to-Rail Input and Output:
  - Common-Mode Input Voltage Extends 400 mV Beyond the Rails
  - Output Swings Within 150 mV From the Rails
- Wide –3-dB Bandwidth at 5 V:
  - 90 MHz at Gain = +1, 40 MHz at Gain = +2
- High Slew Rate: 35 V/µs
- Fast Settling Time (2-V Step):
  - 78 ns to 0.1%
  - 150 ns to 0.01%
- Low Distortion at Gain = +2, V_O = 2-V_{PP}, 5 V:
  - –91 dBc at 100 kHz, –67 dBc at 1 MHz
- Input Offset Voltage: 2.5 mV (Max at +25°C)
- Output Current > 30 mA (10-Ω Load, 5 V)
- Low Voltage Noise of 12.5 nV/$\sqrt{\text{Hz}}$
- Supply Voltages: +2.7 V, 3 V, +5 V, ±5 V, +15 V
- Packages: SOT23, MSOP, and SOIC

2 Applications

- Portable/Battery-Powered Applications
- High Channel Count Systems
- ADC Buffer
- Active Filters
- Current Sensing

3 Description

Fabricated using the BiCom-II process, the THS4281 is a low-power, rail-to-rail input and output, voltage-feedback operational amplifier designed to operate over a wide power-supply range of 2.7-V to 15-V single supply, and ±1.35-V to ±7.5-V dual supply. Consuming only 750 µA with a unity gain bandwidth of 90 MHz and a high 35-V/µs slew rate, the THS4281 allows portable or other power-sensitive applications to realize high performance with minimal power. To ensure long battery life in portable applications, the quiescent current is trimmed to be less than 900 µA at +25°C, and 1 mA from –40°C to +85°C.

The THS4281 is a true single-supply amplifier with a specified common-mode input range of 400 mV beyond the rails. This allows for high-side current sensing applications without phase reversal concerns. Its output swings to within 40 mV from the rails with 10-kΩ loads, and 150 mV from the rails with 1-kΩ loads.

The THS4281 has a good 0.1% settling time of 78 ns, and 0.01% settling time of 150 ns. The low THD of –87 dBc at 100 kHz, coupled with a maximum offset voltage of less than 2.5 mV, makes the THS4281 a good match for high-resolution ADCs sampling less than 2 MSPS.

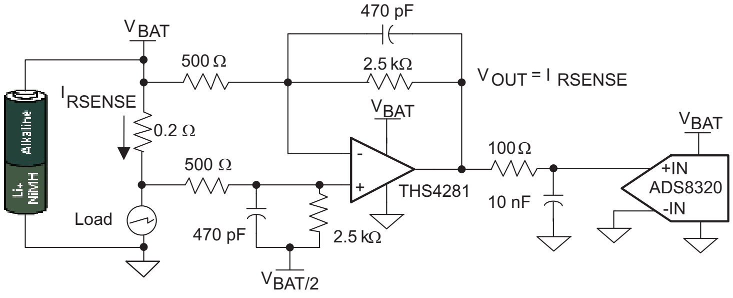
The THS4281 is offered in a space-saving SOT23-5 package, a small MSOP-8 package, and the industry standard SOIC-8 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4281	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

High-side, Low Power Current-Sensing system



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed the *Packaging/Ordering Information* table ... 1
- Removed *Design Tools* section ... 1
- Updated Thermal Values ... 1
- Removed the *Applications Section Contents* section ... 24
- Removed the *Bill of Materials* section ... 24

Changes from Original (April 2004) to Revision A **Page**

- Updated document format to current standards ... 1
- Deleted *Lead temperature* specification from Absolute Maximum Ratings table ... 4
- Revised *Driving Capacitive Loads* section ... 26
- Changed *Board Layout* section; revised statements in fourth recommendation about how to make connections to other wideband devices on the board ... 29

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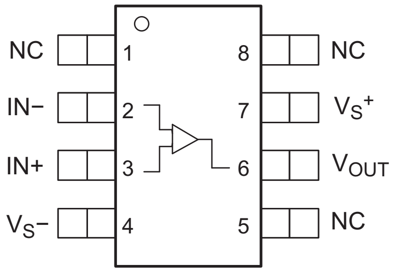
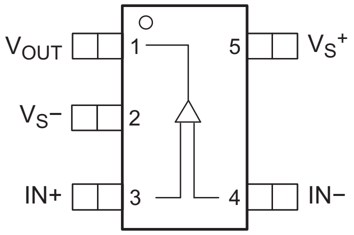
5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC
Top View



DBV Package
5-Pin SOT-23
Top View



Note: NC Indicates there is no internal connection to these pins

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	SOT-23		
NC	1	—	—	
IN-	2	4	I	Negative input voltage pin
IN+	3	3	I	Positive input voltage pin
Vs-	4	2	I/O	Negative supply input voltage pin
NC	5	—	—	
V_{out}	6	1	O	Output voltage pin
Vs+	7	5	I/O	Postive supply input voltage pin
NC	8	—	—	

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

	MIN	MAX	UNIT
Supply voltage, V_{S-} to V_{S+}		16.5	V
Input voltage, V_I		$\pm V_S \pm 0.5$	V
Differential input voltage, V_{ID}		±2	V
Output current, I_O		±100	mA
Continuous power dissipation	See *Dissipation Ratings* Table		
Maximum junction temperature, any condition, (2) T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(2) T_J		125°	°C
Storage temperature, T_{stg}	–65	150	°C

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. recommended operating conditions.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine Model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±8.25	V
	Single supply	2.7	16.5	

6.4 Thermal Information

THERMAL METRIC(1)		THS4281			UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	154.4	126.6	192.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	69	77.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	64.7	112.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	20.5	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31	64.3	111.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) This data was taken using the JEDEC standard High-K test PCB.

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6.5 Electrical Characteristics, V_S = 3 V (V_{S+} = 3 V, V_{S-} = GND)

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ to 1.5 V, T_A = 25°C unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-Signal Bandwidth	G = +1, V_O = 100 mV_{PP}, R_F = 34 Ω			83		MHz
	G = +2, V_O = 100 mV_{PP}, R_F = 1.65 kΩ			40		MHz
	G = +5, V_O = 100 mV_{PP}, R_F = 1.65 kΩ			8		MHz
	G = +10, V_O = 100 mV_{PP}, R_F = 1.65 kΩ			3.8		MHz
0.1-dB Flat Bandwidth	G = +2, V_O = 100 mV_{PP}, R_F = 1.65 kΩ			20		MHz
Full-Power Bandwidth	G = +2, V_O = 2 V_{PP}			8		MHz
Slew Rate	G = +1, V_O = 2-V Step			26		V/µs
	G = –1, V_O = 2-V Step			27		V/µs
Settling time to 0.1%	G = –1, V_O = 1-V Step			80		ns
Settling time to 0.01%	G = –1, V_O = 1-V Step			155		ns
Rise/Fall Times	G = +1, V_O = 2-V Step			55		ns
AC PERFORMANCE— HARMONIC DISTORTION						
Second Harmonic Distortion	G = +2, V_O = 2 V_{PP}, f = 1 MHz, R_L = 1 kΩ			–52		dBc
	G = +2, V_O = 2 V_{PP}, f = 100 kHz, RL = 1 kΩ			–52		
Third Harmonic Distortion	G = +2, V_O = 2 V_{PP}, f = 1 MHz, RL = 1 kΩ			–69		dBc
	G = +2, V_O = 2 V_{PP}, f = 100 kHz, RL = 1 kΩ			–71		
THD + N	G = +2, V_O = 2 V_{PP}, VO = 1 VPP, f = 10 kHz			0.003%		
	G = +2, V_O = 2 V_{PP}, VO = 2 VPP, f = 10 kHz			0.03%		
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω			0.05/0.08 %		
Differential Phase (NTSC/PAL)	G = +2, R_L = 150 Ω			0.25/0.35		º
Input Voltage Noise	f = 100 kHz			12.5		nA/√Hz
Input Current Noise	f = 100 kHz			1.5		pA/√Hz
DC PERFORMANCE						
Open-Loop Voltage Gain (AOL)				95		dB
Input Offset Voltage	V_{CM} = 1.5 V	25°C		0.5	2.5	mV
		0°C to 70°C			3.5	
		–40°C to +85°C			3.5	
Average Offset Voltage Drift	V_{CM} = 1.5 V	0°C to 70°C			±7	µV/°C
		–40°C to +85°C			±7	
Input Bias Current	V_{CM} = 1.5 V	25°C		0.5	0.8	µA
		0°C to 70°C			1	
		–40°C to +85°C			1	
Average Bias Current Drift	V_{CM} = 1.5 V	0°C to 70°C		±2		nA/°C
		–40°C to +85°C		±2		
Input Offset Current	V_{CM} = 1.5 V	25°C		0.1	0.4	µA
		0°C to 70°C			0.5	
		–40°C to +85°C			0.5	
Average Offset Current Drift	V_{CM} = 1.5 V	0°C to 70°C			±2	nA/°C
		–40°C to +85°C			±2	
INPUT CHARACTERISTICS						
Common-Mode Input Range	25°C		–0.3/3.3	–0.4/3.4		V
	0°C to 70°C		–0.1/3.1			
	–40°C to +85°C		–0.1/3.1			
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	25°C	75	92		dB
		0°C to 70°C	70			
		–40°C to +85°C	70			
Input Resistance	Common-mode			100		MΩ
Input Capacitance	Common-mode/Differential			0.8/1.2		pF

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Electrical Characteristics, V_S = 3 V (V_{S+} = 3 V, V_{S-} = GND) (continued)

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ to 1.5 V, T_A = 25°C unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 10 kΩ			0.04/2.96		V
	R_L = 1 kΩ	25°C	0.14/2.86	0.1/2.9		V
		0°C to 70°C	0.2/2.8			
		–40°C to +85°C	0.2/2.8			
Output Current (Sourcing)	R_L = 10 Ω	25°C	18	23		mA
		0°C to 70°C	15			
		–40°C to +85°C	15			
Output Current (Sinking)	R_L = 10 Ω	25°C	22	29		mA
		0°C to 70°C	19			
		–40°C to +85°C	19			
Output Impedance	f = 1 MHz			1		Ω
POWER SUPPLY						
Maximum Operating Voltage	25°C			3	16.5	V
	0°C to 70°C				16.5	
	–40°C to +85°C				16.5	
Minimum Operating Voltage	25°C		2.7	3		V
	0°C to 70°C		2.7			
	–40°C to +85°C		2.7			
Maximum Quiescent Current	25°C			0.75	0.9	mA
	0°C to 70°C				0.98	
	–40°C to +85°C				1	
Minimum Quiescent Current	25°C		0.6	0.75		mA
	0°C to 70°C		0.57			
	–40°C to +85°C		0.55			
Power-Supply Rejection (+PSRR)	V_{S+} = 3.25 V to 2.75 V, V_{S-} = 0 V	25°C	70	90		dB
		0°C to 70°C	65			
		–40°C to +85°C	65			
Power-Supply Rejection (–PSRR)	V_{S+} = 3 V, V_{S-} = 0 V to 0.65 V	25°C	70	90		dB
		0°C to 70°C	65			
		–40°C to +85°C	65			

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6.6 Electrical Characteristics, V_S = 5 V (V_{S+} = 5 V, $V_{S–}$ = GND)

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ to 2.5 V, T_A = 25°C unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-Signal Bandwidth	G = +1, V_O = 100 mV_{PP}, R_F = 34 Ω			90		MHz
	G = +2, V_O = 100 mV_{PP}, R_F = 2 kΩ			40		MHz
	G = +5, V_O = 100 mV_{PP}, R_F = 2 kΩ			8		MHz
	G = +10, V_O = 100 mV_{PP}, R_F = 2 kΩ			3.8		MHz
0.1-dB Flat Bandwidth	G = +2, V_O = 100 mV_{PP}, R_F = 2 kΩ			20		MHz
Full-Power Bandwidth	G = +2, V_O = 2 V_{PP}			9		MHz
Slew Rate	G = +1, V_O = 2-V Step			31		V/μs
	G = –1, V_O = 2-V Step			34		V/μs
Settling Time to 0.1%	G = –1, V_O = 2-V Step			78		ns
Settling Time to 0.01%	G = –1, V_O = 2-V Step			150		ns
Rise/Fall Times	G = +1, V_O = 2-V Step			48		ns
AC PERFORMANCE— HARMONIC DISTORTION						
Second Harmonic Distortion	G = +2, V_O = 2 V_{PP}, f = 1 MHz, R_L = 1 kΩ			–67		dBc
	G = +2, V_O = 2 V_{PP}, f = 100 kHz, R_L = 1 kΩ			–92		
Third Harmonic Distortion	G = +2, V_O = 2 V_{PP}, f = 1 MHz, R_L = 1 kΩ			–76		dBc
	G = +2, V_O = 2 V_{PP}, f = 100 kHz, R_L = 1 kΩ			–106		
THD + N	G = +2, V_O = 2 V_{PP}, V_O = 2 V_{PP}, f = 10 kHz			0.0009%		
	G = +2, V_O = 2 V_{PP}, V_O = 4 V_{PP}, f = 10 kHz			0.0005%		
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω			0.11/0.17%		
Differential Phase (NTSC/PAL)				0.11/0.14		º
Input Voltage Noise	f = 100 kHz			12.5		nV/√Hz
Input Current Noise	f = 100 kHz			1.5		pA/√Hz
DC PERFORMANCE						
Open-Loop Voltage Gain (AOL)	25°C		85	105		dB
	0°C to 70°C		80			
	–40°C to +85°C		80			
Input Offset Voltage	V_{CM} = 2.5 V	25°C		2.5	0.5	mV
		0°C to 70°C			3.5	
		–40°C to +85°C			3.5	
Average Offset Voltage Drift	V_{CM} = 2.5 V	0°C to 70°C		±7		μV/°C
		–40°C to +85°C		±7		
Input Bias Current	V_{CM} = 2.5 V	25°C		0.5	0.8	μA
		0°C to 70°C			1	
		–40°C to +85°C			1	
Average Bias Current Drift	V_{CM} = 2.5 V	0°C to 70°C		±2		nA/°C
		–40°C to +85°C		±2		
Input Offset Current	V_{CM} = 2.5 V	25°C		0.1	0.4	μA
		0°C to 70°C			0.5	
		–40°C to +85°C			0.5	
Average Offset Current Drift	V_{CM} = 2.5 V	0°C to 70°C		±2		nA/°C
		–40°C to +85°C		±2		
INPUT CHARACTERISTICS						
Common-Mode Input Range	25°C		–0.4/5.4	–0.3/5.3		V
	0°C to 70°C		–0.1/5.1			
	–40°C to +85°C		–0.1/5.1			

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Electrical Characteristics, V_S = 5 V (V_{S+} = 5 V, V_{S-} = GND) (continued)

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ to 2.5 V, T_A = 25°C unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Common-Mode Rejection Ratio	V_{CM} = 0 V to 5 V	25°C	85	100		dB
		0°C to 70°C	80			
		–40°C to +85°C	80			
Input Resistance	Common-mode			100		MΩ
Input Capacitance	Common-mode/Differential			0.8/1.2		pF
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 10 kΩ			0.04/4.96		V
	R_L = 1 kΩ	25°C	0.2/4.8	0.15/4.85		V
		0°C to 70°C	0.25/4.75			
		–40°C to +85°C	0.25/4.75			
Output Current (Sourcing)	R_L = 10 Ω	25°C	24	33		mA
		0°C to 70°C	20			
		–40°C to +85°C	20			
Output Current (Sinking)	R_L = 10 Ω	25°C	30	44		mA
		0°C to 70°C	25			
		–40°C to +85°C	25			
Output Impedance	f = 1 MHz	25°C		1		Ω
		0°C to 70°C				
		–40°C to +85°C				
POWER SUPPLY						
Maximum Operating Voltage	25°C			5	16.5	V
	0°C to 70°C				16.5	
	–40°C to +85°C				16.5	
Minimum Operating Voltage	25°C		2.7	5		V
	0°C to 70°C		2.7			
	–40°C to +85°C		2.7			
Maximum Quiescent Current	25°C			0.75	0.9	mA
	0°C to 70°C				0.98	
	–40°C to +85°C				1.0	
Minimum Quiescent Current	25°C		0.6	0.75		mA
	0°C to 70°C		0.57			
	–40°C to +85°C		0.55			
Power-Supply Rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V	25°C	80	100		dB
		0°C to 70°C	75			
		–40°C to +85°C	75			
Power-Supply Rejection (–PSRR)	V_{S+} = 5 V, V_{S-} = 0 V to 1.0 V	25°C	80	100		dB
		0°C to 70°C	75			
		–40°C to +85°C	75			

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6.7 Electrical Characteristics, V_S = ±5 V

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ, unless otherwise noted

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-Signal Bandwidth	G = +1, V_O = 100 mV_{PP}, R_F = 34 Ω			95		MHz
	G = +2, V_O = 100 mV_{PP}			40		MHz
	G = +5, V_O = 100 mV_{PP}			8		MHz
	G = +10, V_O = 100 mV_{PP}			3.8		MHz
0.1-dB Flat Bandwidth	G = +2, V_O = 100 mV_{PP}			20		MHz
Full-Power Bandwidth	G = +1, V_O = 2 V_{PP}			9.5		MHz
Slew Rate	G = +1, V_O = 2-V Step			35		V/µs
	G = –1, V_O = 2-V Step			35		V/µs
Settling Time to 0.1%	G = –1, V_O = 2-V Step			78		ns
Settling Time to 0.01%	G = –1, V_O = 2-V Step			140		ns
Rise/Fall Times	G = +1, V_O = 2-V Step			45		ns
AC PERFORMANCE— HARMONIC DISTORTION						
Second Harmonic Distortion	G = +2, V_O = 2 $V_{PP,}$ f = 1 MHz, R_L = 1 kΩ			–69		dBc
	G = +2, V_O = 2 $V_{PP,}$ f = 100 kHz, R_L = 1 kΩ			–76		
Third Harmonic Distortion	G = +2, V_O = 2 $V_{PP,}$ f = 1 MHz, R_L = 1 kΩ			–93		dBc
	G = +2, V_O = 2 $V_{PP,}$ f = 100 kHz, R_L = 1 kΩ			–107		
THD + N	G = +2, V_O = 2 $V_{PP,}$ V_O = 2 V_{PP}, f = 10 kHz			0.0009		
	G = +2, V_O = 2 $V_{PP,}$ V_O = 4 V_{PP}, f = 10 kHz			0.0003%		
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω			0.03/0.03 %		
Differential Phase (NTSC/PAL)				0.08/0.1		º
Input Voltage Noise	f = 100 kHz			12.5		nV/√Hz
Input Current Noise	f = 100 kHz			1.5		pA/√Hz
DC PERFORMANCE						
Open-Loop Voltage Gain (AOL)	25°C		90	108		dB
	0°C to 70°C		85			
	–40°C to +85°C		85			
Input Offset Voltage	V_{CM} = 0 V	25°C		0.5	2.5	mV
		0°C to 70°C			3.5	
		–40°C to +85°C			3.5	
Average Offset Voltage Drift	V_{CM} = 0 V	0°C to 70°C		±7		µV/°C
		–40°C to +85°C		±7		
Input Bias Current	V_{CM} = 0 V	25°C		0.5	0.8	µA
		0°C to 70°C			1	
		–40°C to +85°C			1	
Average Bias Current Drift	V_{CM} = 0 V	0°C to 70°C		±2		nA/°C
		–40°C to +85°C		±2		
Input Offset Current	V_{CM} = 0 V	25°C		0.1	0.4	µA
		0°C to 70°C			0.5	
		–40°C to +85°C			0.5	
Average Offset Current Drift	V_{CM} = 0 V	0°C to 70°C		±2		nA/°C
		–40°C to +85°C		±2		

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Electrical Characteristics, V_S = ±5 V (continued)

At G = +2, R_F = 2.49 kΩ, and R_L = 1 kΩ, unless otherwise noted

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Common-Mode Input Range	25°C		±5.3	±5.4		V
	0°C to 70°C		±5.1			
	–40°C to +85°C		±5.1			
Common-Mode Rejection Ratio	V_{CM} = –5 V to +5 V	25°C	90	107		dB
		0°C to 70°C	85			
		–40°C to +85°C	85			
Input Resistance	Common-mode			100		MΩ
Input Capacitance	Common-mode/Differential			0.8/1.2		pF
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 10 kΩ			±4.93		V
	R_L = 1 kΩ	25°C	±4.6	±4.8		V
		0°C to 70°C	±4.5			
		–40°C to +85°C	±4.5			
Output Current (Sourcing)	R_L = 10 Ω	25°C	35	48		mA
		0°C to 70°C	30			
		–40°C to +85°C	30			
Output Current (Sinking)	R_L = 10 Ω	25°C	45	60		mA
		0°C to 70°C	40			
		–40°C to +85°C	40			
Output Impedance	f = 1 MHz			1		Ω
POWER SUPPLY						
Maximum Operating Voltage	25°C			±5	±8.25	V
	0°C to 70°C				±8.25	
	–40°C to +85°C				±8.25	
Minimum Operating Voltage	25°C		±1.35	±5		V
	0°C to 70°C		±1.35			
	–40°C to +85°C		±1.35			
Maximum Quiescent Current	25°C			0.8	0.93	mA
	0°C to 70°C				1.0	
	–40°C to +85°C				1.05	
Minimum Quiescent Current	25°C		0.67	0.8		mA
	0°C to 70°C		0.62			
	–40°C to +85°C		0.6			
Power-Supply Rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 5.0 V	25°C	80	100		dB
		0°C to 70°C	75			
		–40°C to +85°C	75			
Power-Supply Rejection (–PSRR)	V_{S+} = 5 V, V_{S-} = –5.5 V to –4.5 V	25°C	80	100		dB
		0°C to 70°C	75			
		–40°C to +85°C	75			

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6.8 Dissipation Ratings

PACKAGE	POWER RATING (1)	
	T_A < +25°C	T_A = +85°C
DBV (5)	391 mW	156 mW
D (8)	1.02 W	410 mW
DGK (8)	553 mW	221 mW

(1) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long term reliability.

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6.9 Typical Characteristics

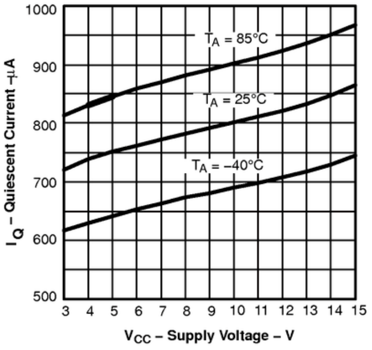
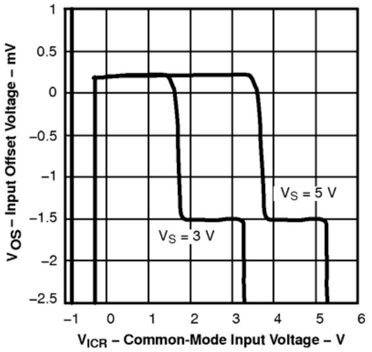
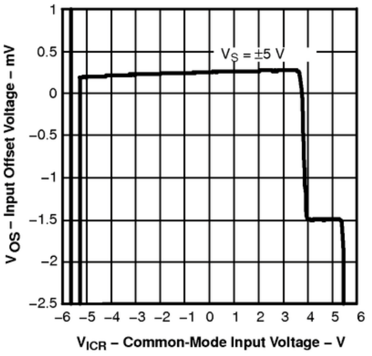


Figure 1. Quiescent Current vs Supply Voltage



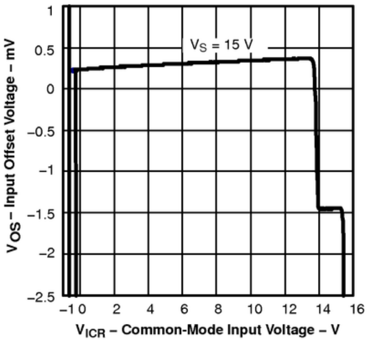
V_S = 3 V V_S = 5 V

Figure 2. Input Offset Voltage vs Common-mode Input Voltage



V_S = ±5 V

Figure 3. Input Offset Voltage vs Common-Mode Input Voltage



V_S = 15 V

Figure 4. Input Offset Voltage vs Common-Mode Input Voltage

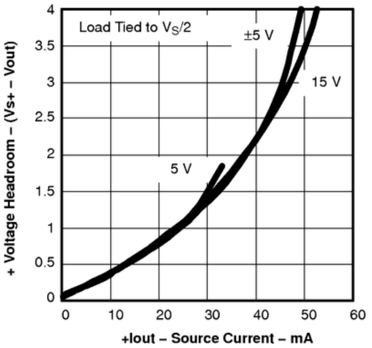


Figure 5. Positive Voltage Headroom vs Source Current

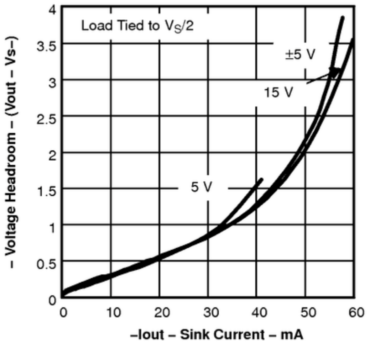


Figure 6. Negative Voltage Headroom vs Sink Current

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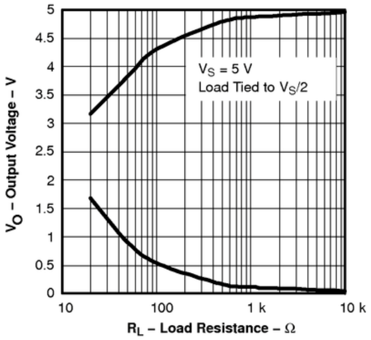
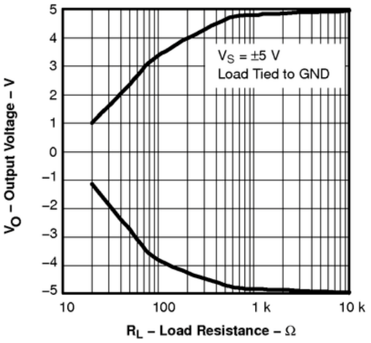
Typical Characteristics (continued)



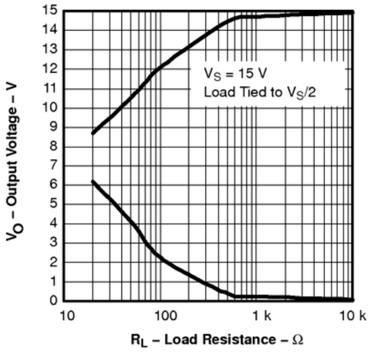
V_S = 5 V

Figure 7. Output Voltage vs Load Resistance



V_S = ±5 V

Figure 8. Output Voltage vs Load Resistance



V_S = 15 V)

Figure 9. Output Voltage vs Load Resistance

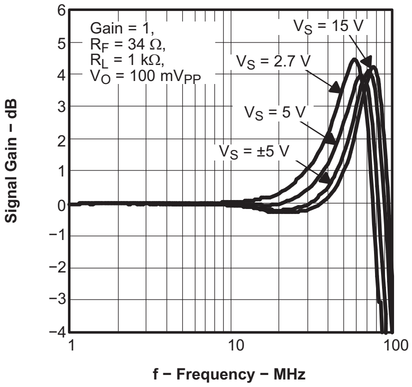
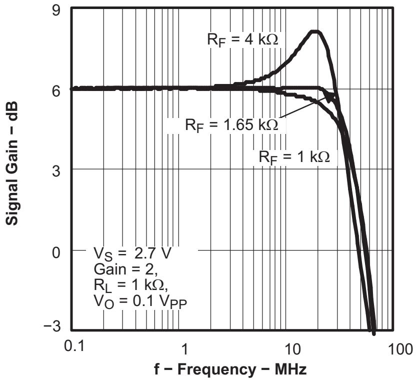
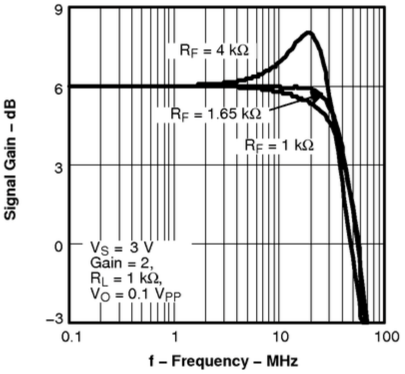


Figure 10. Frequency Response



V_S = 2.7 V

Figure 11. Frequency Response



V_S = 3 V

Figure 12. Frequency Response

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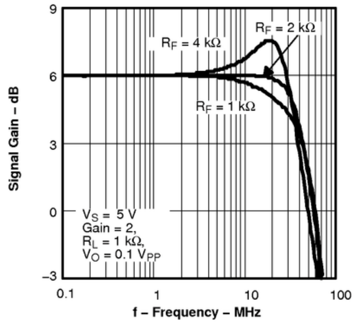
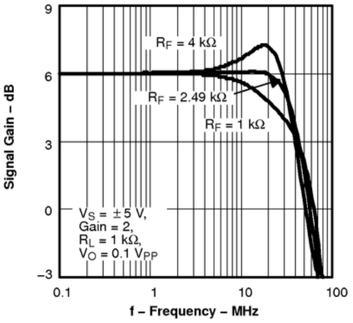
Typical Characteristics (continued)



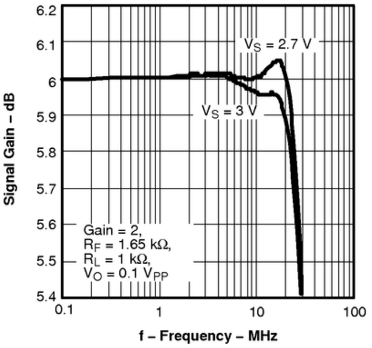
V_S = 5 V

Figure 13. Frequency Response



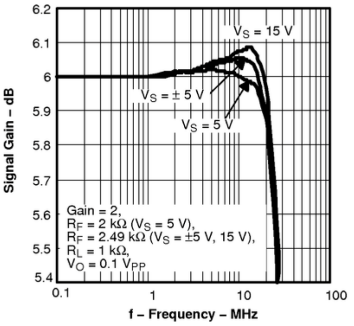
V_S = ±5 V

Figure 14. Frequency Response



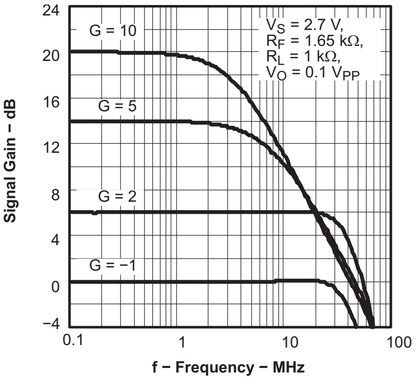
V_S = 2.7 V V_S = 3 V

Figure 15. 0.1-dB Frequency Response



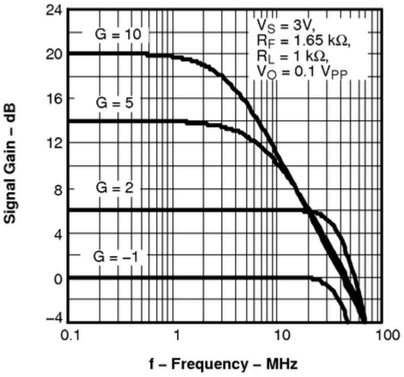
V_S = 5 V, ±5 V, 15 V

Figure 16. 0.1-dB Frequency Response



V_S = 2.7 V

Figure 17. Frequency Response



V_S = 3 V

Figure 18. Frequency Response

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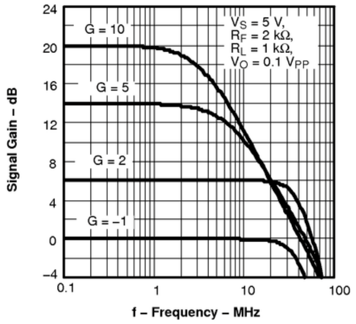
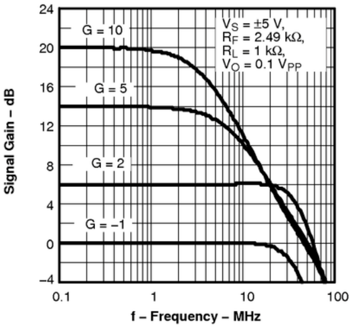
Typical Characteristics (continued)



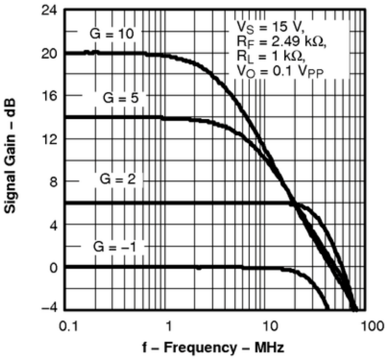
V_S = 5 V

Figure 19. Frequency Response



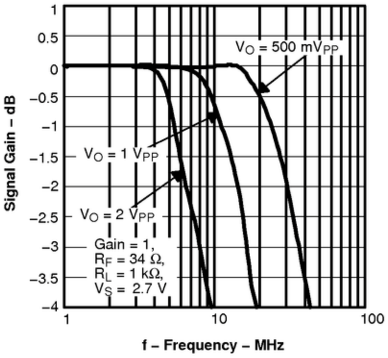
V_S = ±5 V

Figure 20. Frequency Response



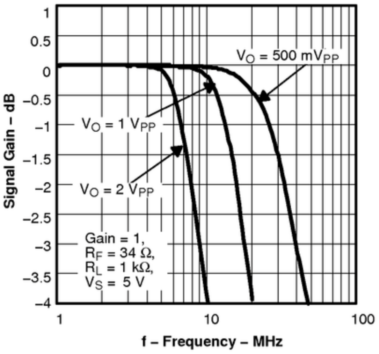
V_S = 15 V

Figure 21. Frequency Response



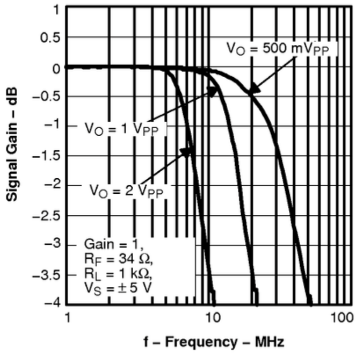
V_S = 2.7 V

Figure 22. Large-Signal Frequency Response



V_S = 5 V

Figure 23. Large-Signal Frequency Response



V_S = ±5 V

Figure 24. Large-Signal Frequency Response

Typical Characteristics (continued)

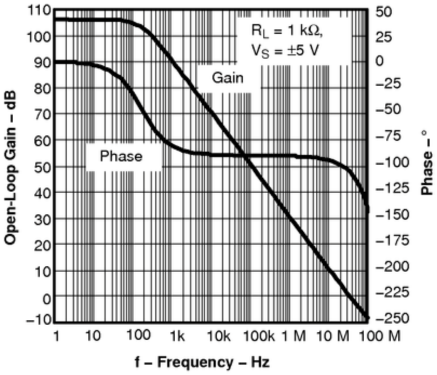


Figure 25. Open-Loop Gain vs Frequency

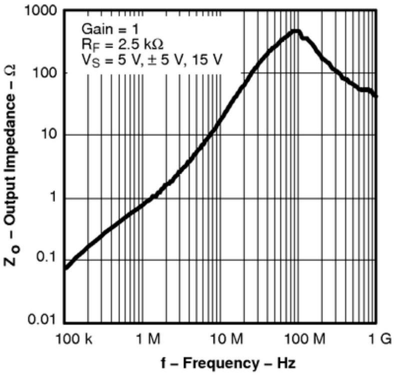


Figure 26. Output Impedance vs Frequency

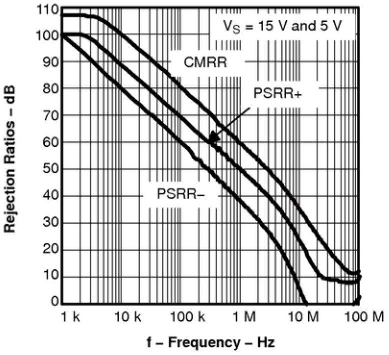


Figure 27. Rejection Ratio vs Frequency

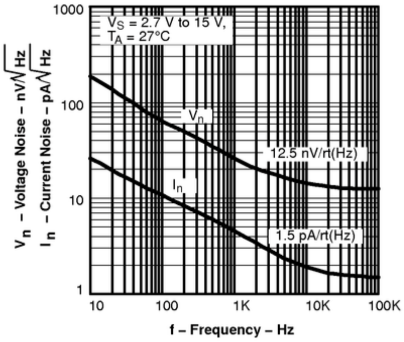
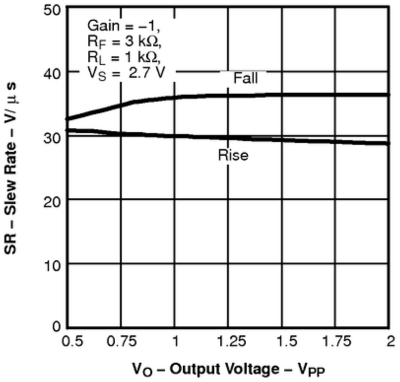
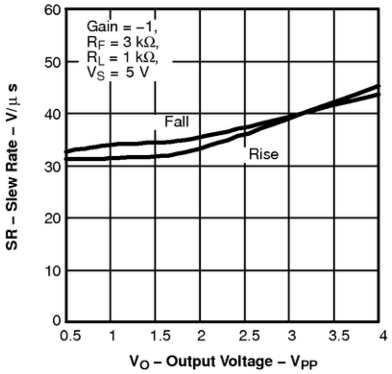


Figure 28. Noise vs Frequency



V_S = 2.7 V

Figure 29. Slew Rate



V_S = 5 V

Figure 30. Slew Rate

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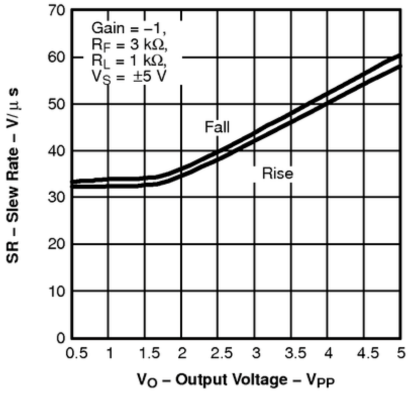
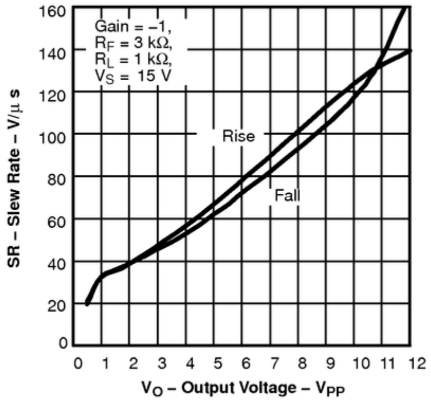
Typical Characteristics (continued)



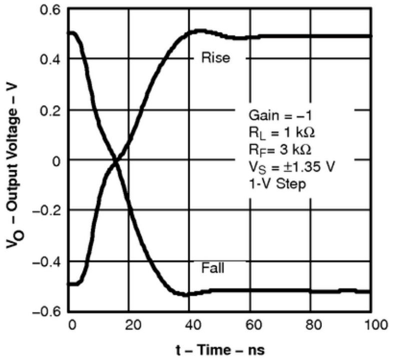
V_S = ±5 V

Figure 31. Slew Rate



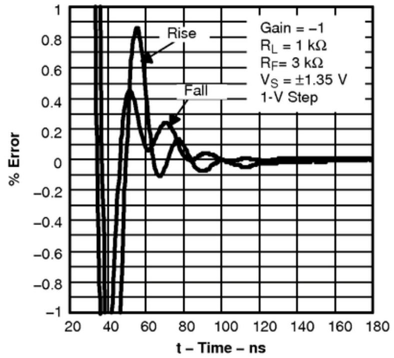
V_S = 15 V

Figure 32. Slew Rate



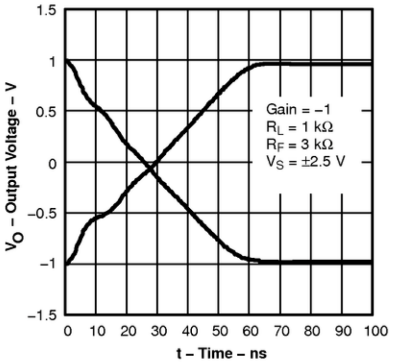
V_S = ±1.35 V

Figure 33. Settling Time



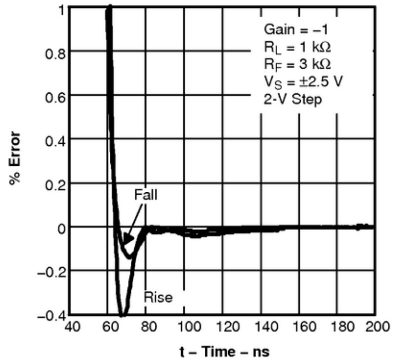
V_S = ±1.35 V

Figure 34. Settling Time



V_S = ±2.5 V

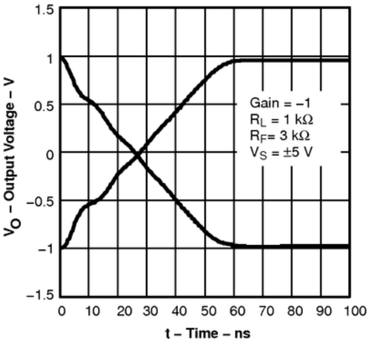
Figure 35. Settling Time



V_S = ±2.5 V

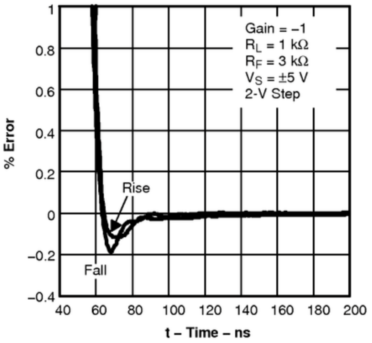
Figure 36. Settling Time

Typical Characteristics (continued)



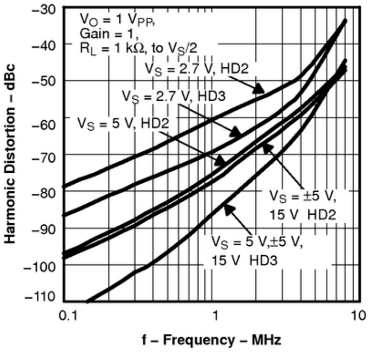
V_S = ±5 V

Figure 37. Settling Time



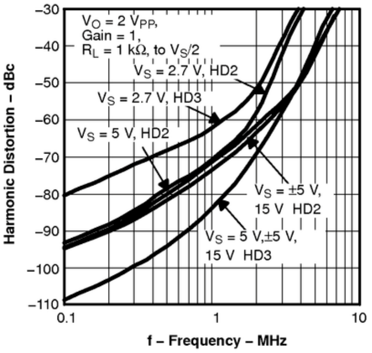
V_S = ±5 V

Figure 38. Settling Time



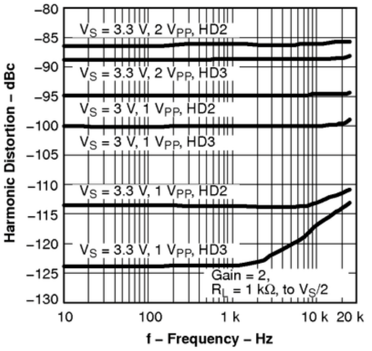
Gain = +1

Figure 39. Harmonic Distortion vs Frequency



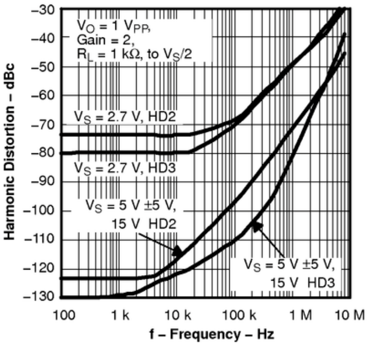
Gain = +1

Figure 40. Harmonic Distortion vs Frequency



V_S = 3 V, 3.3 V

Figure 41. Harmonic Distortion vs Frequency



Gain = +2

Figure 42. Harmonic Distortion vs Frequency

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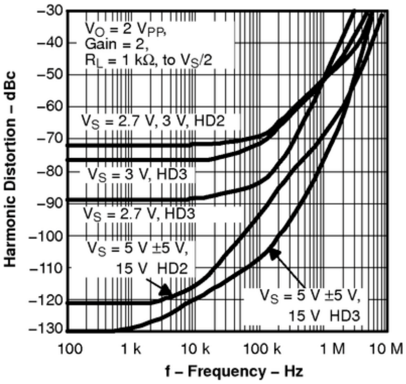
Typical Characteristics (continued)



Gain = +2

Figure 43. Harmonic Distortion vs Frequency

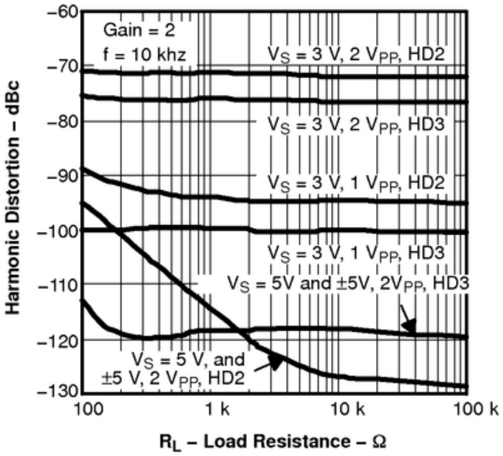
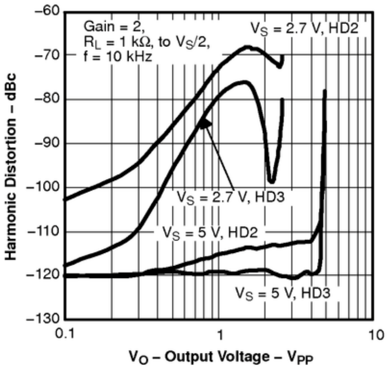


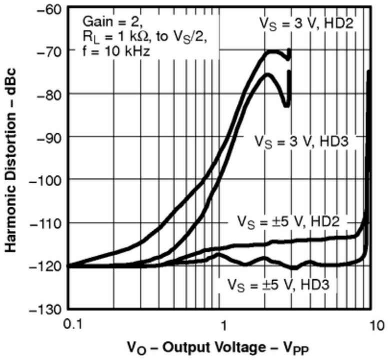
Figure 44. Harmonic Distortion vs Load Resistance



\

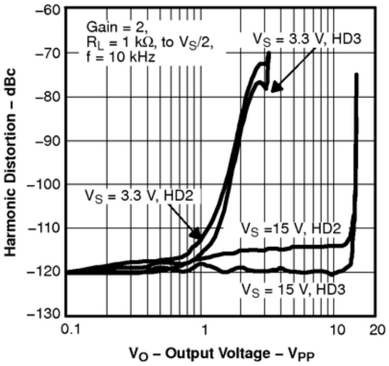
V_S = 2.7 V, 5 V

Figure 45. Harmonic Distortion vs Output Voltage



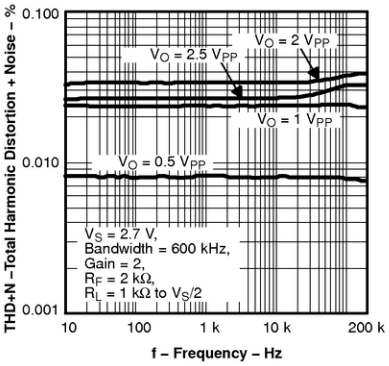
V_S = 3 V, ±5 V

Figure 46. Harmonic Distortion vs Output Voltage



V_S = 3.3 V, 15 V

Figure 47. Harmonic Distortion vs Output Voltage



V_S = 2.7 V

Figure 48. Total Harmonic Distortion + Noise vs Frequency

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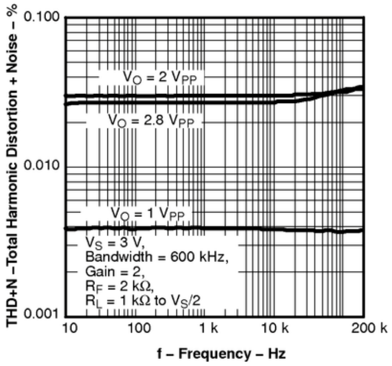
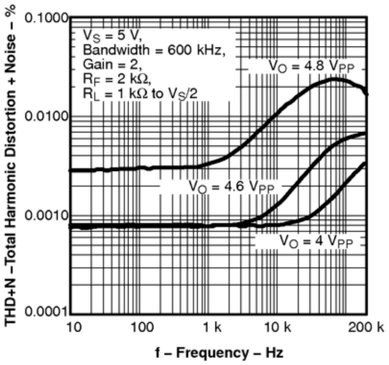
Typical Characteristics (continued)



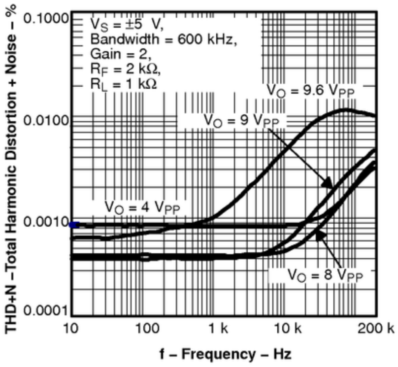
V_S = 3 V

Figure 49. Total Harmonic Distortion + Noise vs Frequency



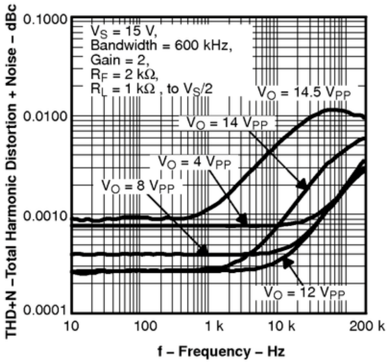
V_S = 5 V

Figure 50. Total Harmonic Distortion + Noise vs Frequency



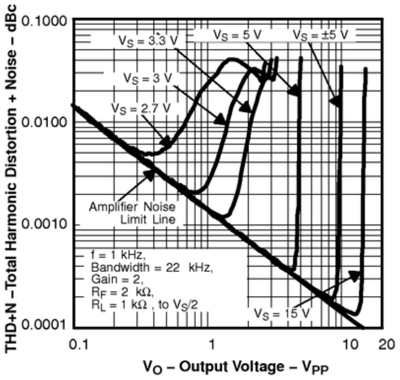
V_S = ±5 V

Figure 51. Total Harmonic Distortion + Noise vs Frequency



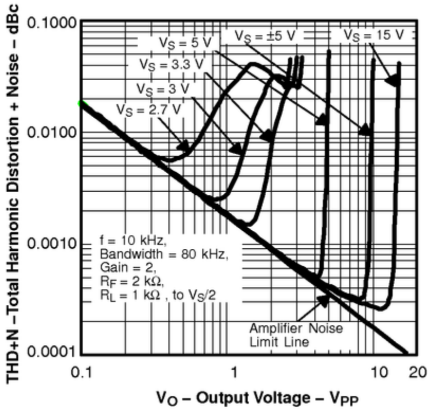
V_S = 15 V

Figure 52. Total Harmonic Distortion + Noise vs Frequency



f = 1 kHz

Figure 53. Total Harmonic Distortion + Noise vs Output Voltage



f = 10 kHz

Figure 54. Total Harmonic Distortion + Noise vs Output Voltage

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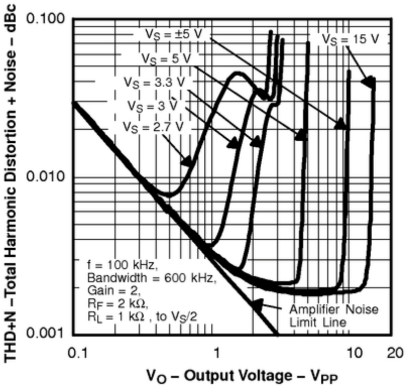
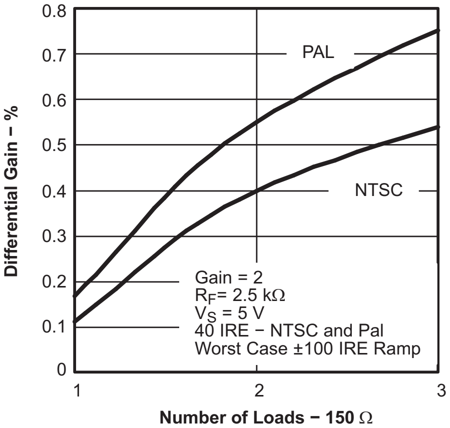
Typical Characteristics (continued)



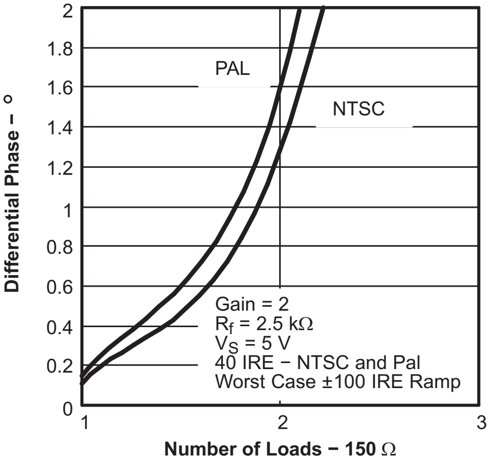
f = 100 kHz

Figure 55. Total Harmonic Distortion + Noise vs Output Voltage



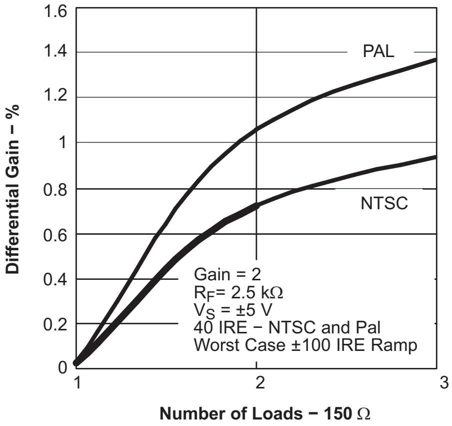
V_S = 5 V

Figure 56. Differential Gain vs Number of Loads



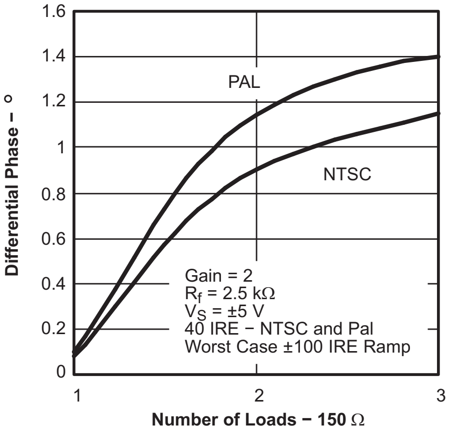
V_S = 5 V

Figure 57. Differential Phase vs Number of Loads



V_S = ±5 V

Figure 58. Differential Gain vs Number of Loads



V_S = ±5 V

Figure 59. Differential Phase vs Number of Loads

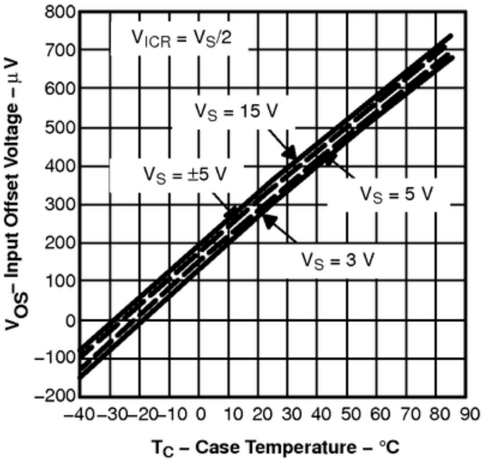


Figure 60. Input Offset Voltage vs Temperature

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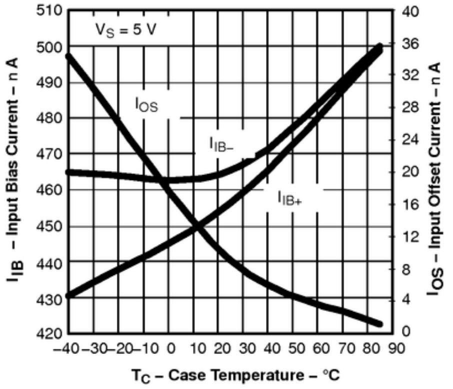
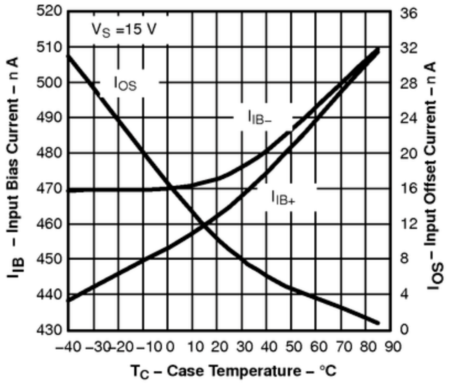
Typical Characteristics (continued)



V_S = 5 V

Figure 61. Input Bias and Offset Current vs Temperature



V_S = 15 V

Figure 62. Input Bias and Offset Current vs Temperature

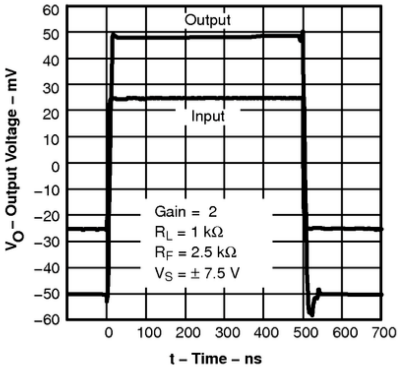


Figure 63. Small-Signal Transient Response

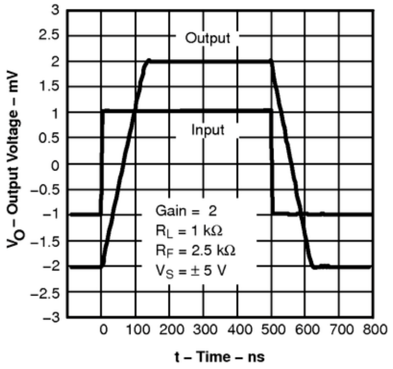
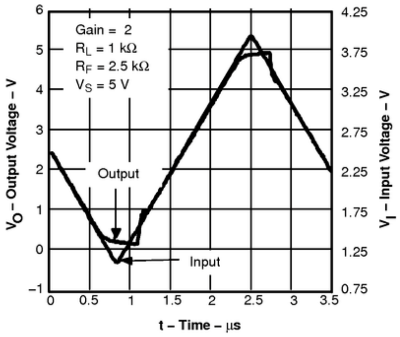
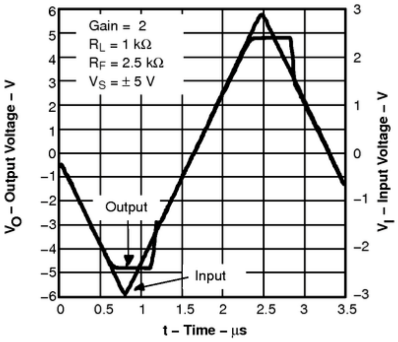


Figure 64. Large-Signal Transient Response



V_S = 5 V

Figure 65. Overdrive Recovery Time



V_S = ±5 V

Figure 66. Overdrive Recovery Time

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Typical Characteristics (continued)

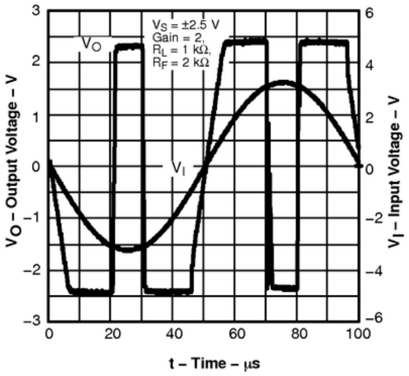

Figure 67. Overdrive Response Output Voltage vs Time

7 Detailed Description

7.1 Overview

7.1.1 High-Speed Operational Amplifiers

The THS4281 is a unity gain stable, rail-to-rail input and output, voltage-feedback operational amplifier designed to operate from a single 2.7-V to 16.5-V power supply.

7.2 Feature Description

7.2.1 Wideband, Noninverting Operation

Figure 68 shows the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves.

Voltage feedback amplifiers can use a wide range of resistors values to set their gain with minimal impact on frequency response. Larger-valued resistors decrease loading of the feedback network on the output of the amplifier, but may cause peaking and instability. For a gain of +2, feedback resistor values between 1 kΩ and 4 kΩ are recommended for most applications. However, as the gain increases, the use of even higher feedback resistors can be used to conserve power. This is due to the inherent nature of amplifiers becoming more stable as the gain increases, at the expense of bandwidth. Figure 73 and Figure 74 show the THS4281 using feedback resistors of 10 kΩ and 100 kΩ. Be cautioned that using such high values with high-speed amplifiers is not typically recommended, but under certain conditions, such as high gain and good high-speed printed circuit board (PCB) layout practices, such resistances can be used.

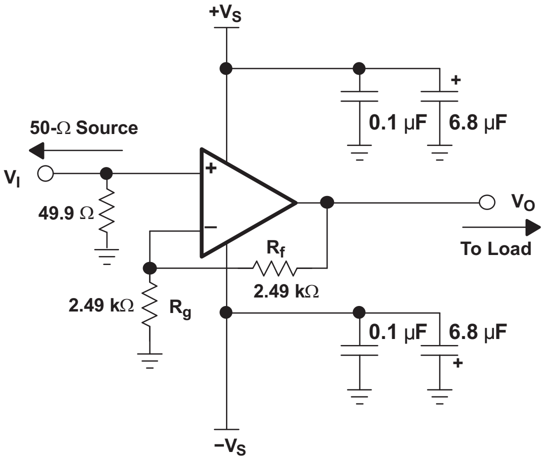

Figure 68. Wideband, Noninverting Gain Configuration

7.2.2 Wideband, Inverting Operation

Figure 69 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 68 are retained with an inverting circuit gain of –1 V/V.

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Feature Description (continued)

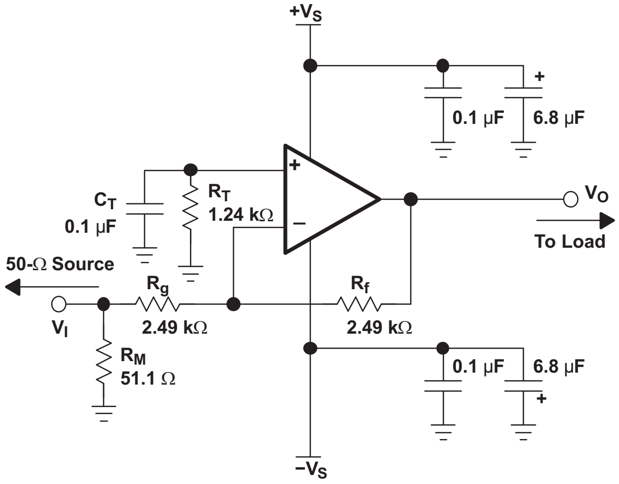

Figure 69. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2, setting R_g to 49.9 Ω for input matching, eliminates the need for R_M but requires a 100-Ω feedback resistor. The 100-Ω feedback resistor, in parallel with the external load, causes excessive loading on the amplifier output. To eliminate this excessive loading, it is preferable to increase both R_g and R_f values, as shown in Figure 69, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance is the parallel combination of R_g and R_M.

Another consideration in inverting amplifier design is setting the bias current cancellation resistor (R_T) on the noninverting input. If the resistance is set equal to the total dc resistance presented to the device at the inverting terminal, the output dc error (due to the input bias currents) is reduced to the input offset current multiplied by R_T. In Figure 69, the dc source impedance presented at the inverting terminal is 2.49 kΩ || (2.49 kΩ + 25.3 Ω) ≈ 1.24 kΩ. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, R_T is bypassed with a 0.1-μF capacitor to ground (C_T).

7.3 Device Functional Modes

This device has no specific function modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Single-Supply Operation

The THS4281 is designed to operate from a single 2.7-V to 16.5-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing and not violate V_{ICR}. The circuits shown in Figure 70 shows inverting and noninverting amplifiers configured for single-supply operation.

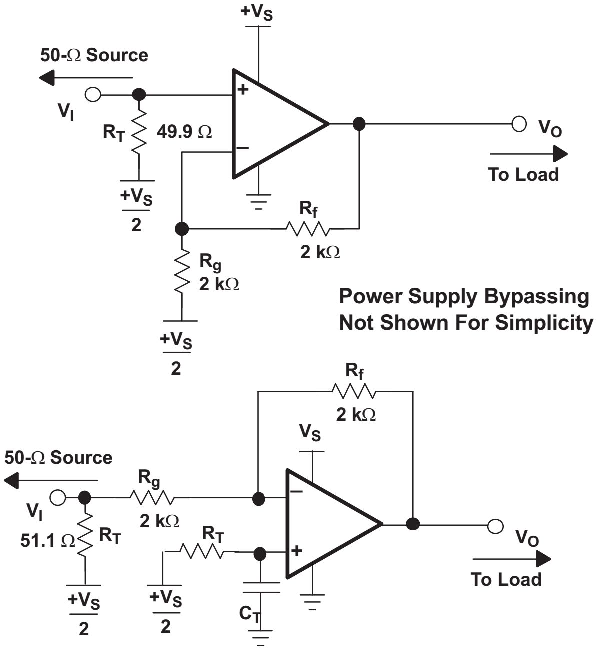

Figure 70. DC-Coupled Single Supply Operation

8.1.2 Driving Capacitive Loads

One of the most demanding, and yet common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4281 can be susceptible to instability and peaking when a capacitive load is placed directly on the output. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the feedback path that decreases the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, a simple and effective solution is to isolate the capacitive load from the feedback loop by inserting a small series isolation resistor (for example, $R_{(ISO)} = 100\ \Omega$ for $C_{LOAD} = 10$ pF to $R_{(ISO)} = 10\ \Omega$ for $C_{LOAD} = 1000$ pF) between the amplifier output and the capacitive load.

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8.2 Typical Application

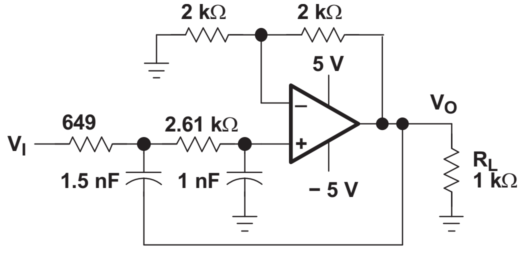

Figure 71. Second-Order Sallen-Key 100-kHz Butterworth Filter, Gain = 2 V/V

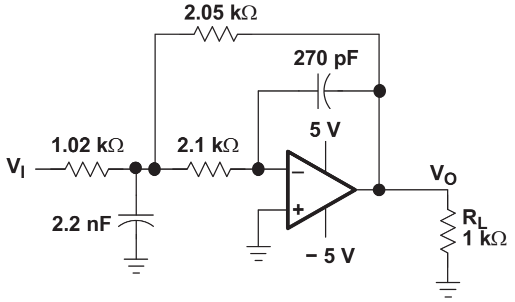

Figure 72. Second-Order MFB 100-kHz Butterworth Filter, Gain = 2 V/V

8.2.1 Design Requirements

Table 1 shows example design parameters and values for the typical application design example in Figure 71.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±5 V
Amplifier topology	Voltage feedback
Gain	2 V/V
Filter requirement	Second Order 100 KHz Sallen- Key Butterworth Filter
Input/Output Requirements	Rail to Rail

8.2.2 Detailed Design Procedure

8.2.2.1 Active Filtering With the THS4281

High-performance active filtering with the THS4281 is achievable due to the amplifier's good slew rate, wide bandwidth, and voltage-feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. Filters can be quite complex and time consuming to design. Several books and application reports are available to help design active filters. But, to help simplify the process and minimize the chance of miscalculations, Texas Instruments has developed a filter design program called FilterPro™. FilterPro is available for download at no cost from TI's web site (www.ti.com).

The two most common low-pass filter circuits used are the Sallen-Key filter and the Multiple Feedback (MFB) – *aka* Rauch filter. FilterPro was used to determine a 2-pole Butterworth response filter with a corner (–3-dB) frequency of 100 kHz, which is shown in Figure 71 and Figure 72. One of the advantages of the MFB filter, a much better high-frequency rejection, is clearly shown in the response shown in Figure 75. This is due to the inherent R-C filter to ground being the first elements in the design of the MFB filter. The Sallen-Key design also has an R-C filter, but the capacitor connects directly to the output. At very high frequencies, where the amplifier's access loop gain is decreasing, the ability of the amplifier to reject high frequencies is severely reduced and allows the high-frequency signals to pass through the system. One other advantage of the MFB filter is the reduced sensitivity in component variation. This is important when using real-world components where capacitors can easily have ±10% variations.

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8.2.3 Application Curves

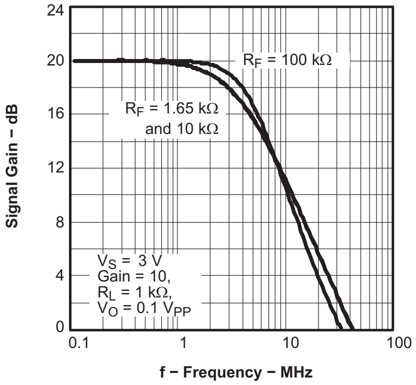

Figure 73. Signal Gain vs Frequency, V_S = 3 V

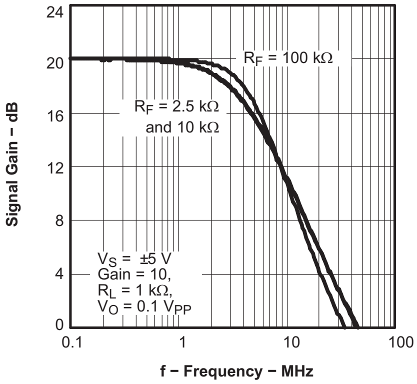

Figure 74. Signal Gain vs Frequency, V_S = ±5 V

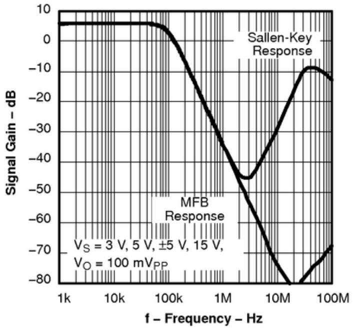

Figure 75. Second-Order 100-kHz Active Filter Response

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9 Power Supply Recommendations

9.1 Power-Supply Decoupling Techniques and Recommendations

Power-supply decoupling is a critical aspect of any high-performance amplifier design. Careful decoupling provides higher quality ac performance. The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power-supply inputs as possible, with the goal of minimizing the inductance.
2. Placement priority should put the smallest valued capacitors closest to the device.
3. Use of solid power and ground planes is recommended to reduce the inductance along power-supply return current paths (with the exception of the areas underneath the input and output pins as noted below).
4. A bulk decoupling capacitor is recommended (6.8 μF to 22 μF) within 1 inch, and a ceramic (0.1 μF) within 0.1 inch of the power input pins.

NOTE

The bulk capacitor may be shared by other operational amplifiers.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the THS4281 requires careful attention to board layout parasitics and external component types. See the EVM layout figures (Figure 76 to Figure 79) in the *Design Tools* section.

Recommendations that optimize performance include:

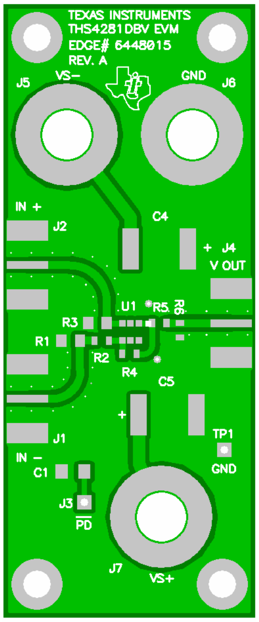
1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability and on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.1-μF decoupling capacitors.** Avoid narrow power and ground traces to minimize inductance. The power-supply connections should always be decoupled as described above.
3. **Careful selection and placement of external components preserves the high-frequency performance of the THS4281.** Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film, axial-lead resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Excessively high resistor values can create significant phase lag that can degrade performance. Keep resistor values as low as possible, consistent with load-driving considerations. It is suggested that a good starting point for design is to set the R_f to 2 kΩ for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms reasonable and minimizes the effect of parasitic capacitance.
4. **Connections to other wideband devices on the board should be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Low parasitic capacitive loads (< 4 pF) may not need an $R_{(ISO)}$, because the THS4281 is nominally compensated to operate at unity gain (+1 V/V) with a 2-pF capacitive load. Higher capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A matching series resistor into the trace from the output of the THS4281 is used as well as a terminating shunt resistor at the input of the destination

Layout Guidelines (continued)

device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and use a series resistor ($R_{(ISO)}$ = 10 Ω to 100 Ω, as noted *Driving Capacitive Loads*) to isolate the capacitive load. If the input impedance of the destination device is low, there is signal attenuation due to the voltage divider formed by $R_{(ISO)}$ into the terminating impedance. A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots.

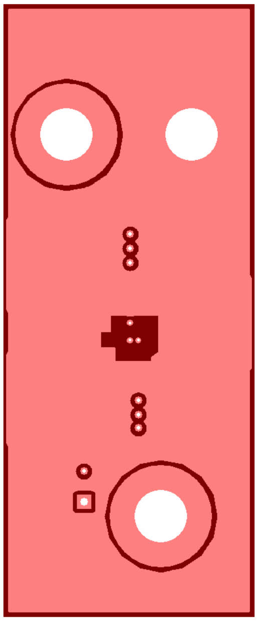
5. **Socketing a high-speed part like the THS4281 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4281 onto the board.

10.2 Layout Examples



TOP

Figure 76. THS4281EVM Layout (Top Layer and Silkscreen Layer)



Layer 2 − GND

Figure 77. THS4281EVM Board Layout

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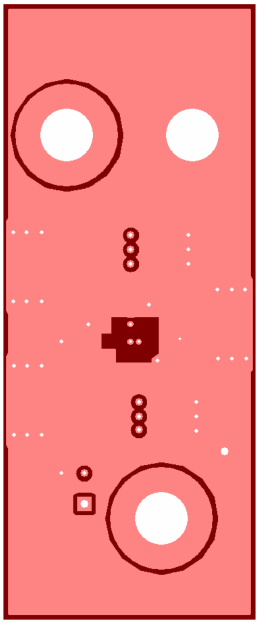
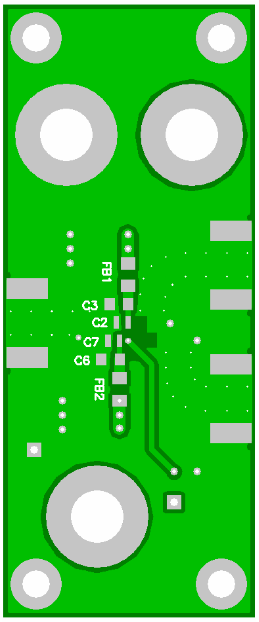
Layout Examples (continued)



Layer 3 − GND

Figure 78. THS4281EVM Board Layout



BOTTOM

Figure 79. THS4281EVM Board Layout

10.3 Thermal Considerations

The THS4281 does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150°C is exceeded. For long-term dependability, the junction temperature should not exceed +125°C.

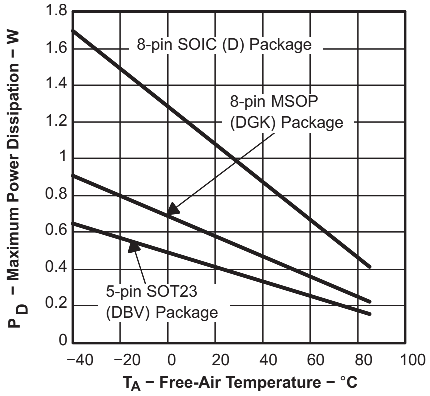
The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = (T_{max} - T_A) / \theta_{JA}$$

where

- P_{Dmax} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junciton temperature (ºC).
- T_A is the ambient temperature (ºC).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ^{JC} is the thermal coefficient from the silicon junctions to the case (ºC/W).
- θ^{JA} is the thermal coefficient from the case to ambient air (ºC/W). (1)

Thermal Considerations (continued)



Θ_{JA} = 97.5°C/W for 8-Pin SOIC (D)
Θ_{JA} = 180.8°C/W for 8-Pin MSOP (DGK)
Θ_{JA} = 255.4°C/W for 5-Pin SOT−23 (DBV)
T_J = 125°C, No Airflow

Figure 80. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS value can provide a reasonable analysis.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *PowerPAD Made Easy*, application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)
- *Active Low-Pass Filter Design*, application report (SLOA049)
- *FilterPro MFB and Sallen-Key Low-Pass Filter Design Program*, application report (SBFA001)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

FilterPro, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4281D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281	Samples
THS4281DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON	Samples
THS4281DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON	Samples
THS4281DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON	Samples
THS4281DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO	Samples
THS4281DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO	Samples
THS4281DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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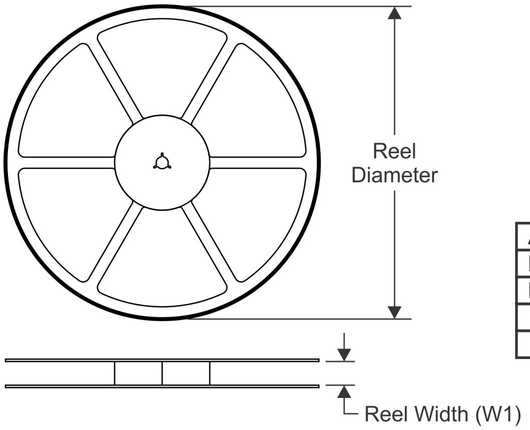
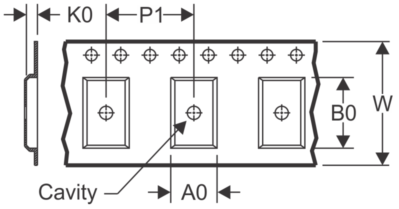
TAPE AND REEL INFORMATION

REEL DIMENSIONS

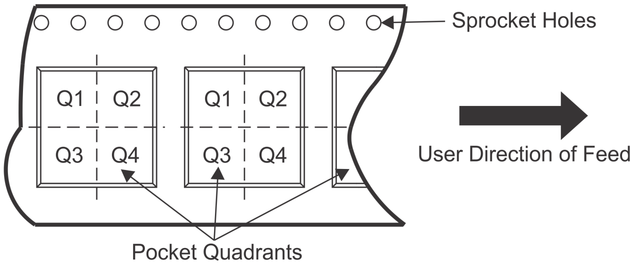


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

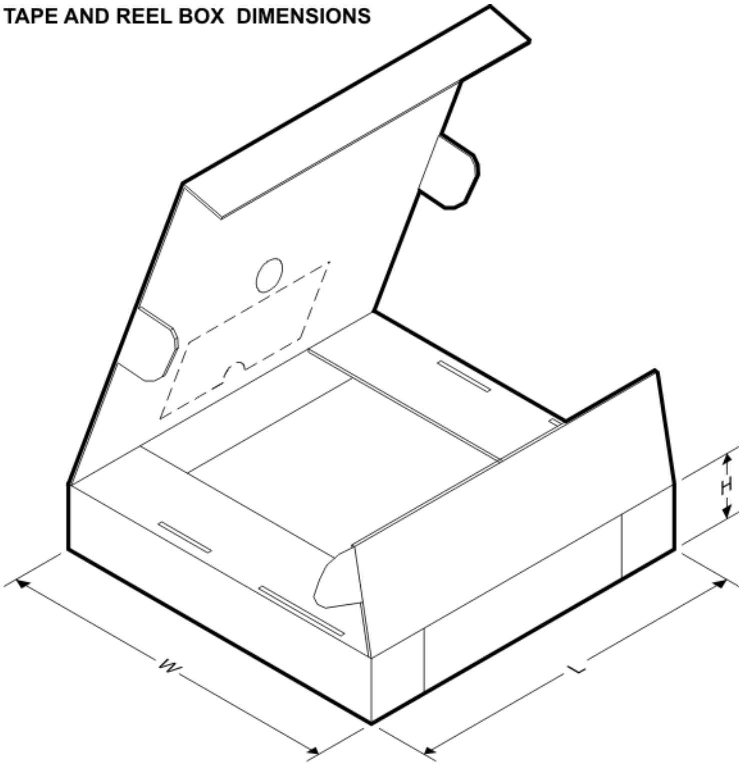
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4281DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4281DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

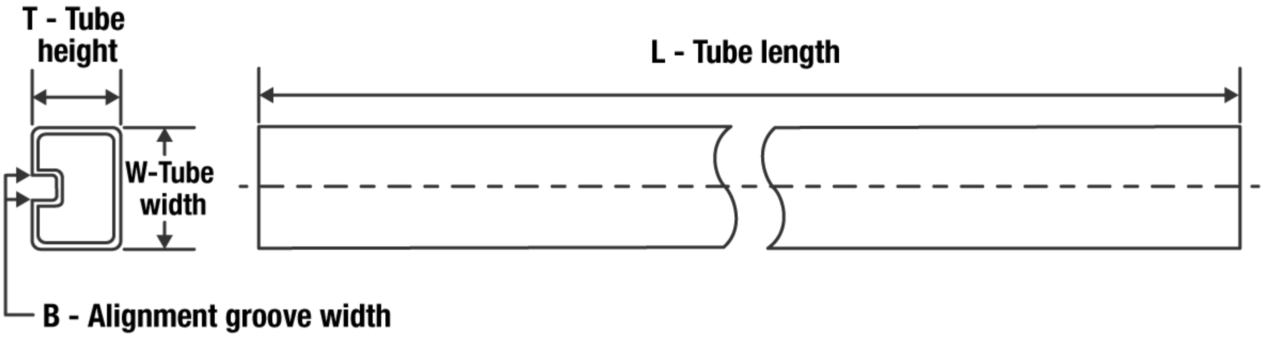
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4281DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
THS4281DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
THS4281DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4281DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



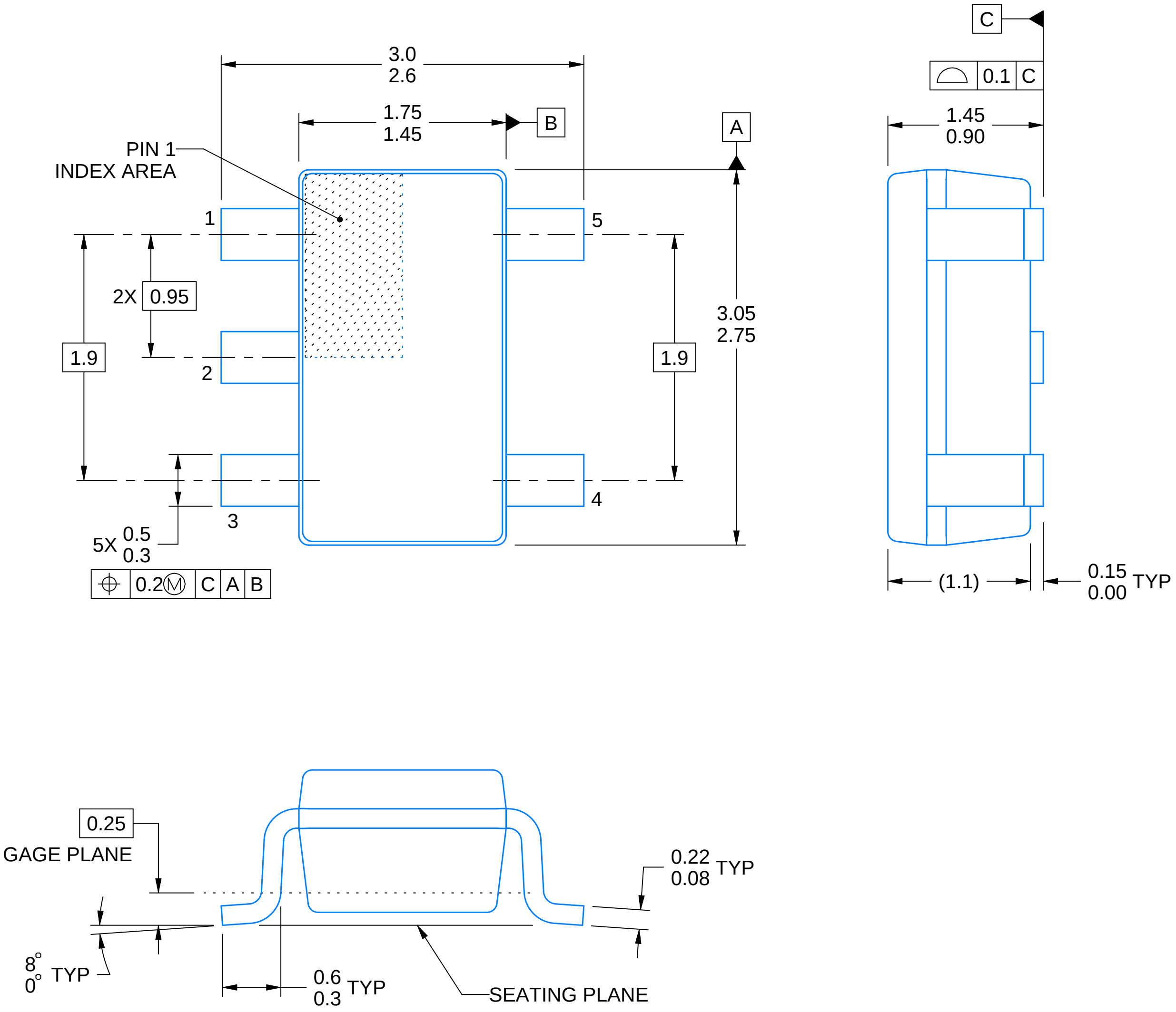
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4281D	D	SOIC	8	75	505.46	6.76	3810	4

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

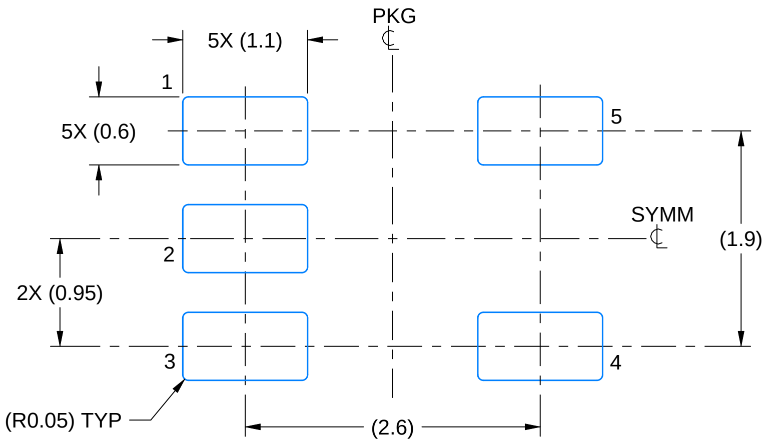
SMALL OUTLINE TRANSISTOR



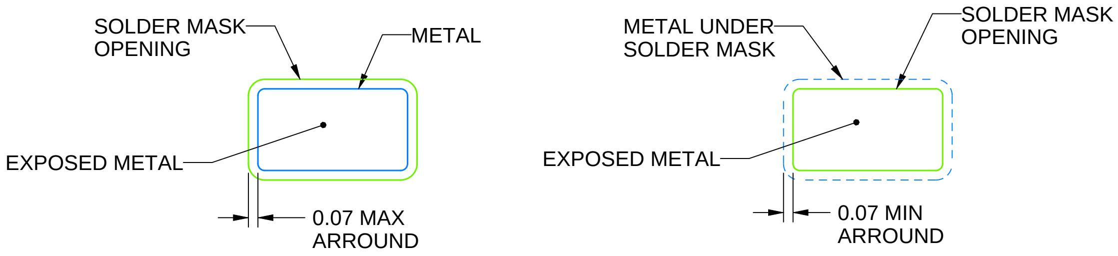
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



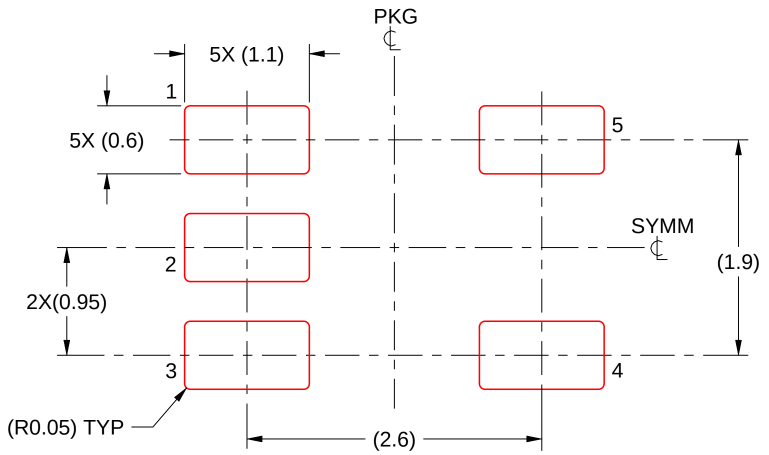
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

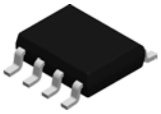
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

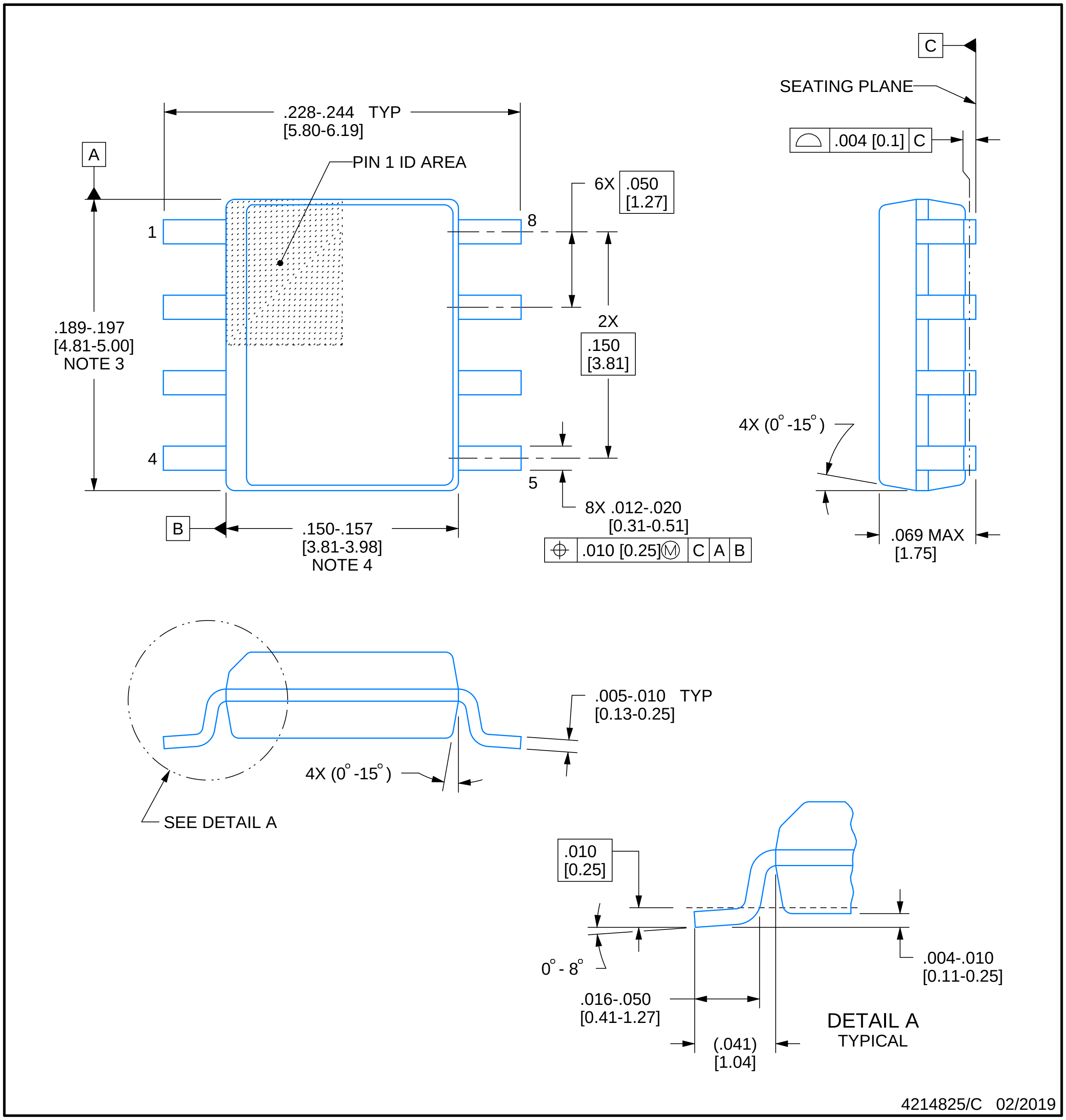


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

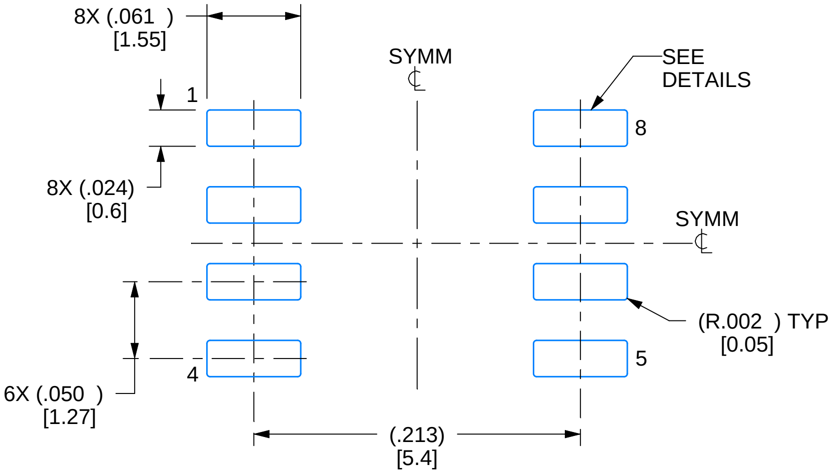
SMALL OUTLINE INTEGRATED CIRCUIT



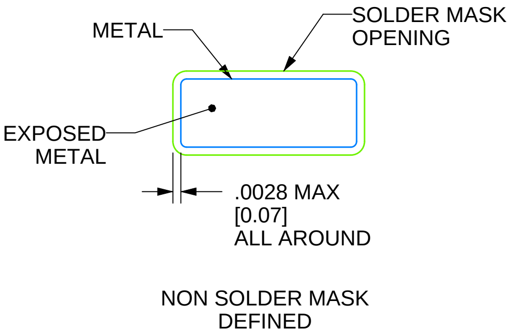
4214825/C 02/2019

NOTES:

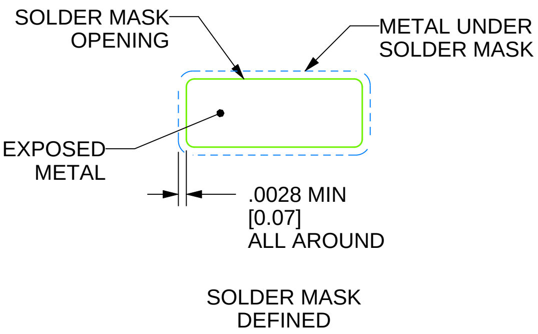
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED



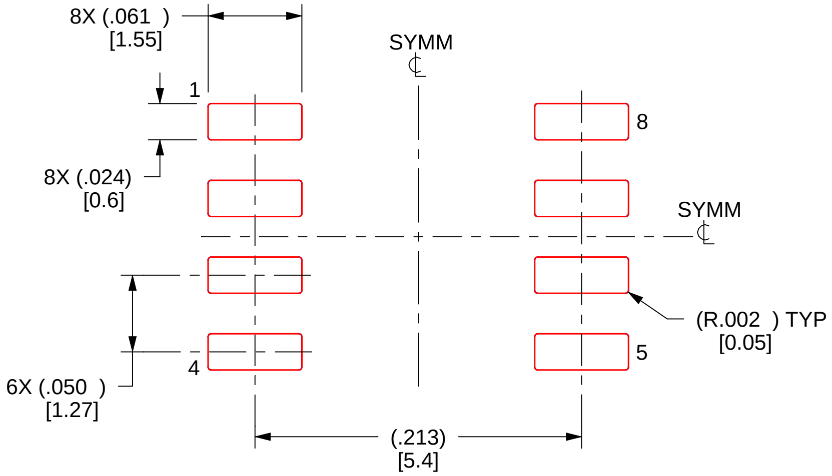
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

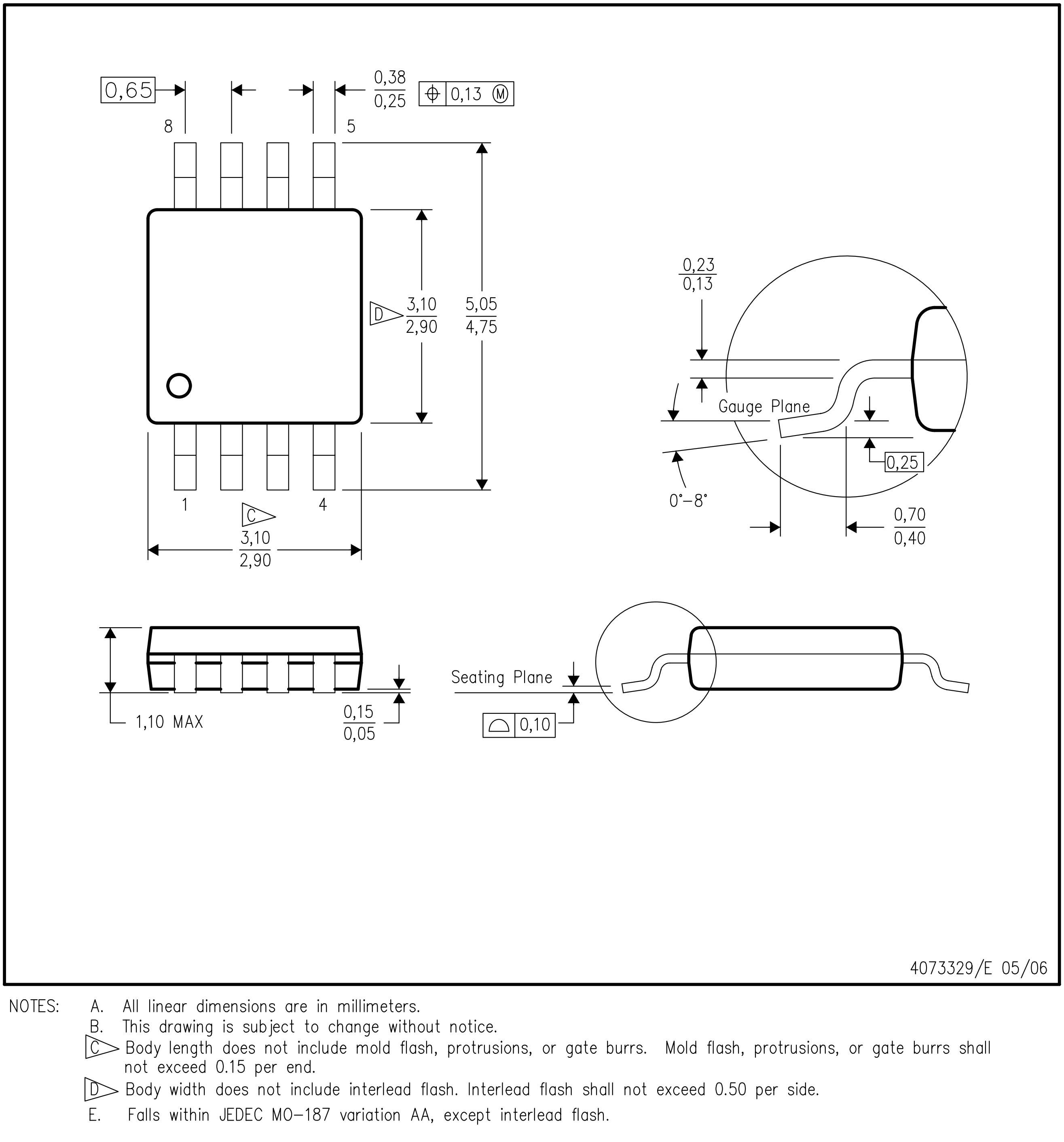


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

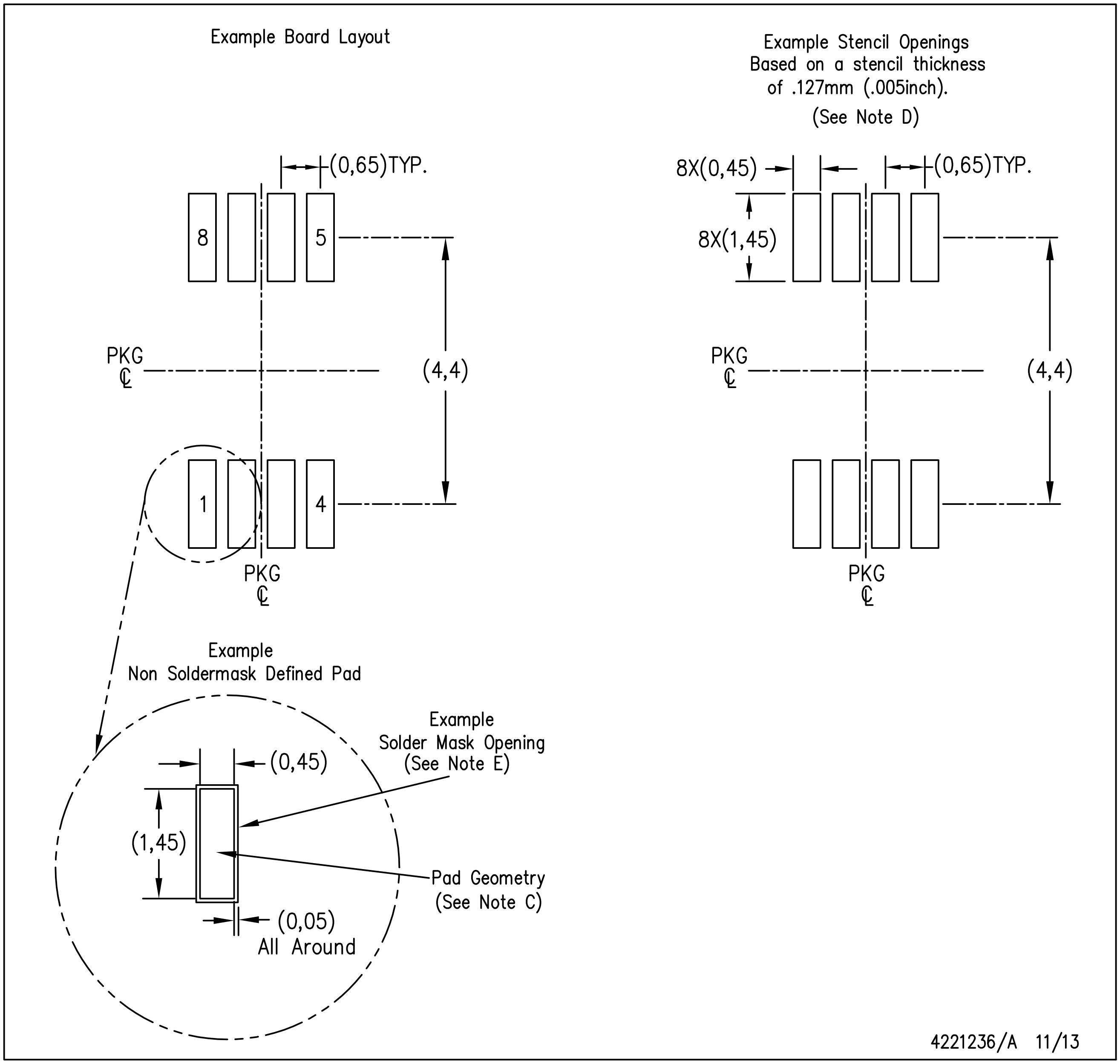
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



4221236/A 11/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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