ARG82801-1

Fully Integrated PMIC for Safety-Related Systems
with Buck or Buck-Boost Pre-Regulator, 4× Linear Regulators, 4× Gate Drivers, and SPI

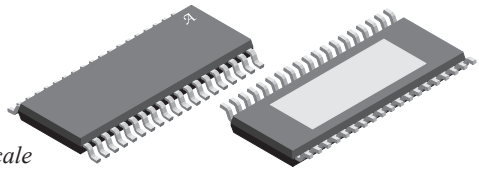
FEATURES AND BENEFITS

- A²-SIL™ product—device features for safety-critical systems
- Automotive AEC-Q100 qualified
- Wide input voltage range, 3.8 to 36 V_{IN} operating range, 40 V_{IN} maximum
- 2.2 MHz buck or buck/boost pre-regulator (VREG: 5.35 V)
- Four internal linear regulators with foldback short-circuit protection
  - □ VUC: selectable output (3.3 V / 5.0 V) regulator for microcontroller
  - □ V5C: 5 V general purpose LDO regulator
  - □ V5P1 and V5P2: two LDO regulators (track VUC voltage) with short-to-battery protection for remote sensors
- Q&A Watchdog and Window Watchdog timer
- Floating gate drivers with charge pump for external isolator NFET control
- Control and diagnostic reporting through a serial peripheral interface (SPI)
- Logic enable input (ENB) for microprocessor control
- Ignition enable input (ENBAT)
- Frequency dithering and controlled slew rate help reduce EMI/EMC
- Undervoltage protection for all output rails
- Thermal shutdown protection
- –40°C to 150°C junction temperature range

APPLICATIONS

- Provides system power for (microcontroller/DSP, CAN, sensors, etc.) and high current isolation FET gate driver in automotive control modules, such as:
  - □ Electronic power steering (EPS)
  - □ Advanced braking systems (ABS)
  - □ Other automotive applications

PACKAGE: 38-Pin eTSSOP (suffix LV)



Not to scale

DESCRIPTION

The ARG82801-1 is a power management IC that integrates a buck or buck/boost pre-regulator, four LDOs, and four floating gate drivers. The pre-regulator uses a buck or buck/boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the pre-regulator supplies a 3.3 V or 5.0 V selectable 350 mA linear regulator, a 5 V / 115 mA linear regulator, and two 120 mA protected linear regulators which track VUC output. Designed to supply power for microprocessors, sensors, and CAN transceivers, the ARG82801-1 is ideal for underhood applications.

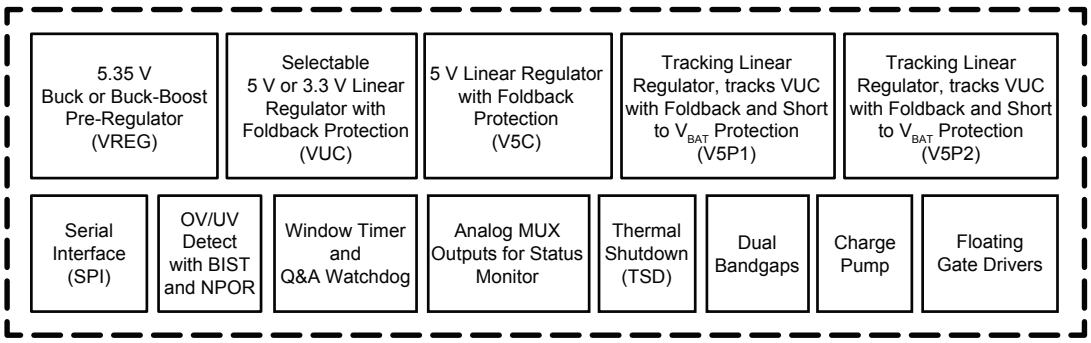
The independent floating gate drivers have the capability of controlling N-channel MOSFETs through SPI. These MOSFETs can be configured as phase or battery isolation devices in high current motor applications. An integrated charge pump allows the driver outputs to maintain the power MOSFETs in the on state over the full supply range with high phase-voltage slew rates.

Enable inputs to the ARG82801-1 include a logic level (ENB) and a high voltage (ENBAT). The ARG82801-1 also provides flexibility with disable function of the individual output rails through a serial peripheral interface (SPI).

Diagnostic outputs from the ARG82801-1 include a power-on-reset output (NPOR) and a fault flag output (FFn) to alert the microprocessor that a fault has occurred. The microprocessor can read fault status through SPI. Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the ARG82801-1.

The ARG82801-1 contains two types of watchdog functions: Q&A and Window Watchdog timer. The watchdog timer is activated once it receives a valid SPI command from a processor. The watchdog can be put into flash mode or be reset via secure SPI commands.

The ARG82801-1 is supplied in a low-profile (1.2 mm maximum height) 38-lead eTSSOP package (suffix “LV”) with exposed power pad.



ARG82801-1 Simplified Block Diagram

SELECTION GUIDE

Part Number	Package	Packing [1]	Lead Frame
ARG82801KLVATR-1	38-pin eTSSOP with thermal pad	4000 pieces per 7-inch reel	100% matte tin

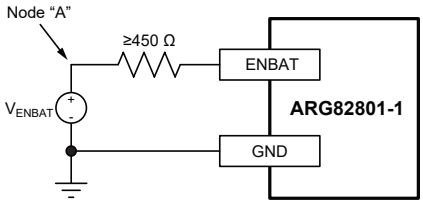
[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBAT}	With current limiting resistor [3]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBAT}		±75	mA
LX	V_{LX}		-0.3 to $V_{VIN} + 0.3$	V
		t < 250 ns	−1.5	V
		t < 50 ns	$V_{VIN} + 3$	V
GU, GV, GW, GVBB	V_{GU}, V_{GV}, V_{GW}, V_{GVBB}		$V_{SX} - 0.3$ to $V_{SX} + 12$	V
SU, SV, SW, SVBB	V_{SU}, V_{SV}, V_{SW}, V_{SVBB}		-6 to $V_{VIN} + 5$	V
		Transient	-18 to $V_{VIN} + 5$	V
VCP1	V_{VCP1}		$V_{VIN} - 0.3$ to $V_{VIN} + 8$	V
VCP2	V_{VCP2}		$V_{VIN} - 0.3$ to $V_{VIN} + 12$	V
CP1C1	V_{CP1C1}	$V_{VIN} \geq 12V$	$V_{VIN} - 12$ to $V_{VIN} + 0.3$	V
		$V_{VIN} < 12V$	-0.3 to $V_{VIN} + 0.3$	V
CP2C1	V_{CP2C1}		$V_{VIN} - 0.3$ to $V_{VCP1} + 0.3$	V
CP1C2	V_{CP1C2}		$V_{VIN} - 0.3$ to $V_{VCP1} + 0.3$	V
CP2C2	V_{CP2C2}		$V_{CP1C2} - 0.3$ to $V_{VCP2} + 0.3$	V
V5P1, V5P2	V_{V5P1}, V_{V5P2}	Independent of V_{VIN}	−1.0 to 40	V
All other pins			−0.3 to 7	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] The higher ENBAT ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	eTSSOP-38 (LV) package	30	°C/W

[4] Additional thermal information available on the Allegro website.

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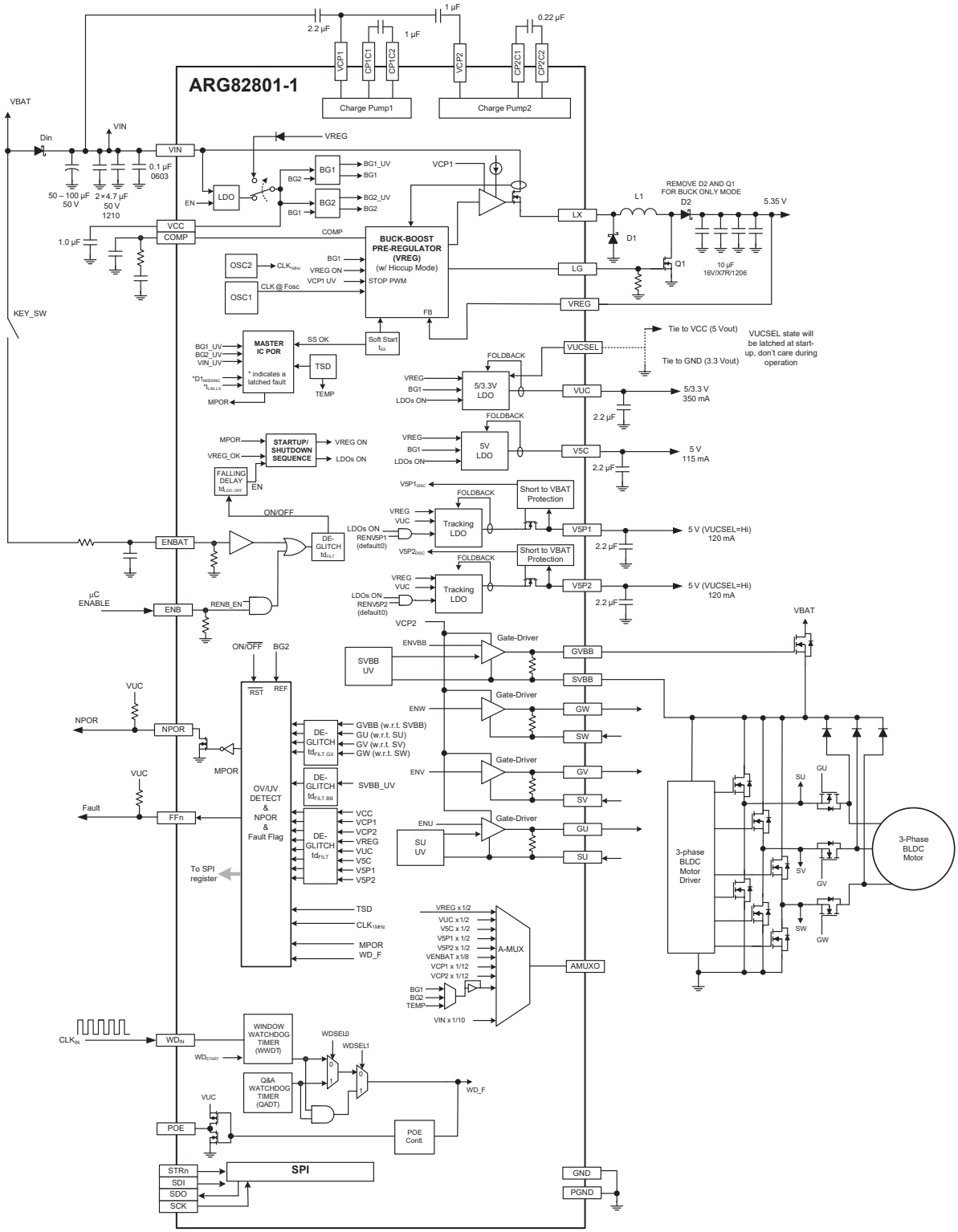
FUNCTIONAL BLOCK DIAGRAM



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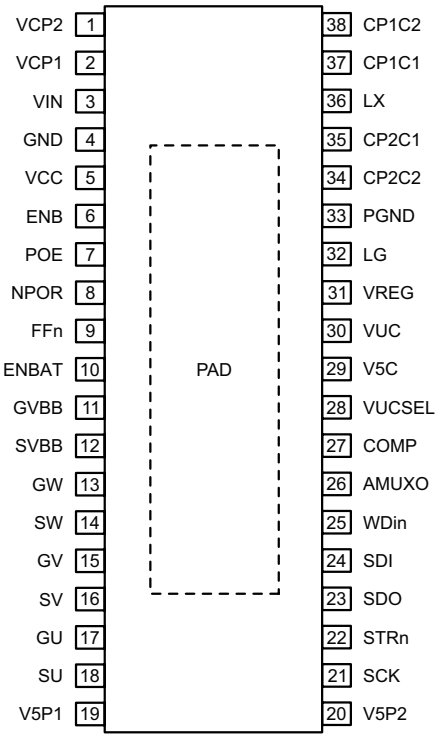

Package LV, 38-Pin eTSSOP
Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCP2	Charge pump 2 reservoir capacitor connection
2	VCP1	Charge pump 1 reservoir capacitor connection
3	VIN	Input voltage pin
4	GND	Ground
5	VCC	Internal voltage regulator bypass capacitor pin
6	ENB	Logic enable input from a microcontroller or DSP
7	POE	Gate drive enable signal, goes low if a watchdog fault is detected
8	NPOR	Active low, open-drain regulator fault detection output
9	FFn	Fault Flag to microcontroller
10	ENBAT	Ignition enable input from the key/switch via a series resistor
11	GVBB	Battery line MOSFET gate drive
12	SVBB	Battery line MOSFET source reference
13	GW	W phase MOSFET gate drive
14	SW	W phase MOSFET source reference
15	GV	V phase MOSFET gate drive
16	SV	V phase MOSFET source reference
17	GU	U phase MOSFET gate drive
18	SU	U phase MOSFET source reference
19	V5P1	5 V protected regulator output which tracks VUC
20	V5P2	5 V protected regulator output which tracks VUC
21	SCK	SPI clock input from the microcontroller
22	STRn	SPI chip select input from the microcontroller
23	SDO	SPI data output to the microcontroller
24	SDI	SPI data input from the microcontroller
25	WDin	Watchdog refresh input from a microcontroller or DSP
26	AMUXO	Analog Multiplexer output
27	COMP	Error amplifier compensation network pin for the buck/boost pre-regulator
28	VUCSEL	VUC output voltage selection pin: 1 (High: should be tied to VCC), V_{VUC} = 5 V 0 (Low: tied to GND), V_{VUC} = 3.3 V
29	V5C	5 V regulator output
30	VUC	Selectable V_{OUT} (5 V or 3.3 V by VUCSEL) regulator output
31	VREG	Voltage feedback input of the pre-regulator and supply input of the linear regulators
32	LG	Boost gate drive output for the buck/boost pre-regulator
33	PGND	Power ground
34	CP2C2	Charge pump 2 capacitor connection
35	CP2C1	Charge pump 2 capacitor connection
36	LX	Switching node for the buck/boost pre-regulator
37	CP1C1	Charge pump 1 capacitor connection
38	CP1C2	Charge pump 1 capacitor connection
–	PAD	Exposed thermal pad

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ELECTRICAL CHARACTERISTICS [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage [2]	V_{VIN}	After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck-Boost Mode	3.8	13.5	36	V
		After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck Mode	5.5	13.5	36	V
VIN UVLO Start Voltage	$V_{VIN(START)}$	V_{VIN} rising	4.55	4.8	5.05	V
VIN UVLO Stop Voltage	$V_{VIN(STOP)}$	V_{VIN} falling	3.25	3.5	3.75	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	1.3	–	V
VIN Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{VREG} = 5.6 V (no PWM)	–	13	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{ENBAT} = Low and V_{ENB} = Low, T_J = 25°C	–	–	13	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	Dithering off	2.0	2.2	2.4	MHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±10	–	%
VIN Dithering Start Threshold [2]	$V_{VIN(DITHER,ON)}$	V_{VIN} rising	8.5	9.0	9.5	V
		V_{VIN} falling	–	17	–	V
VIN Dithering Stop Threshold [2]	$V_{VIN(DITHER,OFF)}$	V_{VIN} falling	7.8	8.3	8.8	V
		V_{VIN} rising	–	18	–	V
CHARGE PUMP (VCP1 AND VCP2)						
VCP1 Output Voltage	V_{VCP1}	V_{VCP1} – V_{VIN}, V_{VIN} ≥ 9 V, I_{VCP1} > –5 mA, Buck Mode	4.1	6.6	–	V
		V_{VCP1} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP1} > –5 mA, Buck Mode	3.6	4.4	–	V
		V_{VCP1} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{REG} = 5.35 V, I_{VCP1} > –5 mA, Buck-Boost Mode	3.0	3.8	–	V
VCP2 Output Voltage	V_{VCP2}	V_{VCP2} – V_{VIN}, V_{VIN} > 9 V, I_{VCP2} > –1 mA, Buck Mode	9	10	–	V
		V_{VCP2} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP2} > –1 mA, Buck Mode	8	10	–	V
		V_{VCP2} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{VREG} = 5.35 V, I_{VCP2} > –1 mA, Buck-Boost Mode	6.6	9.5	–	V
Switching Frequency	$f_{SW(CP)}$		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.4	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Pre-Regulator Output Voltage [2]	V_{VREG}	V_{VIN} = 13.5 V, 0.1 A < I_{VREG} < 1.2 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM(OFFS)}$	V_{COMP} for 0% duty cycle	–	480	–	mV
LX Rising Slew Rate [2]	SR_{LXRISE}	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	–	1.4	–	V/ns
LX Falling Slew Rate [2]	SR_{LXFALL}	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time	$t_{ON(BUCK,MIN)}$		–	85	160	ns
Buck Maximum Duty Cycle	$D_{BUCK(MAX)}$	V_{VIN} < 7.8 V	–	–	100	%
Boost Maximum Duty Cycle	$D_{BST(MAX)}$	After V_{VIN} > $V_{VIN(START)}$, and VREG in regulating, V_{VIN} = 3.8 V	–	65	–	%
COMP to LX Current Gain	gm_{POWER}		–	4.57	–	A/V
Slope Compensation [2]	S_E		1.1	1.62	2.15	A/µs
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	–	60	90	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.1 A	–	95	115	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	160	190	mΩ
MOSFET Leakage Current	$I_{FET(LKG)}$	V_{ENBAT} ≤ 2.2 V, V_{ENB} = Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [3]	–	–	10	µA
		V_{ENBAT} ≤ 2.2 V, V_{ENB} ≤ Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{VOL}		–	60	–	dB
Transconductance	gm_{EA}	V_{SS} (internal signal) = 750 mV	520	720	920	µA/V
		V_{SS} (internal signal) = 500 mV	260	360	460	µA/V
Output Current	$I_{O(EA)}$		–	±75	–	µA
Maximum Output Voltage	$V_{O(EA,MAX)}$	V_{VIN} < 8.5 V	1.2	1.52	2.1	V
		V_{VIN} > 9.5 V	0.9	1.22	1.7	V
Minimum Output Voltage	$V_{O(EA,MIN)}$		–	–	300	mV
COMP Pull-Down Resistance	R_{COMP}	HICCUP = 1 or FAULT = 1 or V_{ENBAT} = Low and V_{ENB} = Low	–	1	–	kΩ

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.35	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{VIN} =13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS Ramp Time [2]	t_{SS}		–	900	–	µs
SS PWM Frequency Foldback	$f_{SW(SS)}$	0 V ≤ V_{VREG} < 0.67 V typical	–	f_{OSC}/8	–	–
		0.67 V ≤ V_{VREG} < 1.34 V typical	–	f_{OSC}/4	–	–
		1.34 V ≤ V_{VREG} < 2.68 V typical	–	f_{OSC}/2	–	–
		V_{VREG} ≥ 2.68 V typical	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup Enable Delay Time [2]	$t_{HIC(EN)}$		–	230	–	µs
Hiccup Recovery Time [2]	$t_{HIC(REC)}$		–	930	–	µs
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	32	–	PWM cycles
		V_{VREG} > 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$	V_{VIN} < 8.5 V	3.83	4.2	4.77	A
		V_{VIN} > 9.5 V	2.49	2.8	3.11	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$	Latched fault after 2nd detection	5.3	7.1	–	A

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.9	−1.4	−1.0	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns
VUC, V5C, V5P1, V5P2 LINEAR REGULATORS						
VUC Accuracy and Load Regulation (5 V_{OUT})	V_{VUC5}	10 mA < I_{VUC} < 350 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
VUC Accuracy and Load Regulation (3.3 V_{OUT}) [2]	V_{VUC33}	10 mA < I_{VUC} < 350 mA, V_{VREG} = 5.25 V, VUCSEL = 0	3.23	3.30	3.37	V
VUC Output Capacitance Range [2]	$C_{OUT(VUC)}$		1.0	–	15	µF
V5C Accuracy and Load Regulation	V_{V5C}	5 mA < I_{V5C} < 115 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5C Output Capacitance Range [2]	$C_{OUT(V5C)}$		1.0	–	15	µF
V5P1 Accuracy and Load Regulation (5 V_{OUT})	V_{V5P1}	5 mA < I_{V5P1} < 120 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
V5P1 Output Capacitance Range [2]	$C_{OUT(V5P1)}$		1.0	–	15	µF
V5P2 Accuracy and Load Regulation (5 V_{OUT})	V_{V5P2}	5 mA < I_{V5P2} < 120 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
V5P2 Output Capacitance Range [2]	$C_{OUT(V5P2)}$		1.0	–	15	µF
V5Px/VUC Tracking Ratio	$TRACK_{V5Px/VUC}$	V_{VUC} = 3.3 V, V_{V5Px} / V_{3V3}, VUCSEL = 0	1.500	1.515	1.530	V/V
V5Px Tracking Accuracy, V_{VUC} = 3.3 V	$TRACK_{33}$	I_{V5Px} = I_{VUC} = 60 mA, VUCSEL = 0	–0.66	–	0.66	%
V5Px Tracking Accuracy, V_{VUC} = 5 V	$V_{TRACK(5V)}$	I_{V5Px} = I_{VUC} = 60 mA, VUCSEL = 1	–25	–	25	mV
VUC OVERCURRENT PROTECTION						
VUC Current Limit [1]	$I_{VUC(LIM)}$		–360	–570	–800	mA
VUC Foldback Current [1]	$I_{VUC(FBK)}$	V_{VUC} = 0 V	–60	–170	–250	mA
V5C OVERCURRENT PROTECTION						
V5C Current Limit [1]	$I_{V5C(LIM)}$		–120	–180	–250	mA
V5C Foldback Current [1]	$I_{V5C(FBK)}$	V_{V5C} = 0 V	–15	–60	–125	mA
V5P1 OVERCURRENT PROTECTION						
V5P1 Current Limit [1]	$I_{V5P1(LIM)}$		–135	–230	–350	mA
V5P1 Foldback Current [1]	$I_{V5P1(FBK)}$	V_{V5P1} = 0 V	–20	–60	–125	mA
V5P2 OVERCURRENT PROTECTION						
V5P2 Current Limit [1]	$I_{V5P2(LIM)}$		–135	–230	–350	mA
V5P2 Foldback Current [1]	$I_{V5P2(FBK)}$	V_{V5P2} = 0 V	–20	–60	–125	mA

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5C, V5P1, AND V5P2 STARTUP TIMING						
VUC Startup Time (5 V_{OUT}) [2]	$t_{VUC5(START)}$	C_{VUC} ≤ 2.9 µF, Load = 33 Ω ±5% (152 mA), VUCSEL = 1	–	–	1.0	ms
VUC Startup Time (3.3 V_{OUT}) [2]	$t_{VUC33(START)}$	C_{VUC} ≤ 2.9 µF, Load = 33 Ω ±5% (100 mA), VUCSEL = 0	–	–	1.0	ms
V5C Startup Time [2]	$t_{V5C(START)}$	C_{V5C} ≤ 2.9 µF, Load = 100 Ω ±5% (50 mA)	–	–	1.0	ms
V5P1 Startup Time [2]	$t_{V5P1(START)}$	C_{V5P1} ≤ 2.9 µF, Load = 100 Ω ±5%	–	–	1.0	ms
V5P2 Startup Time [2]	$t_{VP2(START)}$	C_{V5P2} ≤ 2.9 µF, Load = 100 Ω ±5%	–	–	1.0	ms
IGNITION ENABLE (ENBAT) INPUT						
ENBAT Thresholds	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.9	3.1	3.5	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT(BIAS)}$	V_{ENBAT} = 0.8 V via a 1 kΩ series resistor	–	–	5	µA
		V_{ENBAT} = 5.5 V via a 1 kΩ series resistor	–	50	100	µA
		V_{ENBAT} = 20 V via a 1 kΩ series resistor	–	–	2	mA
ENBAT Pulldown Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	600	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBAT FILTER/DEGLITCH						
Enable Filter/Deglitch Time	$t_{d(EN)}$		10	15	20	µs
VUC, V5C, V5P1, AND V5P2 UNDERVOLTAGE PROTECTION THRESHOLDS						
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Undervoltage Thresholds	$V_{V5(UV,H)}$	V_{V5} rising, VUCSEL = 1	–	4.68	–	V
	$V_{V5(UV,L)}$	V_{V5} falling, VUCSEL = 1	4.50	4.65	4.80	V
VUC (3.3 V_{OUT}) Undervoltage Thresholds	$V_{V33(UV,H)}$	V_{V33} rising, VUCSEL = 0	–	3.12	–	V
	$V_{V33(UV,L)}$	V_{V33} falling, VUCSEL = 0	2.8	3.1	3.19	V
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Undervoltage Hysteresis	$V_{V5(UV,HYS)}$	$V_{V5(UV,H)} – V_{V5(UV,L)}$	–	30	–	mV
VUC (3.3 V_{OUT}) Undervoltage Hysteresis	$V_{V33(UV,HYS)}$	$V_{V33(UV,H)} – V_{V33(UV,L)}$	–	20	–	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5C, V5P1, AND V5P2 OVERVOLTAGE PROTECTION THRESHOLDS						
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Overvoltage Thresholds	$V_{V5(OV,H)}$	V_{V5} rising, VUCSEL = 1	5.15	5.33	5.5	V
	$V_{V5(OV,L)}$	V_{V5} falling, VUCSEL = 1	–	5.30	–	V
VUC (3.3 V_{OUT}) Overvoltage Thresholds	$V_{V33(OV,H)}$	V_{V33} rising, VUCSEL = 0	3.41	3.51	3.62	V
	$V_{V33(OV,L)}$	V_{V33} falling, VUCSEL = 0	–	3.49	–	V
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Overvoltage Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	–	30	–	mV
VUC (3.3 V_{OUT}) Overvoltage Hysteresis	$V_{V33(OV,HYS)}$	$V_{V33(OV,H)} – V_{V33(OV,L)}$	–	20	–	mV
V5Px Output Disconnect Threshold	$V_{V5PX(DISC)}$	V_{V5PX} rising	–	7.2	–	V
VREG, VCPX, AND BG THRESHOLDS						
VREG Non-Latching Overvoltage Threshold	$V_{VREG(OV,H)}$	V_{VREG} rising, LX PWM disabled	5.70	5.95	6.20	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX PWM enabled	–	5.85	–	V
VREG Non-Latching Overvoltage Hysteresis	$V_{VREG(OV,HYS)}$	$V_{VREG(OV,H)} – V_{VREG(OV,L)}$	–	100	–	mV
VREG Undervoltage Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of VUC linear regulator	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.28	–	V
VREG Undervoltage Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP1 Overvoltage Thresholds [2]	$V_{VCP1(OV,H)}$	V_{VCP1} rising (w.r.t. V_{VIN})	11.0	12.5	14.0	V
VCP1 Undervoltage Thresholds	$V_{VCP1(UV,H)}$	V_{VCP1} rising, PWM enabled (w.r.t. V_{VIN})	2.9	3.1	3.35	V
	$V_{VCP1(UV,L)}$	V_{VCP1} falling, PWM disabled (w.r.t. V_{VIN})	–	2.8	–	V
VCP1 Undervoltage Hysteresis	$V_{VCP1(UV,HYS)}$	$V_{VCP1(UV,H)} – V_{VCP1(UV,L)}$	–	400	–	mV
VCP2 Undervoltage Thresholds	$V_{VCP2(UV,H)}$	V_{VCP2} rising, PWM enabled (w.r.t. V_{VIN})	5.95	6.3	6.65	V
	$V_{VCP2(UV,L)}$	V_{VCP2} falling, PWM disabled (w.r.t. V_{VIN})	–	5.1	–	V
VCP2 Undervoltage Hysteresis	$V_{VCP2(UV,HYS)}$	$V_{VCP2(UV,H)} – V_{VCP2(UV,L)}$	–	1.2	–	V
BG1 and BG2 Undervoltage Thresholds [2]	$V_{BGx(UV)}$	V_{BG1} or V_{BG2} falling	1.00	1.05	1.10	V
OVERVOLTAGE FILTERING/DEGLITCH TIME						
Overvoltage Detection Delay [2]	$t_{d(OV)}$	Overvoltage detection delay time	5	–	25	µs
UNDERVOLTAGE FILTERING/DEGLITCH TIME						
Undervoltage Filter/Deglitch Times [2]	$t_{d(UV)}$	Undervoltage detection delay time	5	–	25	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-on Delay	$t_{d(NPOR,ON)}$	Time from when VUC and V5C are all in regulation to NPOR being asserted high	15	20	25	ms
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	V_{VIN} ≥ 2.5 V, I_{NPOR} = 2 mA	–	150	400	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
FAULT FLAG OUTPUT VOLTAGES (FFn)						
FFn Output Voltage	$V_{FF(L)}$	FFn is tripped, V_{VIN} ≥ 2.5 V, I_{FF} = 2 mA	–	150	400	mV
FFn Leakage Current	$I_{FF(LKG)}$	V_{FF} = 3.3 V	–	–	2	µA
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$V_{WDIN(LO)}$	V_{WDIN} falling	0.8	–	–	V
	$V_{WDIN(HI)}$	V_{WDIN} rising	–	–	2.0	V
WD_{IN} Pull-Down Resistance [2]	R_{WDIN}		–	50	–	kΩ
WD_{IN} TIMING SPECIFICATIONS						
WD_{IN} Duty Cycle [2]	D_{WDIN}		–	50	–	%
Watchdog Activation Delay	$t_{d(WD)}$		–	30	–	ms
GATE DRIVE ENABLE (POE)						
POE Output Voltage	$V_{POE(L)}$	I_{POE} = 4 mA	–	150	400	mV
	$V_{POE(H)}$	I_{POE} = –1.5 mA	0.8 × V_{VUC}	–	–	V
VUCSEL LOGIC INPUT						
VUCSEL Thresholds	$V_{VUCSEL(H)}$	V_{VUCSEL} rising	–	–	2.0	V
	$V_{VUCSEL(L)}$	V_{VUCSEL} falling	0.8	–	–	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (STRn, SDI, SDO, SCK)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{VIN} < 5 V	–	50	–	kΩ
Input Pull-Up To VCC	I_{PU}	STRn	–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	0.8 × V_{VUC}	–	–	V
Clock High Time	t_{SCKH}	A in Figure 1	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 1	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 1	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 1	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 1	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 1	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 1	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 1	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	J in Figure 1	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	K in Figure 1	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	L in Figure 1	10	–	–	ns
Wake Up From Sleep	t_{EN}		–	–	2	ms

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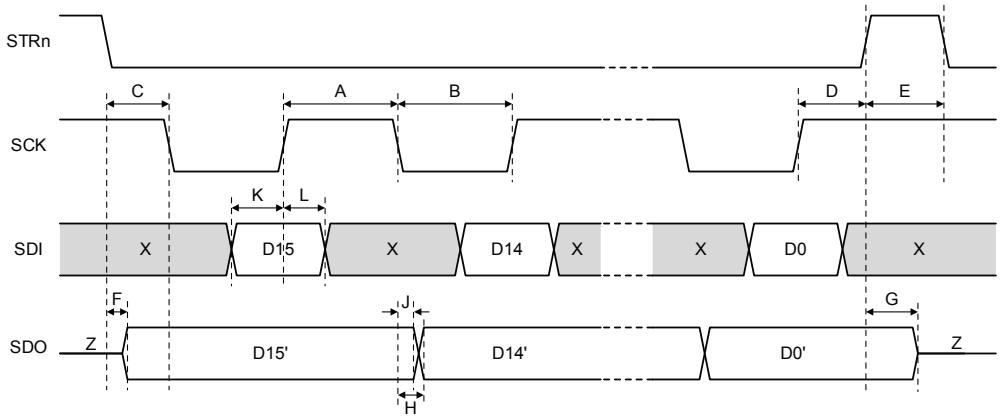

Figure 1: Serial Interface Timing
X = do not exceed Watchdog Config timeout; Z = high-impedance (tri-state)

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Gate Output Drive						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	5	–	µs
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	0.5	–	µs
Turn-On Pulse Current	I_{GXP}		8.5	10	12	mA
Turn-On Pulse Time	t_{GXP}		22	–	42	µs
On Hold Current	I_{GXH}		–	400	–	µA
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{Gx} = 10 mA	–	5	–	Ω
		T_J = 150°C, I_{Gx} = 10 mA	–	10	–	Ω
Gx Output High Voltage	V_{GH}	V_{VIN} > 5.5 V (w.r.t. Sx, or VIN if V_{Sx} > V_{VIN})	8	9	12	V
		5.0 V < V_{VIN} ≤ 5.5 V (w.r.t. Sx, or VIN if V_{Sx} > V_{VIN}), Buck-boost mode	7.2	9	–	V
		V_{VIN} = 4.5 V, V_{SX} = 5.5 V (w.r.t. Sx), Buck-boost mode	6.2	6.9	–	V
Gate Drive Static Load Resistance [2]	R_{GS}	Between Gx and Sx (using ±1% tolerance resistor)	100	–	–	kΩ
Gx Output Voltage Low	V_{GL}	–10 µA < I_{Gx} < 10 µA	–	–	V_{Sx} + 0.3	V
Gx Passive Pull-Down	R_{GPD}	V_{Gx} – V_{Sx} < 0.3 V	–	950	–	kΩ
SVBB Undervoltage Threshold Falling	$V_{SVBB(UV,L)}$	V_{SVBB} falling (w.r.t. GND)	–	–	3	V
SVBB Undervoltage Filter/Deglitch Times	$t_{d(UV,FILT,BB)}$	Undervoltage detection delay time, slow; GD_UV_FLT = 0	–	0.8	1.0	ms
		Undervoltage detection delay time, fast; GD_UV_FLT = 1	3.7	–	18	µs
SU Undervoltage Threshold Falling	$V_{SUUV(L)}$	V_{SU} falling (w.r.t. GND); GD_U_SEL = 1	–	–	3	V
SU Undervoltage Filter/Deglitch Times	$t_{d(UV,FILT,SU)}$	Undervoltage detection delay time, slow; GD_UV_FLT = 0, GD_U_SEL = 1	–	0.8	1.0	ms
		Undervoltage detection delay time, fast; GD_UV_FLT = 1	3.7	–	18	µs
GSx Undervoltage Threshold Rising [2]	$V_{GSx(UV,H)}$	V_{Gx} rising (w.r.t. Sx, x = VBB, U, V, W)	6.0	–	7.0	V
GSx Undervoltage Threshold Hysteresis [2]	$V_{GSx(UV,HYS)}$	x = VBB, U, V, W	–	250	–	mV
GSx Undervoltage Filter/Deglitch Time	$t_{d(UV,FILT,GSx)}$	Undervoltage detection delay time, x = VBB, U, V, W	–	1.4	–	ms

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
ENVBB Enable/Disable Delay Time	$t_{d(EN,BB)}$	From “SPI command is written” to GVBB 20% (enable), to GVBB 80% (disable); GD_EN_DLY = 0	–	1.5	–	ms
ENU Enable/Disable Delay Time	$t_{d(EN,U)}$	From “SPI command is written” to GU 20% (enable), to GU 80% (disable); GD_U_SEL = 1; GD_EN_DLY = 0	–	1.5	–	ms
		From “SPI command is written” to GU 20% (enable), to GU 80% (disable); GD_U_SEL = 0; GD_EN_DLY = 0	–	10	–	ms
ENV and ENW Enable/Disable Delay Time	$t_{d(EN,X)}$	From “SPI command is written” to Gx 20% (enable), to Gx 80% (disable); GD_EN_DLY = 0	–	10	–	ms
ENVBB, ENU, ENV, and ENW Enable Delay Time, Fast	$t_{d(EN,X)}$	From “SPI command is written” to Gx 20%; GD_EN_DLY = 1	–	–	3	µs
ENVBB, ENU, ENV, and ENW Disable Delay Time, Fast	$t_{d(EN,X)}$	From “SPI command is written” to Gx 80%; GD_EN_DLY = 1	–	–	2.25	µs

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Table 1: Startup and Shutdown Logic (signal names consistent with Block Diagram)

ARG82801-1 MODE	Regulator/Isolator Control Bits (0 = OFF, 1 = ON, R = Ready)					ARG82801-1 Status Signals						
	VREG ON	VUC ON	V5C ON	V5P1 and V5P2 ON	Isolator Drivers	EN	MPOR	VREG UV	VUC UV	V5C UV	V5P1 and V5P2 UV	NPOR
RESET	0	0	0	0	0	0	1	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1	1	1	1	0
STARTUP	1	0	0	0	0	1	0	1	1	1	1	0
↓	1	1	0	0	R	1	0	0	1	1	1	0
↓	1	1	1	0	R	1	0	0	0	1	1	1
↓	1	1	1	R	R	1	0	0	0	0	1	1
RUN	1	1	1	R	R	1	0	0	0	0	0	1
15 µs DEGLITCH	1	1	1	R	R	0	0	0	0	0	0	0
SHUTTING DOWN	1	1	0	0	R	0	0	0	0	0	0	0
↓	1	0	0	0	0	0	0	0	0	1	1	0
↓	0	0	0	0	0	0	0	0	1	1	1	0
OFF	0	0	0	0	0	0	0	1	1	1	1	0

TIME

X = DON'T CARE
EN = ENBAT + ENB
MPOR = VCC_UV + VCPx_UV + BG1_UV + BG2_UV + TSD + $D1_{MISSING}$ (latched) + $I_{LIM(LX)}$ (latched)

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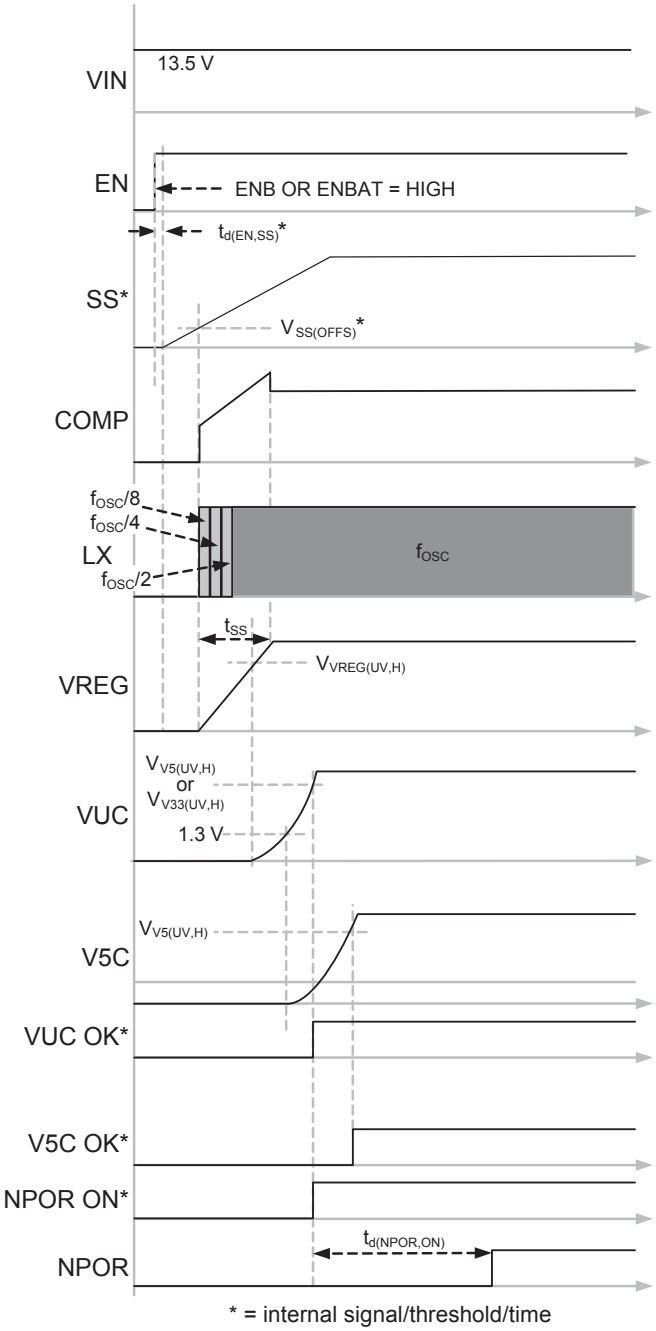

Figure 2: Startup Timing Diagram

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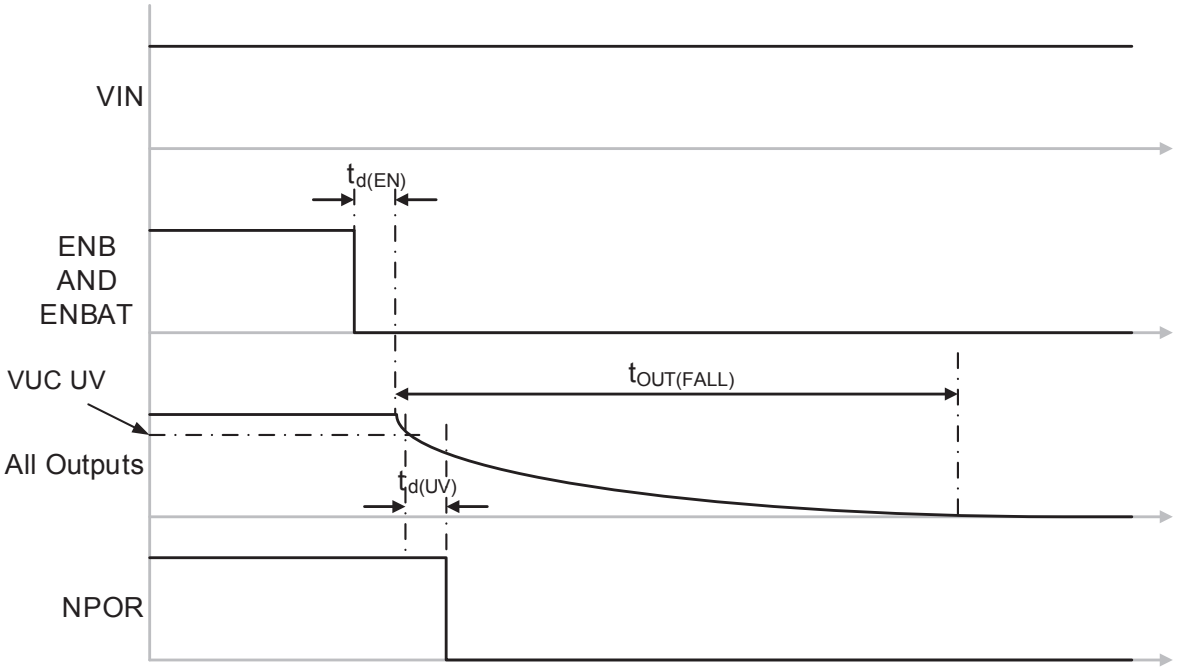

All outputs start to decay $t_{d(EN)}$ seconds after ENB and ENBAT are low.
Time for outputs to drop to zero, $t_{OUT(FALL)}$, various for each output and depends on load current and capacitance.
NPOR falls when VUC reaches its UV point.

Figure 3: Shutdown Timing Diagram

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TIMING DIAGRAMS (not to scale)
* = internal signal/threshold, + is for “or”

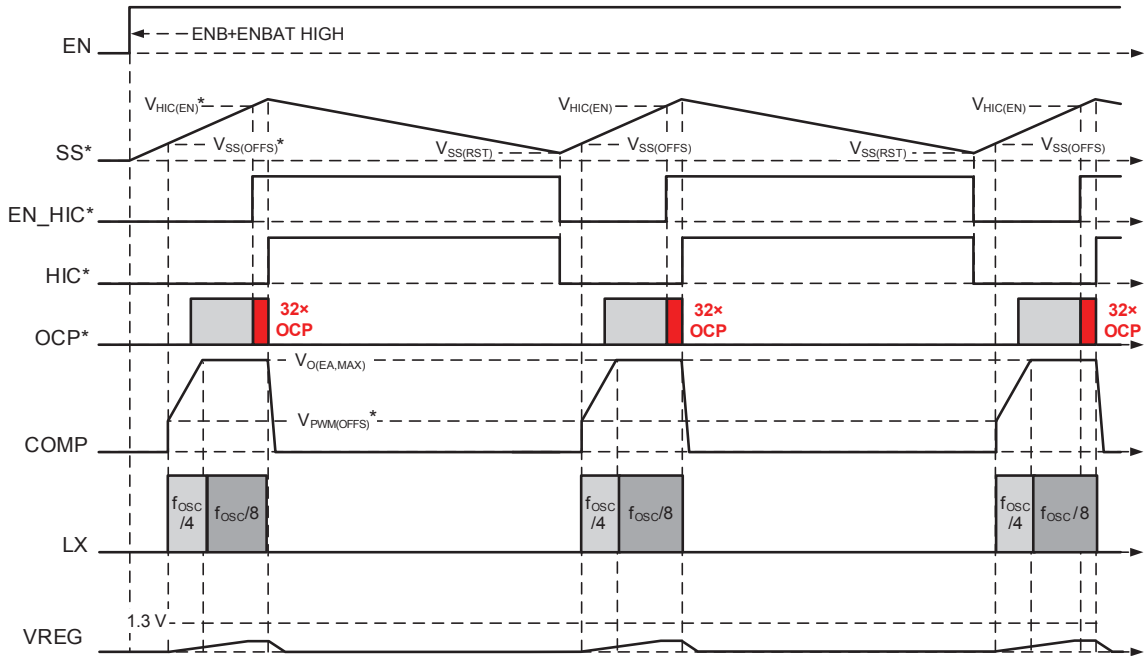

Figure 4: Hiccup Mode Operation with VREG Shorted to GND (R_{LOAD} < 50 mΩ)

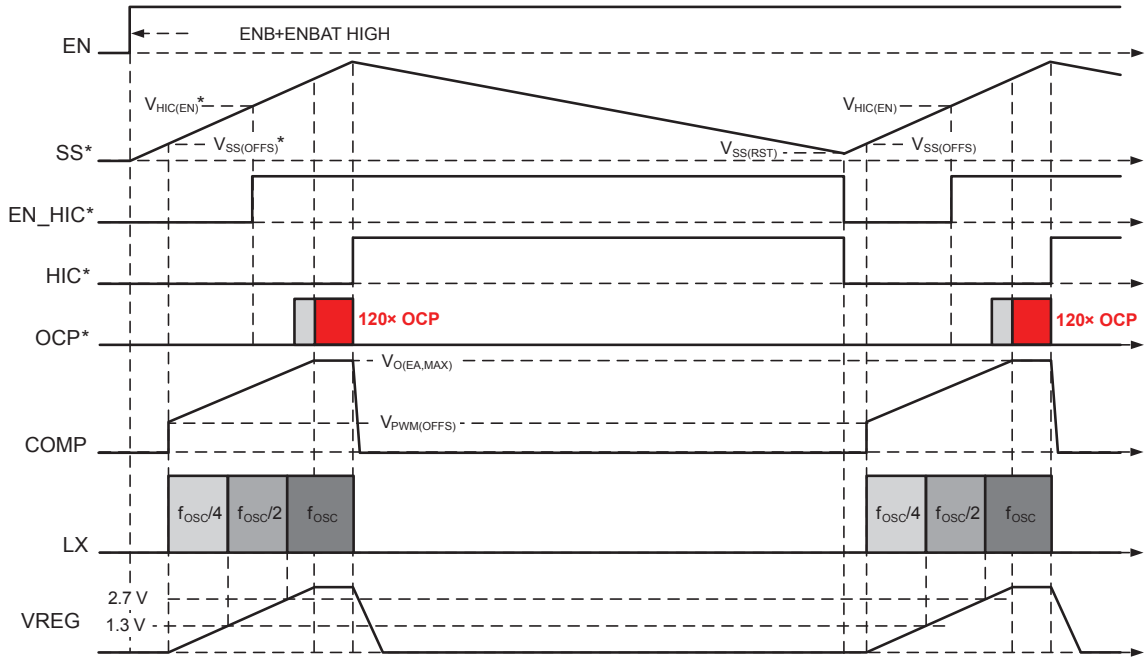

Figure 5: Hiccup Mode Operation with VREG Overloaded (R_{LOAD} ≈ 0.5 Ω)

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Table 2: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	ARG82801-1 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP1	VCP2	VREG	VUC	V5C	V5P1	V5P2	Isolator Drivers	NPOR	FFn	POE	SPI	WD	RESET METHOD
VREG asynchronous diode (D1) missing	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short-circuited or LX shorted to ground	Results in an MPOR after the high-side MOSFET current exceeds $I_{LIM(LX)}$ so all regulators are shut off	Yes	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short then cycle EN or VIN
VCP1 OV	If OV condition persists for more than $t_{d(OV)}$, then set FFn Low	No	No effect	> $V_{VCP1(OV,H)}$	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	On	On	Check for short circuits on VCP1
VIN UVLO	ARG82801-1 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Increase VIN
BG1 UVLO	ARG82801-1 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Replace ARG82801-1
BG2 UVLO	ARG82801-1 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Replace ARG82801-1
VCC UVLO	ARG82801-1 is in reset state	No	UVLO	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCC short limit	ARG82801-1 is in reset state	No	UVLO	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCP1 UVLO	ARG82801-1 is in reset state	No	ON	UVLO	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCP2 UVLO	Terminate isolator portion	No	ON	No effect	UVLO	No effect	No effect	No effect	No effect	No effect	Off	No effect	Low	Low	No effect	No effect	Remove the short circuit
VREG overvoltage $V_{VREG(OV,H)} < V_{VREG}$	Stop PWM switching of LX	No	No effect	No effect	No effect	> $V_{VREG(OV,H)}$	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on VREG
VREG pin open circuit	VREG will decay to 0 V, LX will switch at maximum duty cycle so the voltage on the output capacitors will be very close to VBAT	No	No effect	No effect	No effect	Decay to 0 V	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Connect the VREG pin
VREG shorted to ground V_{VREG} < 1.95 V, $V_{COMP} \neq V_{O(EA,MAX)}$	Continue to PWM but turn off LX when the high side MOSFET current exceeds $I_{LIM(LX)}$	No	No effect	No effect	No effect	Shorted	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Remove the short circuit
VREG overcurrent V_{VREG} < 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 30 OCP faults	No	No effect	No effect	No effect	Over-current	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Decrease the load
VREG overcurrent V_{VREG} > 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 120 OCP faults	No	No effect	No effect	No effect	Over-current	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Low if VUC < $V_{VXX(UV,L)}$	No effect	No effect	Decrease the load
VUC undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	No	No effect	No effect	No effect	No effect	V_{VUC} < $V_{VXX(UV,L)}$	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Off	Low	Low	Low	No effect	No effect	Decrease the load
VUC overvoltage	If OV condition persists for more than $t_{d(OV)}$ then set NPOR Low	No	No effect	No effect	No effect	No effect	V_{VUC} > $V_{VXX(OV,H)}$	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Off	Low	Low	Low	No effect	No effect	Check for short circuits
VUC overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	Falling	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	No effect	No effect	Decrease the load
V5P1 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	V_{V5P1} < $V_{V5(UV,L)}$	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P1 overvoltage or shorted to VBAT	If OV condition persists for more than td (OV) then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5P1

Continued on next page...

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Table 2: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	ARG82801-1 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP1	VCP2	VREG	VUC	V5C	V5P1	V5P2	Isolator Drivers	NPOR	FFn	POE	SPI	WD	RESET METHOD
V5P1 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P2 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	$V_{V5P2} < V_{V5(UV,L)}$	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P2 overvoltage or shorted to VBAT	If OV condition persists for more than $t_{d(OV)}$ then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5P2
V5P2 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5C overvoltage	If OV condition persists for more than $t_{d(OV)}$ then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	$V_{V5C} > V_{V5(OV,H)}$	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5C
V5C undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	$V_{V5C} < V_{V5(UV,L)}$	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5C overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
Thermal shutdown	Results in an MPOR, so all regulators are shut off	No	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	No effect	No effect	Let the ARG82801-1 cool
Window WD error	Put the system into a safe state	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	Off	Off	No effect	Low	Low	No effect	–	Get proper signal from microcontroller
Q&A watchdog error	Put the system into a safe state	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	Off	Off	No effect	Low	Low	No effect	–	Get proper signal from microcontroller
BIST error	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	Low	Low	No effect	No effect	Write 1 to reset
SVBB_UV	Corresponding (GVBB) Isolator off	Yes	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	GVBB: off GU, GV, GW: No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on SVBB, Toggle ENVBB
SU_UV (see 0x09 [D7])	Corresponding (GU) Isolator off	Yes	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	GU: off GVBB, GV, GW: No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on SU, Toggle ENU and Write 1 to reset
GSx_UV	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on Gx
LG operation failure	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on LG
VDD_UV	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	May lose contents	May have effect	Restart the device
DBE Fault	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Restart the device
SE Fault	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check SPI signal

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FUNCTIONAL DESCRIPTION

Overview

The ARG82801-1 is a power management IC designed for safety-critical applications. It contains one switching and four linear regulators to create the voltages necessary for typical automotive applications such as electrical power steering.

The ARG82801-1 pre-regulator can be configured as a buck converter or buck boost. Buck boost is suitable for when applications must work with extremely low battery voltages. This pre-regulator generates a fixed 5.35 V to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

Pre-Regulator

The pre-regulator incorporates an internal high-side buck switch and a boost switch gate driver. An external freewheeling diode and LC filter are required to complete the buck converter. By adding a MOSFET and boost diode, the pre-regulator can now maintain all outputs with input voltages down to 3.8 V.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage detection and reporting
3. Shorted switch node to ground
4. Open freewheeling diode protection
5. High voltage rating for load dump

Bias Supply

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the ARG82801-1. These features include:

1. Input voltage undervoltage lockout
2. Output undervoltage detection and reporting
3. Overcurrent and short-circuit limit
4. Dual input, VIN and VREG, for low battery voltage operation

Charge Pump

Charge pump circuits provide the voltage necessary to drive high-side N-channel MOSFETs in the pre-regulator, linear regulators, and floating gate drivers. Four external capacitors are required for charge pump operation. During the first cycle of the charge pump action, the flying capacitor between pins CP1C1 and CP1C2 is charged either from VIN or VREG, whichever is highest. During the second cycle, the voltage on the flying capacitor charges the VCP1 capacitor and the flying capacitor, between pins CP2C1 and CP2C2. During the next cycle, the voltage on the flying capacitor charges the VCP2 capacitor. The charge pump incorporates some safety features:

1. Undervoltage and overvoltage detection and reporting
2. Overcurrent safe mode protection

Bandgap

Dual bandgaps are implemented within the ARG82801-1. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCPx, VREG, and the four post-regulators. The second is dedicated to the monitoring function of all the regulators undervoltage and overvoltage. This improves safety coverage and fault reporting from the ARG82801-1.

Should the regulation bandgap fail, then the outputs will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the outputs will remain in regulation, but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two other bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable

Two Enable pins are available on the ARG82801-1. A high signal on either of these pins enables the regulated outputs of the ARG82801-1. One Enable (ENB) is logic-level compatible. The second enable (ENBAT), is battery-level rated and can be connected to the ignition switch.

Linear Regulators

The ARG82801-1 has four linear regulators: one 5 V regulator, one 5 V or 3.3 V selectable regulator, and two protected regulators which track VUC (5 V or 3.3 V).

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

The protected regulators (V5P1 and V5P2) include protection against connection to the battery voltage. This makes these outputs suitable for powering remote sensors or circuitry where short to battery is possible.

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The pre-regulator powers these linear regulators which reduces power dissipation and temperature.

	VUCSEL	$V_{OUT(TYP)}$	Startup	Tracking
VUC	1	5 V	When $V_{VREG} > V_{VREG(UV,H)}$	n/a
	0	3.3 V		
V5C	Don't Care	5 V	When $V_{VUC} > V_{V5} / V_{V33(UV,H)}$	n/a
V5Px	Don't Care	5 V	Enabled via SPI	VUC (DC level) During start-up it does not track VUC since default SPI bit is "disabled"

Fault Detection and Reporting

There is extensive fault detection within the ARG82801-1; most have been discussed previously. There are two fault reporting mechanisms used by the ARG82801-1: one through hardwired pins and the other through a serial communications interface (SPI).

Two hardwired pins on the ARG82801-1 are used for fault reporting. The first pin, NPOR, reports on the status of the VUC output. This signal goes low if this output is out of regulation. The second pin, FFn (active low fault flag), reports on all other faults. FFn goes low if a fault within the ARG82801-1 exists. The FFn pin can be used by the processor as an alert to check the status of the ARG82801-1 via SPI and see where the fault occurred.

Startup Self-Test

The ARG82801-1 includes self-test which is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detection circuits for the main outputs.

In the event the self-test fails, the ARG82801-1 will report the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detectors are verified during startup of the ARG82801-1. A voltage that is higher than the undervoltage threshold is applied to each UV comparator; this should cause the relative undervoltage fault bit in the diagnostic registers to change state. If the diagnostic UV register bits change state, the corresponding verify register bits will latch high. When the test of all UV detectors is complete, the verify register bits will remain high if the test passed. If any UV bits in the verify registers, after test, are not set high, then the verification has failed. The following UV detectors are tested: VREG, VUC, V5C, V5P1, and V5P2.

Overvoltage Detect Self-Test

The overvoltage (OV) detectors are verified during startup of the ARG82801-1. A voltage is applied to each OV comparator that is higher than the overvoltage threshold; this should cause the relative overvoltage fault bit in the diagnostic registers to change state. If the diagnostic OV register bits change state, the corresponding verify register bits will latch high. When the test of all OV detectors is complete, the verify register bits will remain high if the test passed. If any OV bits in the verify registers after test are not set high, then the verification has failed. The following OV detectors are tested: VREG, VUC, V5C, V5P1, and V5P2.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified on startup of the ARG82801-1. A voltage is applied to the comparator that is lower than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit, TSD, to be latched in the Verify Result register 0. When the test is complete, the general fault flag will be cleared and the overtemperature fault will remain in the Verify Result register 0 until reset. If the TSD bit is not set, then the verification has failed.

Power-On Enable Self-Test

The ARG82801-1 also incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin with the internal demanded status. If they differ for any reason, an FFn is set and the POE_OK in SPI diagnostic register goes low.

Watchdog Timer

The ARG82801-1 has two watchdog functions: window watchdog timer and Q&A watchdog timer. When the regulators (VUC and V5C) have been above their undervoltage thresholds for watchdog activation delay ($t_{d(WD)}$), WD is activated, WD state will be in the configuration state ("Config"), and the user can set the configuration within 220 ms (min, $t_{WDTO(CONFIG)}$). If no configuration input until $t_{WDTO(CONFIG)}$ is expired, WD moves into "RESET". Moving back to "Config" mode requires secure SPI command (0x0B).

WINDOW WATCHDOG

The ARG82801-1 window watchdog circuit monitors an external clock applied to the WDIN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within a SPI-programmed "window" or a watchdog fault will be generated. A watchdog fault will set POE "low".

After startup, if no clock edges are detected at WDIN for watchdog activation delay $t_{d(WD)}$ + max timeout (written in 0x09), the ARG82801-1 will generate watchdog fault and reset its counters. This process will repeat until the system recovers and clock edges are applied to WDIN.

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Q&A WATCHDOG

The Q&A watchdog circuit monitors an answer code from the microcontroller. The Q&A watchdog procedure is as follows:

1. Write 0x08 to set open window period and acceptable number of mis-refresh in “Config” mode.
2. Write 0x0B for watchdog restart. Then ARG82801-1 enters into “Normal” mode and generates 6-bit random code.
3. Microcontroller reads 0x0A to get 6-bit random code via SDO.
4. Write 0x0A with 6-bit inverted random code within open window period. In case the ARG82801-1 can’t get the right inverted code, then the watchdog timer is refreshed and generates new 6-bit random code. ARG82801-1 can accept mis-refresh.
5. Repeat #2 to #4 within the programmed window.

Analog Multiplexer Output

The AMUXO terminal is an analog multiplexer output to monitor the voltage of the nodes detailed in Table 3. The output is selected through the serial interface (0x0C). The driving capability of this output is 1 mA and maximum voltage is 3.8 V. Reference response time from SPI register write to AMUX output change is ~20 µs.

Table 3: Analog Multiplexer Output

Node	Signal Divide Ratio	Tolerance (reference)
VREG	1/2	±6%
VUC	1/2	±6%
V5C	1/2	±6%
V5P1	1/2	±6%
V5P2	1/2	±6%
VENBAT	1/8	±6%
VCP1	1/12	±6%
VCP2	1/12	±6%
BG1	1/1	±6%
BG2	1/1	±6%
VIN	1/10	±6%
TEMP	–	Output (mV) = 1440 mV – 3.92 mV/°C × T_J (°C)

Floating MOSFET Gate Drivers

The ARG82801-1 has four independent floating gate drive outputs to drive external, low on-resistance, power N-channel MOSFETs connected as a 3-phase solid state relay in phase-isolation applications and an input battery line isolator.

A charge pump regulator provides the above-battery supply voltage necessary to maintain the power MOSFETs in the on state continuously when the phase voltage is equal to the battery voltage.

An internal resistor, R_{GPD}, between the Gx and Sx pins plus an integrated hold-off circuit, will ensure that the gate-source voltage of the MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate-source resistors on the isolation MOSFETs. In any case, if gate-source resistors are mandatory for the application, then the pump regulator can provide sufficient current to maintain the MOSFET in the on state with a gate-source resistor as low as 100 kΩ.

The four gate drives can be controlled independently through the serial interface by setting the appropriate bit in the control register.

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GVBB, GU, GV, and GW. Gx=1 (or “high”) means that the upper half of the driver is turned on and current will be sourced to the gate of the MOSFET in the phase isolation circuit, turning it on. Gx=0 (or “low”) means that the lower half of the driver is turned on and will sink current from the external MOSFET’s gate to the respective Sx terminal, turning it off.

The reference points for the floating drives are the load phase connections, SVBB, SU, SV, and SW. The discharge current from the floating MOSFET gate capacitance flows through these connections.

In some applications, it may be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary in situations where the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off.

The recirculation path can be provided by connecting a suitably rated power diode to the “motor” side of the isolation MOSFETs and GND. See the Functional Block Diagram for more details.

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Table 4: Floating MOSFET Driver

Name	GD_U_SEL (0x09 [D5])	Purpose	Enable/Disable			Gate to Source UV	Source to GND UV		UV Filter		
			Register Bit	GD_EN_DLY	Delay	State Register bit	Function	State Register bit	GD_UV_FLT	GSx UV Filter	SVBB/SU UV Filter
GVBB / SVBB	X (don't care)	VBAT disconnect	ENVBB (0x07 [D3])	0	1.5 ms	GSVBB_UV (0x02 [D7])	Yes	SVBB_UV (0x02 [D3])	0	1.4 ms	0.8 ms
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	11 µs
GU / SU	0	Phase disconnect	ENU (0x07 [D2])	0	10 ms	GSU_UV (0x02 [D6])	No (Disabled)	SU_UV (0x02 [D2]) Always=0	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–
	1	VBAT disconnect		0	1.5 ms		Yes	SU_UV (0x02 [D2])	0	1.4 ms	0.8 ms
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	11 µs
GV / SV	X	Phase disconnect	ENV (0x07 [D1])	0	10 ms	GSV_UV (0x02 [D5])	No	–	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–
GW / SW	X	Phase disconnect	ENW (0x07 [D0])	0	10 ms	GSW_UV (0x02 [D4])	No	–	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–

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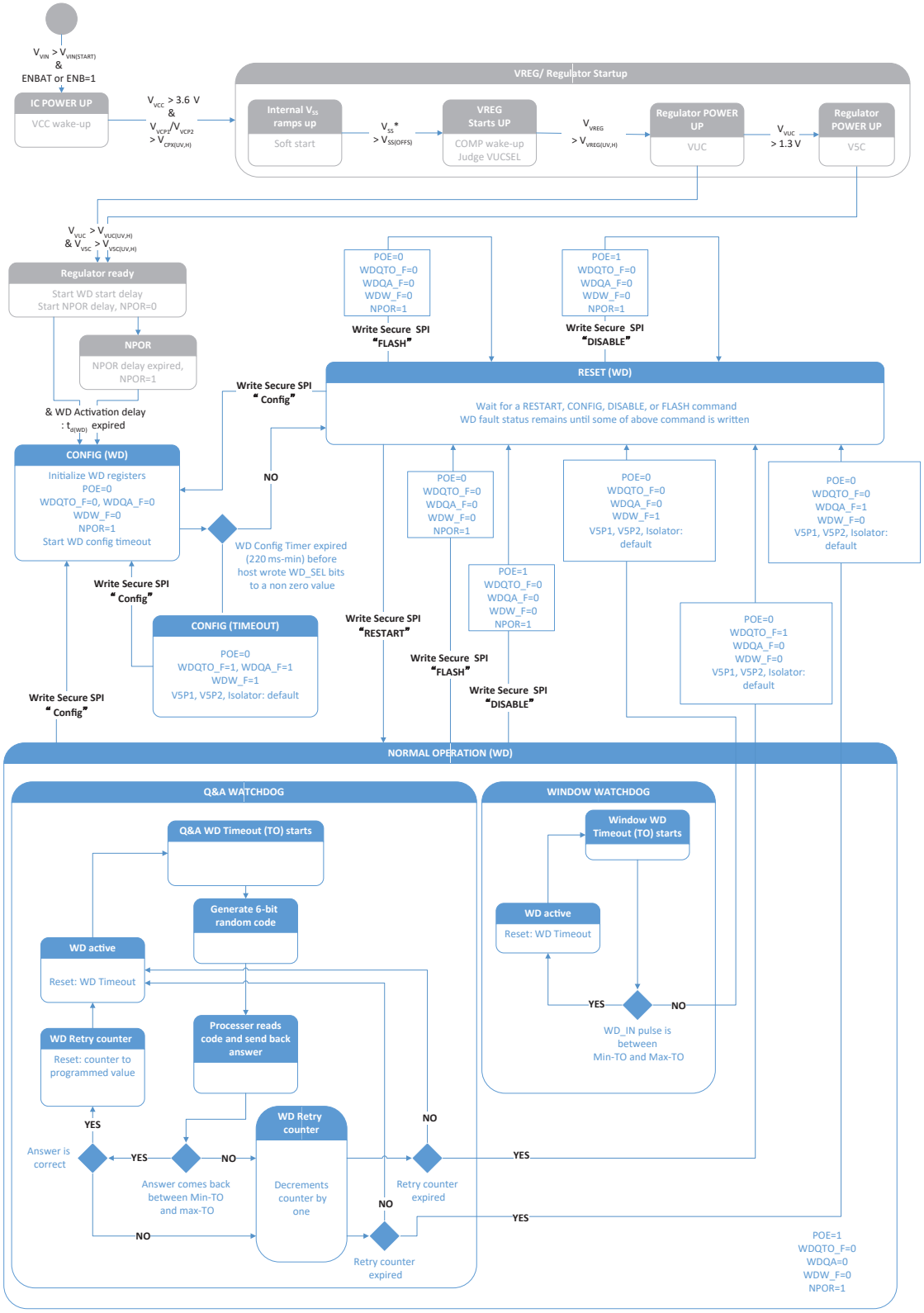

Figure 6: Watchdog State Diagram

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SERIAL COMMUNICATION INTERFACE

The ARG82801-1 provides the user with a three-wire synchronous serial interface that is compatible with SPI (Serial Peripheral Interface). A fourth wire can be used to provide diagnostic feedback and readback of the register content.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing diagram (Figure 1). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple SDI slave units to use common SDI, SCK, and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Diagnostic register is reset.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic register will not be reset, and the SE (serial error) bit will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers is output on the SDO terminal MSB first while STRn is low, and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF (fault flag) bit from the Diagnostic register, is output as soon as STRn goes low.

Each of the programmable (configuration and control) registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0, then the remaining data bits (bits 9 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to 1, then the Diagnostic register is output. If WR is set to 0, then the contents of the register selected by the first five bits is output. In all cases, the first bit output on SDO will always be the FF bit from the Diagnostic Register.

The ARG82801-1 has 15 register banks. Bit <15:11> represents the register address for read and write. Bit <10> detects the read and write operation. For write operation, Bit <10> = 1, and for read operation, bit value is logic low. Bit <9> is an unused bit. Maximum data size is eight bits, so Bit <8:1> represents the data word. The last bit in the serial transfer, Bit <0> is parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transmission should always be an odd number. This ensures that there is always at

Pattern at SDI Pin

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A4	A3	A2	A1	A0	W/R	NU	D7	D6	D5	D4	D3	D2	D1	D0	P
5-Bit Address							8-Bit Data								

Pattern at SDO Pin after SDI Write

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBE	FF	SE	ENBATS	WDW_F	WDQTO_F	WDQA_F	VREG_OK	VCC_OK	VCP_OK	VUC_OK	V5C_OK	0	0	0	P
Diagnostics															

Pattern at SDO Pin after SDI Read

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBE	FF	SE	ENBATS	WDW_F	WDQTO_F	WDQA_F	D7	D6	D5	D4	D3	D2	D1	D0	P
Diagnostics							8-Bit Data								

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least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

Register data is output on the SDO terminal MSB first while STRn is low and changes to the next bit on each falling edge of the SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

If there are more than 16 rising edges on SCL or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset the SE bit will be set to indicate a data transfer error.

SDI: Serial data logic input with pull down. 16-bit serial word input MSB first.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCL. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

SDO: Serial data output. High impedance when STRn is high. Output bit 15 of the status register, the fault flag (FF) as soon as STRn goes low.

Register Mapping

STATUS REGISTERS

The ARG82801-1 provides three status registers. These registers are read only. They provide real-time status of various functions within the ARG82801-1.

These registers report on the status of all four system rails. They also report on internal rail status, including the charge pump, VREG, and VCC rails. The general fault flag and watchdog fault state are found in these status registers.

The logic that creates the power-on enable and power reset status are reported through these registers.

CONFIGURATION REGISTERS

The ARG82801-1 allows configuration of the watchdog validation parameters and disabling dithering function.

The watchdog can only be configured during “Config” state. This occurs when the ARG82801-1 is initially enabled or the watchdog is restarted through SPI.

The ARG82801-1 uses frequency dithering for pre-regulator to help reduce EMC noise. The user can disable this feature through the SPI. Default is enabled.

All WD Configuration must be entered before modifying the WD_SEL bits, meaning Config_1 must be written before Config_0.

DIAGNOSTIC REGISTERS

There are multiple diagnostic registers in the ARG82801-1. These registers can be read to evaluate the status of the ARG82801-1. The high-level registers will indicate which area a fault has occurred. Logic high on a data bit in this register implies that no fault has occurred. The following are monitored by these registers:

- All four outputs
- ARG82801-1 bias voltage
- Charge pump voltage
- Pre-regulator voltage
- Overtemperature
- Watchdog output
- Shorts on LX pin or open diode on pre-regulator

Note some of these faults will cause the ARG82801-1 to shut down, which might shutdown the microprocessor monitoring the SPI. In this event, the only way to read the fault would be to have alternative power to the microprocessor so it can read the registers. If V_{CC} of the ARG82801-1 shuts down, all stored register information is lost and the registers revert back to default values.

Other diagnostic registers store more details on each fault, this includes:

- Overvoltage on a particular output or internal rail
- Undervoltage on a particular output or internal rail

The diagnostic registers are latch registers and will hold data if a fault has occurred but recovered. These registers are reset by writing a 1 to them.

OUTPUT ENABLE/DISABLE REGISTER

The output enable/disable register provides the user control of the LDO outputs and isolator drivers. For LDO control, two bits must be set high to enable an output. If only one bit is high, then the 5 V outputs remain off.

WATCHDOG MODE KEY REGISTER

At times, it may be necessary to re-flash or restart the processor. To do this, the user must put the watchdog into “Flash Mode” or “restart”. This is done by writing a sequence of key words to the “watchdog_mode_key” register. If the correct word sequence is

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not received, then the sequence must restart.

Once flash is complete, the processor must send the restart sequence of keywords for the watchdog to exit “Flash Mode”. If V_{CC} has not been removed from the ARG82801-1, the watchdog will restart with the current configuration.

VERIFY RESULT REGISTERS

On every startup, the ARG82801-1 performs a self-test of the UV and OV detect circuits. This test should cause the diagnostic registers to toggle state. If the diagnostic register successfully changes state, the verify result register will latch high. Upon completion of startup, the system’s microprocessor can check the verify result registers to see if the self-test passed.

Table 5: Register Map

HEX Address	Register Name	DEC Address	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	status_0	0	RO	FF	POE_OK	SE	NPOR_S	NPOR_OK	WDW_F	WDQTO_F	WDQA_F
0x01	status_1	1	RO		VCC_OK	VCP_OK	VREG_OK	VUC_OK	V5C_OK	V5P1_OK	V5P2_OK
0x02	status_2	2	RO	GSVBB_UV	GSU_UV	GSV_UV	GSW_UV			POE_S	ENBAT_S
			RW1C					SVBB_UV	SU_UV		
0x03	status_3	3	RO	CLK_ST_H	CLK_ST_L	ENB_S	DBE	TSD_OK	LG_OK	LX_OK	D1_OK
0x04	diag_0	4	RW1C			VDD_UV	VCC_UV	VCP_OV	VCP_UV	V5P2_OV	V5P2_UV
0x05	diag_1	5	RW1C	VREG_OV	VREG_UV	VUC_OV	VUC_UV	V5C_OV	V5C_UV	V5P1_OV	V5P1_UV
0x06	output_enable / disable_0	6	RW				V5P1_EN1	V5P2_EN1		V5P1_EN0	V5P2_EN0
0x07	output_enable / disable_1	7	RW					ENVBB	ENU	ENV	ENW
0x08	config_0	8	RW	WD_SEL_1	WD_SEL_0	TRY_1	TRY_0	TIMER_3	TIMER_2	TIMER_1	TIMER_0
0x09	config_1	9	RW	GD_UV_FLT	GD_EN_DLY	GD_U_SEL	FFn_SEL	WIN_Timer_2	WIN_Timer_1	WIN_Timer_0	DITH_DIS
0x0A	Q&A Watchdog	10	RW			RND_5	RND_4	RND_3	RND_2	RND_1	RND_0
0x0B	Watchdog_Secure_key	11	WO	Keycode entry (White only)							
0x0C	AMUXOUT	12	RW					SEL_MUX_3	SEL_MUX_2	SEL_MUX_1	SEL_MUX_0
0x0D	Verify_result_0	13	RW1C	BIST_FAIL	TSD_FAIL	VREG_OV_FAIL	VREG_UV_FAIL	VUC_OV_FAIL	VUC_UV_FAIL	V5C_OV_FAIL	V5C_UV_FAIL
0x0E	Verify_result_1	14	RW1C					V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL

Register Types:
RO = Read-Only
RW = Read or Write
RW1C = Read or Write 1 to clear
WO = Write-Only

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0x00: STATUS REGISTER 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5-bit Address					Type	NU	8-bit Data								
Status_0	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	RO		FF	POE_OK	SE	NPOR_S	NPOR_OK	WDW_F	WDQTO_F	WDQA_F	P
							0	0	0	0	0	0	0	0	0	

FF	Fault Flag	
0	No Fault	Default
1	Fault	

POE_OK	Power-on enable signal matches what ARG82801-1 is demanding	
0	Fault	Default
1	No Fault	

SE	Serial Error Flag [1]	
0	No Fault	Default
1	Fault	

NPOR_S	Power-On Reset Internal Logic Status	
0	NPOR is Low	Default
1	NPOR is High	

NPOR_OK	NPOR Signal matches what device is demanding	
0	Fault	Default
1	No Fault	

WDW_F	Window Watchdog Fault Flag	
0	No Fault or Window Watchdog is disabled	Default
1	Fault	

WDQTO_F	Q&A Watchdog Timeout Fault Flag	
0	Q&A watchdog off or No fault	Default
1	Q&A watchdog Timeout fault	

WDQA_F	Q&A Watchdog Answer Fault Flag	
0	Q&A watchdog off or No fault	Default
1	Q&A watchdog Answer fault	

[1] SE Fault: If more than sixteen rising edges on SCK are detected while STRn is LOW or if STRn goes HIGH and there are fewer than sixteen rising edges on SCK.

0x01: STATUS REGISTER 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5-bit Address					Type	NU	8-bit Data								
Status_1	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	1	RO			VCC_OK	VCP_OK	VREG_OK	VUC_OK	V5C_OK	V5P1_OK	V5P2_OK	P
							0	0	0	0	0	0	0	0	0	

VCC_OK	VCC Output Rail is OK	
0	Fault (UV)	Default
1	No Fault	

VCP_OK	Charge Pump Output Rail is OK	
0	Fault (VCP1-UV, VCP1-OV or VCP2-UV)	Default
1	No Fault	

VREG_OK	VREG Output Rail is OK	
0	Fault (UV or OV)	Default
1	No Fault	

VUC_OK	VUC Output Rail is OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5C_OK	V5C Output Rail is OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5P1_OK	V5P1 Output Rail is OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5P2_OK	V5P2 Output Rail is OK	
0	Fault (UV or OV)	Default
1	No Fault	

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0x02: STATUS REGISTER 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status_2	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	1	0	RO		GSVBB_UV	GSU_UV	GSV_UV	GSW_UV			POE_S	ENBAT_S	P
						RW1C						SVBB_UV	SU_UV			
							0	0	0	0	0	0	0	0	0	

GSVBB_UV	GVBB - SVBB Undervoltage Status	
0	OK (Undervoltage is NOT detected or ENVBB=0)	Default
1	Undervoltage	

GSU_UV	GU - SU Undervoltage Status	
0	OK (Undervoltage is NOT detected or ENU=0)	Default
1	Undervoltage	

GSV_UV	GV - SV Undervoltage Status	
0	OK (Undervoltage is NOT detected or ENV=0)	Default
1	Undervoltage	

GSW_UV	GW - SW Undervoltage Status	
0	OK (Undervoltage is NOT detected or ENW=0)	Default
1	Undervoltage	

SVBB_UV	SVBB - GND Undervoltage Status	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage	

SU_UV	SU - GND Undervoltage Status	
0	OK (Undervoltage is NOT detected or GD_U_SEL=0)	Default
1	Undervoltage (GD_U_SEL=1)	

POE_S	Power-On Enable Internal Logic Status	
0	POE is Low	Default
1	POE is High	

ENBAT_S	Battery Enable (ENBAT) Status	
0	ENBAT is Low	Default
1	ENBAT is High	

0x03: STATUS REGISTER 3

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status_3	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	1	1	RO		CLK_ST_H	CLK_ST_L	ENB_S	DBE	TSD_OK	LG_OK	LX_OK	D1_OK	P
							0	0	0	0	0	0	0	0	0	

CLK_ST_H	Indicates the internal clock is stuck high	
0	Internal Clock is not stuck high	Default
1	Internal Clock is stuck high	

CLK_ST_L	Indicates the internal clock is stuck low	
0	Internal Clock is not stuck Low	Default
1	Internal Clock is stuck Low	

ENB_S	Logic Enable (ENB) Status	
0	ENB is low	Default
1	ENB is high	

DBE	EEPROM Dual Bit Error Flag [1]	
0	No Fault	Default
1	Fault	

TSD_OK	Thermal Shutdown (Overtemperature) Detection Flag	
0	Overtemperature is detected	Default
1	OK (Overtemperature is NOT detected)	

LG_OK	Pre-Regulator Boost Gate Drive Output (LG) Status	
0	Fault on LG is detected	Default
1	OK (LG is working correctly)	

LX_OK	Pre-Regulator SW-Node (LX) Fault Detection Flag	
0	Fault on LX is detected	Default
1	OK (LX is working correctly)	

D1_OK	Pre-Regulator Asynchronous Diode (D1) Missing Detection Status	
0	Fault (D1 missing is detected)	Default
1	OK (D1 missing is NOT detected)	

[1] DBE Fault: it means that a dual bit error occurred loading the trim data from EEPROM.

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0x04: DIAG REGISTER 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diag_0	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	1	0	0	RW1C				VDD_UV	VCC_UV	VCP_OV	VCP_UV	V5P2_OV	V5P2_UV	P
							0	0	0	0	0	0	0	0	0	

VDD_UV	VDD Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

VCC_UV	VCC Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

VCP_OV	VCP Output Overvoltage Detection	
0	OK (VCP1 Overvoltage is NOT detected)	Default
1	VCP1 Overvoltage is detected	

VCP_UV	VCP Output Undervoltage Detection	
0	OK (VCP1 and VCP2 Undervoltage is NOT detected)	Default
1	VCP1 or VCP2 Undervoltage is detected	

V5P2_OV	V5P2 Output Overvoltage Detection	
0	OK (Overvoltage is NOT detected)	Default
1	Overvoltage is detected	

VR5P2_UV	V5P2 Rail Over Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

0x05: DIAG REGISTER 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diag_1	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	1	0	1	RW1C		VREG_OV	VREG_UV	VUC_OV	VUC_UV	V5C_OV	V5C_UV	V5P1_OV	V5P1_UV	P
							0	0	0	0	0	0	0	0	0	

VREG_OV	VREG Output Overvoltage Detection	
0	OK (Overvoltage is NOT detected)	Default
1	Overvoltage is detected	

VREG_UV	VREG Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

VUC_OV	VUC Output Overvoltage Detection	
0	OK (Overvoltage is NOT detected)	Default
1	Overvoltage is detected	

VUC_UV	VUC Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

V5C_OV	V5C Output Overvoltage Detection	
0	OK (Overvoltage is NOT detected)	Default
1	Overvoltage is detected	

V5C_UV	V5C Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

V5P1_OV	V5P1 Output Overvoltage Detection	
0	OK (Overvoltage is NOT detected)	Default
1	Overvoltage is detected	

V5P1_UV	V5P1 Output Undervoltage Detection	
0	OK (Undervoltage is NOT detected)	Default
1	Undervoltage is detected	

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0x06: OUTPUT ENABLE/DISABLE REGISTER 0

Output Enable/ Disable Register_0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	1	1	0	RW					V5P1_EN1	V5P2_EN1		V5P1_EN0	V5P2_EN0	P
							0	0	0	0	0	0	0	0	0	

V5P1_EN1	V5P1_EN0	Enable V5P1	
0	0	V5P1 is Disabled	Default
0	1	V5P1 is Disabled	
1	0	V5P1 is Disabled	
1	1	V5P1 is Enabled	

V5P2_EN1	V5P2_EN0	Enable V5P2	
0	0	V5P2 is Disabled	Default
0	1	V5P2 is Disabled	
1	0	V5P2 is Disabled	
1	1	V5P2 is Enabled	

0x07: OUTPUT ENABLE/ DISABLE REGISTER 1

Output Enable/ Disable Register_1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	1	1	1	RW						ENVBB	ENU	ENV	ENW	P
							0	0	0	0	0	0	0	0	0	

ENVBB	Enable GVBB-Gate driver	
0	Disabled	Default
1	Enabled	

ENU	Enable GU-Gate driver	
0	Disabled	Default
1	Enabled	

ENV	Enable GV-Gate driver	
0	Disabled	Default
1	Enabled	

ENW	Enable GW-Gate driver	
0	Disabled	Default
1	Enabled	

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0x08: CONFIGURATION REGISTER 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config_0	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	1	0	0	0	RW		WD_SEL_1	WD_SEL_0	TRY_1	TRY_0	TIMER_3	TIMER_2	TIMER_1	TIMER_0	P
							0	0	0	0	0	0	0	0	0	

WD_SEL_1	WD_SEL_0	Watchdog	
0	0	Default (WD waiting for config)	Default
0	1	Window watchdog only	
1	0	Q&A watchdog only	
1	1	Both (Window and Q&A)	

TRY_1	TRY_0	Acceptable Number of Mis-Refresh	
0	0	0	Default
0	1	1 time	
1	0	3 times	
1	1	7 times	

Timer3	Timer2	Timer1	Timer0	Min. Timeout [1]	Max. Timeout [1]	
0	0	0	0	0.5 ms	1 ms	Default
0	0	0	1	1 ms	2 ms	
0	0	1	0	2 ms	4 ms	
0	0	1	1	4 ms	8 ms	
0	1	0	0	8 ms	16 ms	
0	1	0	1	12 ms	24 ms	
0	1	1	0	16 ms	32 ms	
0	1	1	1	24 ms	48 ms	
1	0	0	0	32 ms	64 ms	
1	0	0	1	40 ms	80 ms	
1	0	1	0	64 ms	128 ms	
1	0	1	1	72 ms	144 ms	
1	1	0	0	80 ms	160 ms	
1	1	0	1	96 ms	192 ms	
1	1	1	0	128 ms	256 ms	
1	1	1	1	144 ms	288 ms	

[1] Typical number at the internal clock is center value, need to keep enough margin for ±5% tolerance of the clock.

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0x09: CONFIGURATION REGISTER 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config_1	5-bit Address					Type	NU	8-bit Data								
	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	1	0	0	1	RW		GD_UV_FLT	GD_EN_DLY	GD_U_SEL	FFn_SEL	WIN_Timer_2	WIN_Timer_1	WIN_Timer_0	DITH_DIS	P
							0	0	0	0	0	0	0	0	0	

Bit D7, D6, GD_U_SEL: Select Gate Drive UV filter and enable/disable delay			
GD_UV_FLT	**GD_EN_DLY**	**Undervoltage Detection Delay Time**	**Enable Delay**
0	0	Slow	Slow
1	x	Fast	–
x	1	–	Fast

GD_U_SEL	**Select Gate Drive GU/SU Node Function**			
	ENU Gate Driver Enable/Disable Delay (typ)	**SU-UV**	**Note**	
0	10 ms	Disabled	GU/SU is used for phase isolator	Default
1	1.5 ms	Enabled	GU/SU is used for VBAT disconnect	

FFn_SEL	**Signal on FFn Pin**	
0	Fault-Low	Default
1	50 Hz (Nominal) clock signal output; independent from fault flag	

WIN_Timer_2	**WIN_Timer_1**	**WIN_Timer_0**	**Window Watchdog Error Timeout (Min.) [1]**	**Window Watchdog Error Timeout (Max.) [1]**	
0	0	0	0.5 ms	4 ms	Default
0	0	1	1 ms	8 ms	
0	1	0	2 ms	16 ms	
0	1	1	4 ms	32 ms	
1	0	0	6 ms	42 ms	
1	0	1	8 ms	64 ms	
1	1	0	10 ms	80 ms	
1	1	1	12.5 ms	100 ms	

[1] Typical number at the internal clock is center value, need to keep enough margin for ±5% tolerance of the clock.

DITH_DIS	**Disable Dithering Function**	
0	Dithering is enabled	Default
1	Dithering is disabled	

0x0A: Q&A WATCHDOG REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q&A WD	0	1	0	1	0	RW				RND_5	RND_4	RND_3	RND_2	RND_1	RND_0	P
							0	0	0	0	0	0	0	0	0	

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0x0B: WATCHDOG SECURE KEY REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD Secure Key	0	1	0	1	1	WO		KEY_7	KEY_6	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	P
							0	0	0	0	0	0	0	0	0	

Three 8-bit words must be sent in the correct order to enable flash mode, config mode, Watchdog restart, or disable the watchdog for debugging purpose. If an incorrect word is received, then the register resets and the first word has to be resent.

	Flash Mode	Config Mode	Watchdog Restart	Watchdog Disable
WORD1	0xD3	0xD3	0xD3	0xD3
WORD2	0x33	0x33	0x33	0x33
WORD3	0xCC	0xCD	0xCE	0xCF

0x0C: ANALOG MUX OUTPUT REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMUXOUT	0	1	1	0	0	RW						SEL_MUX_3	SEL_MUX_2	SEL_MUX_1	SEL_MUX_0	P
							0	0	0	0	0	0	0	0	0	

SEL_MUX_3	SEL_MUX_2	SEL_MUX_1	SEL_MUX_0	MUX Output (Signal Divided Ratio)	
0	0	0	0	VREG (1/2)	Default
0	0	0	1	VUC (1/2)	
0	0	1	0	V5C (1/2)	
0	0	1	1	V5P1 (1/2)	
0	1	0	0	V5P2 (1/2)	
0	1	0	1	ENBAT (1/8)	
0	1	1	0	BG1 (1/1)	
0	1	1	1	BG2 (1/1)	
1	0	0	0	TEMP (n/a) Output (mV) = 1440 mV – 3.92 mV/°C × T_J (°C)	
1	0	0	1	VIN (1/10)	
1	0	1	0	VCP1 (1/12)	
1	0	1	1	VCP2 (1/12)	

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0x0D: VERIFY REGISTER 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5-bit Address					Type	NU	8-bit Data								
Verify_0	A4	A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0	
	0	1	1	0	1	RW1C		BIST_FAIL	TSD_FAIL	VREG_OV_FAIL	VREG_UV_FAIL	VUC_OV_FAIL	VUC_UV_FAIL	V5C_OV_FAIL	V5C_UV_FAIL	P
							0	0	0	0	0	0	0	0	0	

BIST_FAIL	Built-In Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

TSD_FAIL	Thermal Shutdown Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

VREG_OV_FAIL	VREG Overvoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

VREG_UV_FAIL	VREG Undervoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

VUC_OV_FAIL	VUC Overvoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

VUC_UV_FAIL	VUC Undervoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

V5C_OV_FAIL	V5C Overvoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

V5C_UV_FAIL	V5C Undervoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

0x0E: VERIFY REGISTER 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Verify_1	0	1	1	1	0	RW1C						V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL	P
							0	0	0	0	0	0	0	0	0	

V5P1_OV_FAIL	V5P1 Overvoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

V5P1_UV_FAIL	V5P1 Undervoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

V5P2_OV_FAIL	V5P2 Overvoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

V5P2_UV_FAIL	V5P2 Undervoltage Self-Test Result Flag	
0	Self-test passed	Default
1	Self-test failed	

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DESIGN AND COMPONENT SELECTION

The following section briefly describes the component selection procedure for the ARG82801-1.

Setting up the Pre-Regulator

This section discusses the component selection for the ARG82801-1 pre-regulator. It covers the charge pump circuit, inductor, diodes, boost MOSFET, and input and output capacitors. It will also cover loop compensation.

Charge Pump Capacitors

The charge pump circuits require two capacitors: VCP1, a 2.2 µF connected from pin VCP1 to VIN and 1 µF connected between pins CP1C1 and CP1C2; and VCP2, a 1 µF connected from pin VCP2 to VCP1 and 0.22 µF connected between pins CP2C1 and CP2C2. These capacitors should be high-quality ceramic capacitors, such as an X5R or X7R, with a voltage rating of at least 16 V.

PWM Switching Frequency

The switching frequency of the ARG82801-1 is fixed at 2.2 MHz nominal. The ARG82801-1 includes a frequency foldback scheme that starts when V_{IN} is greater than 18 V. Between 18 V and 36 V, the switching frequency will foldback from 2.2 MHz typical to 1 MHz typical. The switching frequency for a given input voltage above 18 V and below 36 V is:

$$f_{SW} = 3.4 - \frac{1.2}{18} \times V_{VIN}\ (MHz) \qquad (1)$$

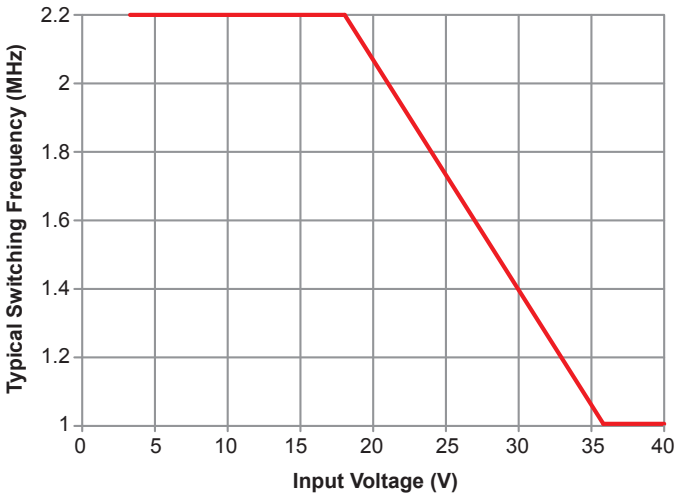

Figure 7: Typical Switching Frequency versus Input Voltage

Pre-Regulator Output Inductor

For peak current-mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate Slope Compensation (S_E). However, the slope compensation in the ARG82801-1 is a fixed value. Therefore, it is important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the ARG82801-1's slope compensation.

Equation 2 can be used to calculate a range of values for the output inductor for the buck-boost. In equation 2, slope compensation can be found in the Electrical Characteristic table, V_F is the asynchronous diode's forward voltage, S_E is in A/µs, and L will be in µH:

$$\frac{(V_{VREG} + V_F)}{S_E} \leq L \leq \frac{2 \times (V_{VREG} + V_F)}{S_E} \qquad (2)$$

If equation 2 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.

Due to topology and frequency switching of the ARG82801-1 pre-regulator, the inductor ripple current varies with input voltage per Figure 8 below:

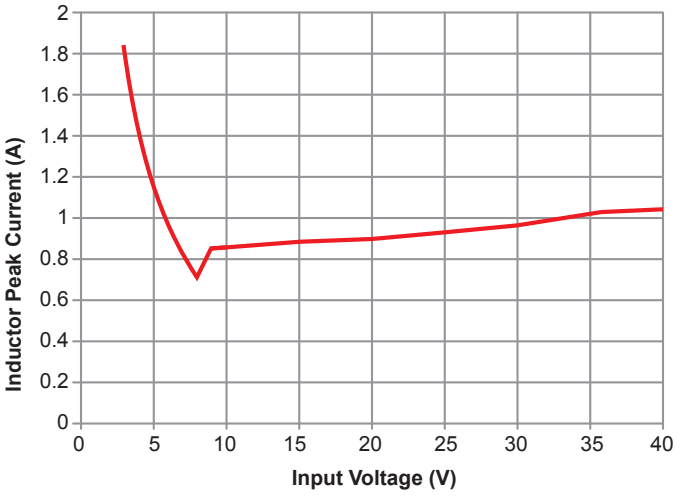

Figure 8: Typical Peak Inductor Current versus Input Voltage for 0.8 A Output Current and 10 µH Inductor

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The inductor should not saturate given the peak operating current during overload. Equation 3 calculates this current. In equation 3, $V_{VIN(MAX)}$ is the maximum continuous input voltage, such as 16 V, and V_F is the asynchronous diode's forward voltage.

$$I_{PEAK} = I_{LIM(ton,min)max} - \frac{S_E \times (V_{VREG} + V_F)}{0.9 \times f_{SW} \times (V_{VIN(MAX)} + V_F)} \quad (3)$$

After an inductor is chosen, it should be tested during output overload and short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Inductor ripple current can be calculated using equation 4 for buck mode, and equation 5 for buck-boost mode.

$$\Delta I_L = \frac{(V_{VIN} - V_{VREG}) \times V_{VREG}}{f_{SW} \times L \times V_{VIN}} \quad (4)$$

$$\Delta I_{L(B/B)} = \frac{V_{VIN} \times D_{BOOST}}{f_{SW} \times L} \quad (5)$$

Pre-Regulator Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage. They also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{VREG}) is a function of the output capacitors parameters: C_O, ESR_{CO}, ESL_{CO}.

$$\Delta V_{VREG} = \Delta I_L \times ESR_{CO} + \frac{V_{VIN} - V_{VREG}}{L} \times ESL_{CO} + \frac{\Delta I_L}{8 \times f_{SW} \times C_O} \quad (6)$$

The type of output capacitors will determine which terms of equation 6 are dominant. For ceramic output capacitors, the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 6.

$$\Delta V_{VREG} = \frac{\Delta I_L}{8 \times f_{SW} \times C_O} \quad (7)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{VREG} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} \times ESL_{CO} \quad (8)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Ceramic Input Capacitors

The ceramic input capacitor(s) must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 8 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG(MAX)} \times 0.25}{0.90 \times f_{SW} \times 50\ mV} \quad (9)$$

where $I_{VREG(MAX)}$ is the maximum current from the pre-regulator,

$$I_{VREG(MAX)} = I_{LINEAR} + I_{AUX} + 20\ mA \quad (10)$$

where I_{LINEAR} is the sum of all the internal linear regulators output currents, I_{AUX} is any extra current drawn from the VREG output to power other devices external to the ARG82801-1.

A good design should consider the DC bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the capacitance value decreases. The X5R and X7R type capacitors

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should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size.

Also for improved noise performance, it is recommended to add smaller sized capacitors close to the input pin and the D1 anode. Use a 0.1 µF 0603 capacitor or less.

Buck-Boost Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the ARG82801-1. Equation 3 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{VIN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

$$I_{AVG} = 0.9 \times I_{VREG(MAX)} \quad (11)$$

where $I_{VREG(MAX)}$ is calculated using equation 10.

Boost MOSFET (Q1)

The RMS current in the boost MOSFET (Q1) occurs when V_{VIN} is at its minimum and both the buck and boost operate at their maximum duty cycles (approximately 64% and 58%, respectively),

$$I_{Q1(RMS)} = \sqrt{D_{BOOST} \times \left[\left(I_{PEAK} - \frac{\Delta I_{L(B/B)}}{2}\right)^2 + \frac{\Delta I_{L(B/B)}^2}{12}\right]} \quad (12)$$

where $\Delta I_{L(B/B)}$ and I_{PEAK} are derived using equations 3 and 5, respectively.

Boost Diode (D2)

In buck mode, this diode will simply conduct the output current. However, in buck-boost mode, the peak currents in this diode may increase a lot. The ARG82801-1 limits the peak current to the value calculated using equation 3. The average current is simply the output current.

Pre-Regulator Compensation Components (R_Z, C_Z, C_P)

Although the ARG82801-1 can operate in buck-boost mode at low input voltages, it still can be considered a buck converter when looking at the control loop. The following equations can be used to calculate the compensation components.

First, select the target crossover frequency for the final system.

While switching at over 2 MHz, the crossover is governed by the required phase margin. Since a type II compensation scheme is used, the system is limited to the amount of phase that can be added. Hence, a crossover frequency, f_C, in the region of 55 kHz is selected. The total system phase will drop off at higher crossover frequencies. The R_Z selection is based on the gain required at the crossover frequency and can be calculated by the following simplified equation:

$$R_Z = \frac{13.36 \times \pi \times f_C \times C_O}{gm_{POWER} \times gm_{EA}} \quad (13)$$

where f_C is in kHz, C_O (actual capacitance at 5.35 V DC bias) is in µF, and R_Z will be in kΩ. The gm_{POWER} (in A/V) and gm_{EA} (in µA/V) can be found in the Electrical Characteristic table.

The series capacitor, C_Z, along with the resistor, R_Z, set the location of the compensation zero. This zero should be placed no lower than ¼ the crossover frequency and should be kept to a minimum value. Equation 14 can be used to estimate this capacitor value.

$$C_Z > \frac{4}{2\pi \times R_Z \times f_C} \quad (14)$$

where f_C is in kHz, R_Z is in kΩ, and C_Z will be in µF.

Determine if the second compensation capacitor (C_P) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency or the following relationship is valid:

$$\frac{1}{2\pi \times C_O \times ESR_{CO}} < \frac{f_{SW}}{2} \quad (15)$$

If this is the case, then add the second compensation capacitor (C_P) to set the pole at the location of the ESR zero. Determine the C_P value by the equation:

$$C_P = \frac{C_{OUT} \times ESR_{CO}}{R_Z} \quad (16)$$

where C_O is in µF, ESR_{CO} is in mΩ, R_Z is in kΩ, and C_Z will be in pF.

An Excel-based design tool is available from Allegro that accepts customer specifications and recommended values for both power and compensation components. The pre-regulator bode plot in Figure 9 was generated with this tool. The bandwidth of this system (f_C) is 56 kHz, the phase margin (PM) is 67 degrees, and the gain margin (GM) is 21 dB.

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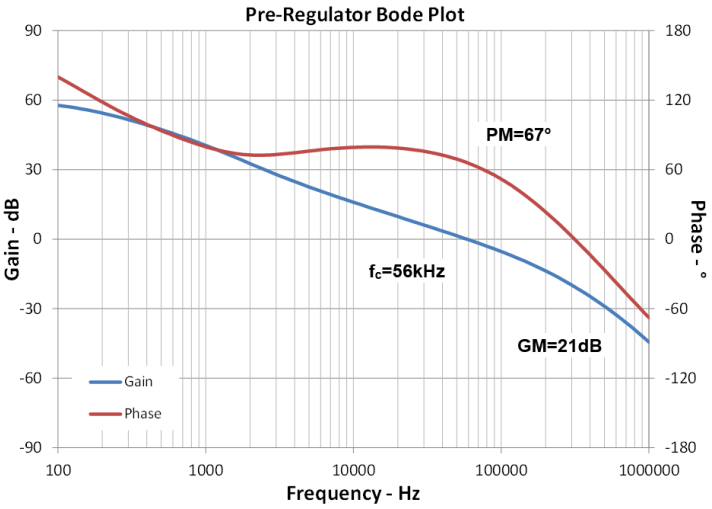

Figure 9: Bode Plot for Pre-Regulator
R_Z = 18.2 kΩ, C_Z = 3.3 nF, C_P = 47 pF
L_O = 4.7 µH, C_O = 3 × 10 µF (16V/X7R/1206) MLCC

Linear Regulators

The four linear regulators only require a single ceramic capacitor located near ARG82801-1 terminals to ensure stable operation. The range of acceptable values is shown in the Electrical Characteristics table. A 2.2 µF capacitor per regulator is recommended.

Also, since the V5P1 and V5P2 are used to power remote circuitry, their load may include external wiring. The inductance of this wiring may cause LC-type ringing and negative spikes on the V5P1 (V5P2) pin if a “fast” short-to-ground occurs. It is recommended a small Schottky diode be placed close to the V5P1 (V5P2) pin to clamp this negative spike. The MSS1P5 (or equivalent) is a good choice.

Internal Bias (VCC)

The internal bias voltage should be decoupled at the VCC pin using a 1 µF ceramic capacitor. It is not recommended to use this pin as a source.

Signal Pins (NPOR, FFn, POE)

The ARG82801-1 has many signal-level pins. The NPOR, FFn, and ENBAT are open-drain outputs and require external pull-up resistors. Allegro recommends sizing the external pull-up resistors so each pin will sink less than 2 mA when it is a logic low. The POE signal is push-pull output and does not require external pull-up resistor.

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PCB LAYOUT RECOMMENDATIONS

The input ceramic capacitors must be located as close as possible to the VIN pins. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger capacitors should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pins.

The pre-regulator asynchronous diode (D1), input ceramic capacitors, and RC snubber must be routed on one layer and "star" grounded at a single location with multiple vias.

The pre-regulator output inductor (L1) should be located close to the LX pins. The LX trace widths (to L1, D1) should be relatively wide and preferably on the same layer as the IC.

The pre-regulators output ceramic capacitors should be located near the VREG pin. There must be 1 or 2 smaller ceramic capacitors as close as possible to the VREG pin.

The four charge pump capacitors must be placed as close as possible to VCP1, CP1C1/CP1C2 and VCP2, CP2C1/ CP2C2.

The ceramic capacitors for the LDOs (VUC, V5C, V5P1, and V5P2) must be placed near their output pins. The V5P1 and V5P2 outputs must have a 1 A/40 V Schottky diode located very close to their pins to limit negative voltages.

The VCC bypass capacitor must be placed very close to the VCC pin.

The COMP network of pre-regulators (R_Z, C_Z, and C_P) must be located very close to the COMP pin.

The thermal pad under the ARG82801-1 must connect to the ground plane(s) with multiple vias.

The boost MOSFET (Q1) and the boost diode (D2) must be placed very close to each other. Q1 should have thermal vias to a polygon on the bottom layer. Also, there should be "local" bypass capacitors from D2 cathode to Q1 source.

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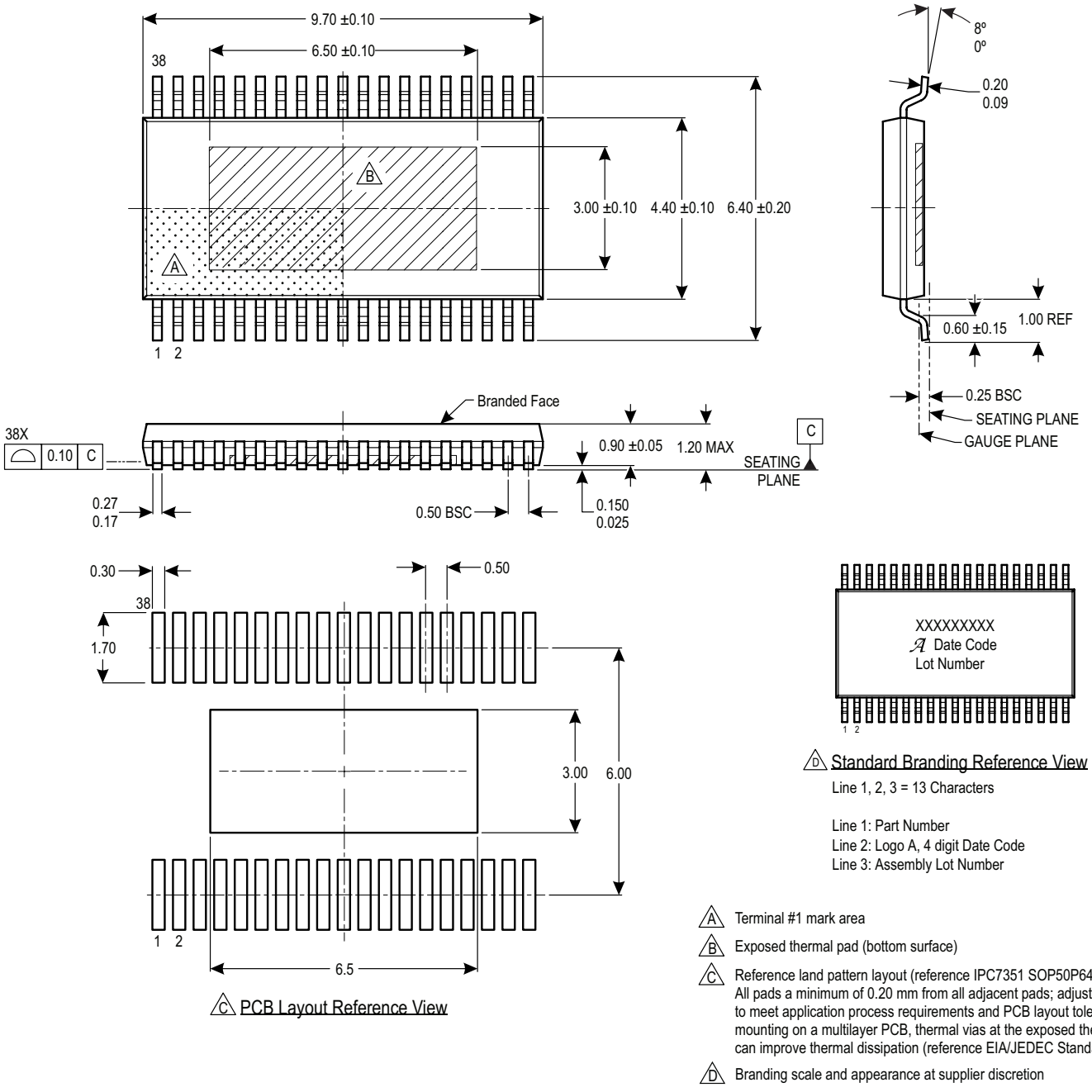
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153 BDT-1)
Dimensions in millimeters
NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

D Standard Branding Reference View

Line 1, 2, 3 = 13 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P640X120-39M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Figure 10: Package LV, 38-Pin eTSSOP

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Revision History

Number	Date	Description
–	December 4, 2018	Initial release
1	December 18, 2019	Minor editorial updates
2	January 6, 2022	Updated package drawing (page 43)

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