74LVC1G58

Low-power configurable multiple function gate

Rev. 11 — 1 February 2022 Product data sheet

1. General description

The 74LVC1G58 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XOR, inverter and buffer; using the 3-bit input. All inputs can be connected diectly to V_{CC} or GND. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power dissipation
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G58GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74LVC1G58GV	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	SOT457
74LVC1G58GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G58GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G58GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G58GW	YK
74LVC1G58GV	V58
74LVC1G58GM	YK
74LVC1G58GN	YK
74LVC1G58GS	YK

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

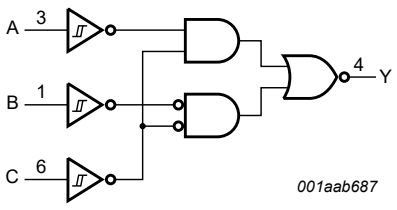


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

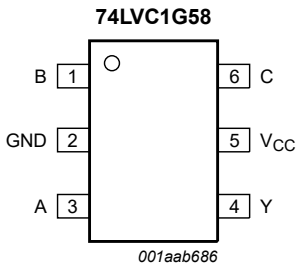
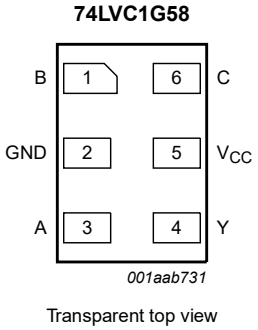
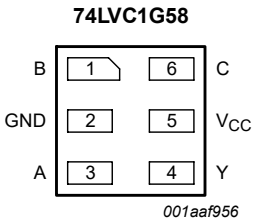


Fig. 2. Pin configuration SOT363-2 (TSSOP6) and SOT457 (SC-74; TSOP6)



Transparent top view

Fig. 3. Pin configuration SOT886 (XSON6)



Transparent top view

Fig. 4. Pin configuration SOT1115 and SOT1202 (XSON6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V_{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Inputs			Output
C	**B**	**A**	**Y**
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input NAND	see Fig. 5
2-input NAND with both inputs inverted	see Fig. 8
2-input AND with inverted input	see Fig. 6 and Fig. 7
2-input NOR with inverted input	see Fig. 6 and Fig. 7
2-input OR	see Fig. 8
2-input OR with both inputs inverted	see Fig. 5
2-input XOR	see Fig. 9
Buffer	see Fig. 10
Inverter	see Fig. 11

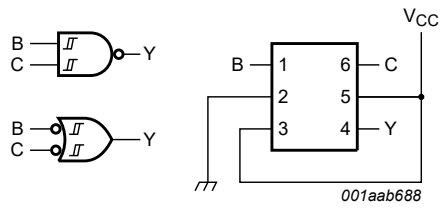


Fig. 5. 2-input NAND gate or 2-input OR with both inputs inverted

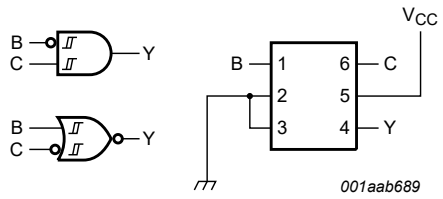


Fig. 6. 2-input AND gate with inverted B input or 2-input NOR gate with inverted C input

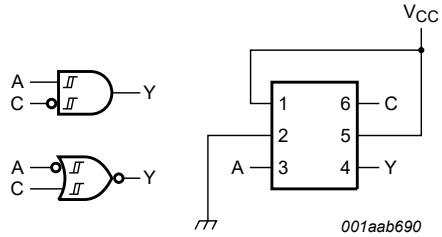


Fig. 7. 2-input AND gate with inverted C input or 2-input NOR gate with inverted A input

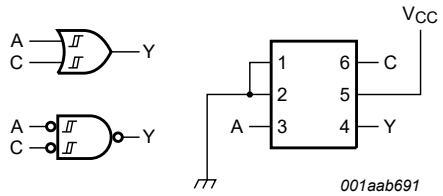


Fig. 8. 2-input OR gate or 2-input NAND gate with both inputs inverted

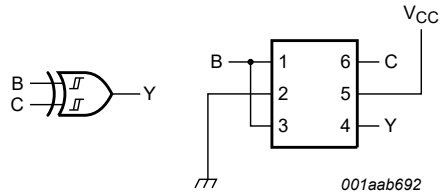


Fig. 9. 2-input XOR gate

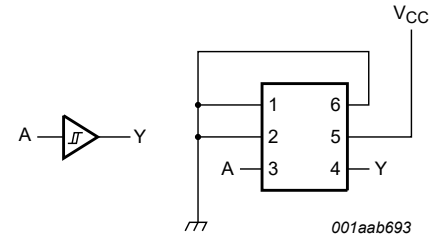


Fig. 10. Buffer

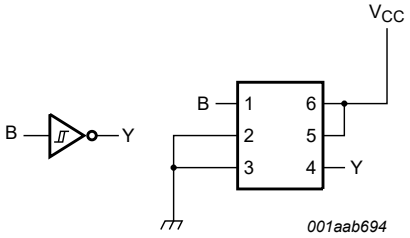


Fig. 11. Inverter

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	+6.5	V
		Power-down mode; $V_{CC} = 0$ V	[1]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.
For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	4	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_I	input capacitance		-	2.5	-	pF

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{OL}	LOW-level output voltage	V_I = V_{T+} or V_{T-}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.7	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{T+} or V_{T-}				
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.4	-	-	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	4	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	500	µA

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

11. Dynamic characteristics

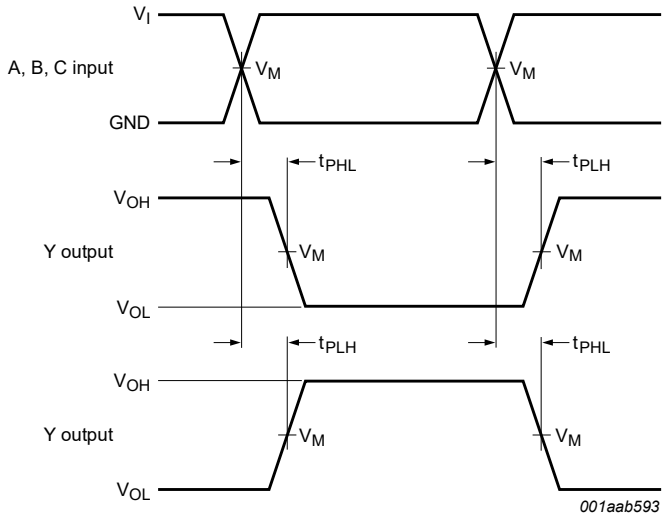
Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18.0	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V_{CC} = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC} [3]	-	20	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



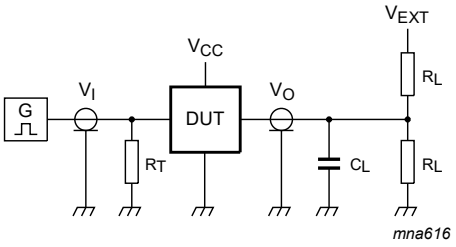
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Input A, B, C to output Y propagation delay times

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 13. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Transfer characteristics

Table 12. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 14, Fig. 15, Fig. 16 and Fig. 17						
		V_{CC} = 1.8 V	0.70	1.02	1.20	0.67	1.20	V
		V_{CC} = 2.3 V	1.11	1.42	1.60	1.08	1.60	V
		V_{CC} = 3.0 V	1.50	1.79	2.00	1.47	2.00	V
		V_{CC} = 4.5 V	2.16	2.52	2.74	2.13	2.74	V
		V_{CC} = 5.5 V	2.61	2.99	3.33	2.58	3.33	V
V_{T-}	negative-going threshold voltage	see Fig. 14, Fig. 15, Fig. 16 and Fig. 17						
		V_{CC} = 1.8 V	0.30	0.53	0.72	0.30	0.75	V
		V_{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V_{CC} = 3.0 V	0.80	1.04	1.30	0.80	1.33	V
		V_{CC} = 4.5 V	1.21	1.55	1.90	1.21	1.93	V
		V_{CC} = 5.5 V	1.45	1.86	2.29	1.45	2.32	V
V_H	hysteresis voltage	(V_{T+} - V_{T-}); see Fig. 14, Fig. 15, Fig. 16 and Fig. 17						
		V_{CC} = 1.8 V	0.30	0.48	0.62	0.23	0.62	V
		V_{CC} = 2.3 V	0.40	0.64	0.80	0.34	0.80	V
		V_{CC} = 3.0 V	0.50	0.75	1.00	0.44	1.00	V
		V_{CC} = 4.5 V	0.71	0.97	1.20	0.65	1.20	V
		V_{CC} = 5.5 V	0.71	1.13	1.40	0.65	1.40	V

[1] Typical values are measured at T_{amb} = 25 °C.

12.1. Waveforms transfer characteristics

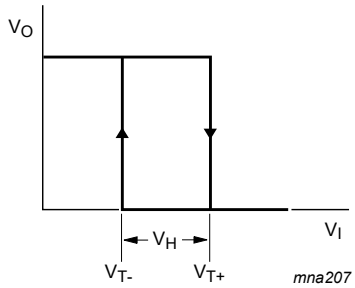
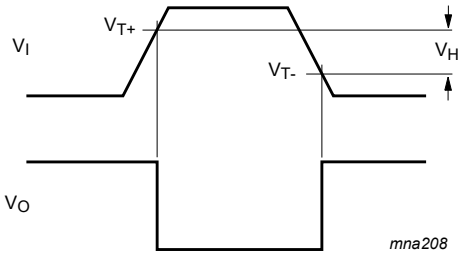


Fig. 14. Transfer characteristics



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig. 15. Definition of V_{T+}, V_{T-} and V_H

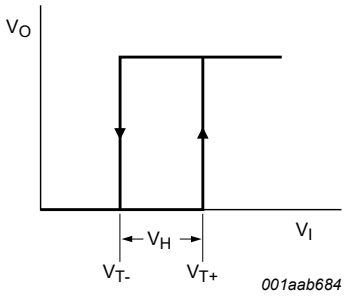
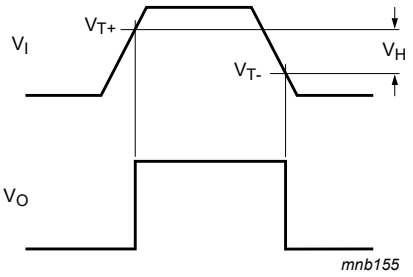


Fig. 16. Transfer characteristics



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig. 17. Definition of V_{T+}, V_{T-} and V_H

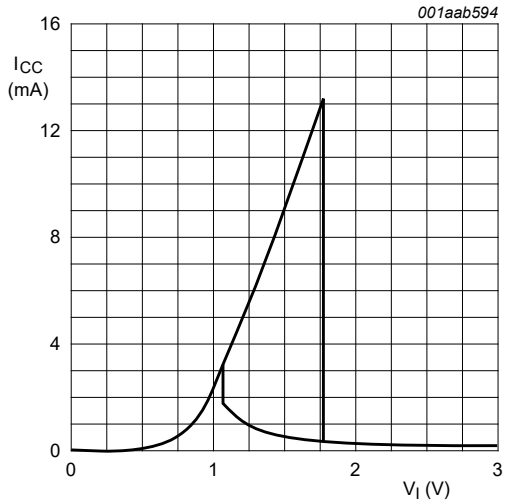
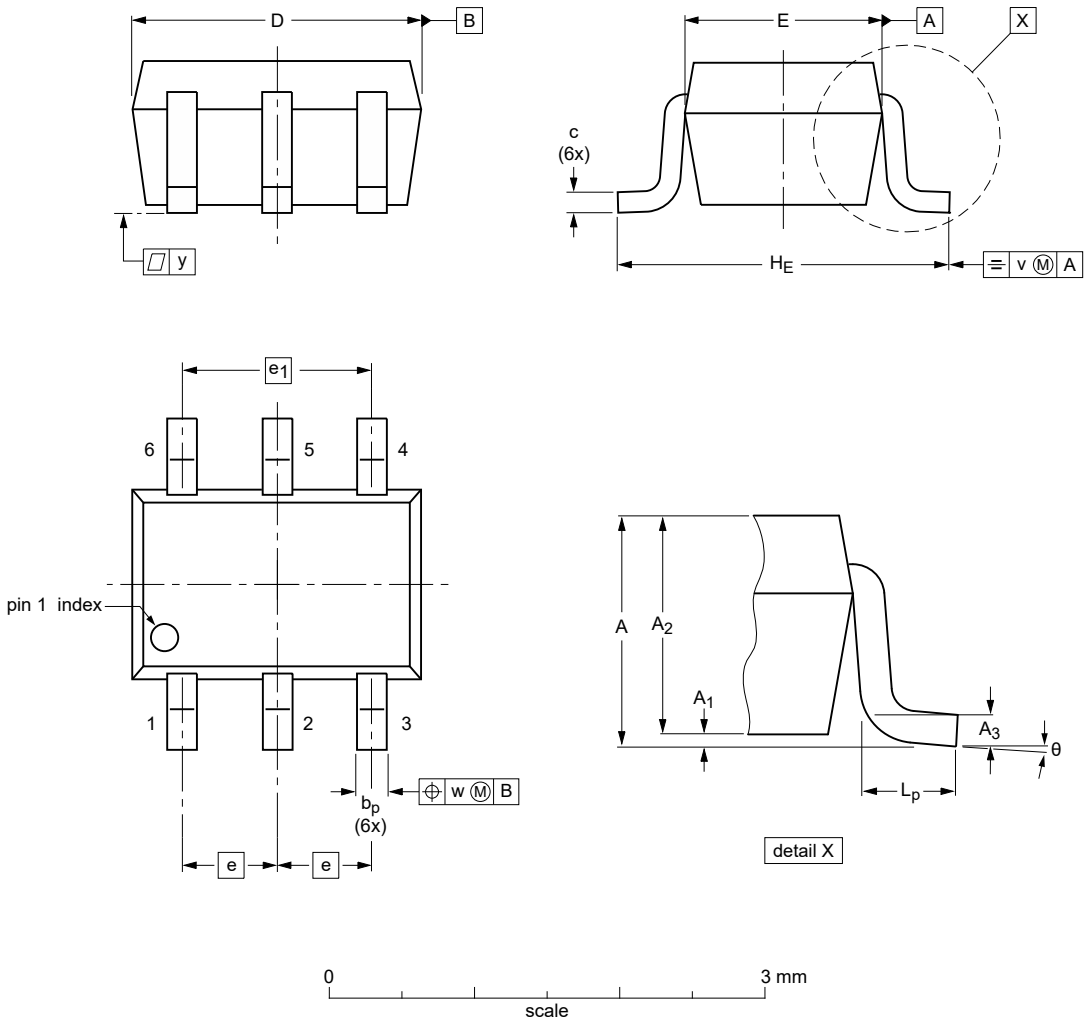


Fig. 18. Typical 74LVC1G58 transfer characteristics; V_{CC} = 3.0 V

13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

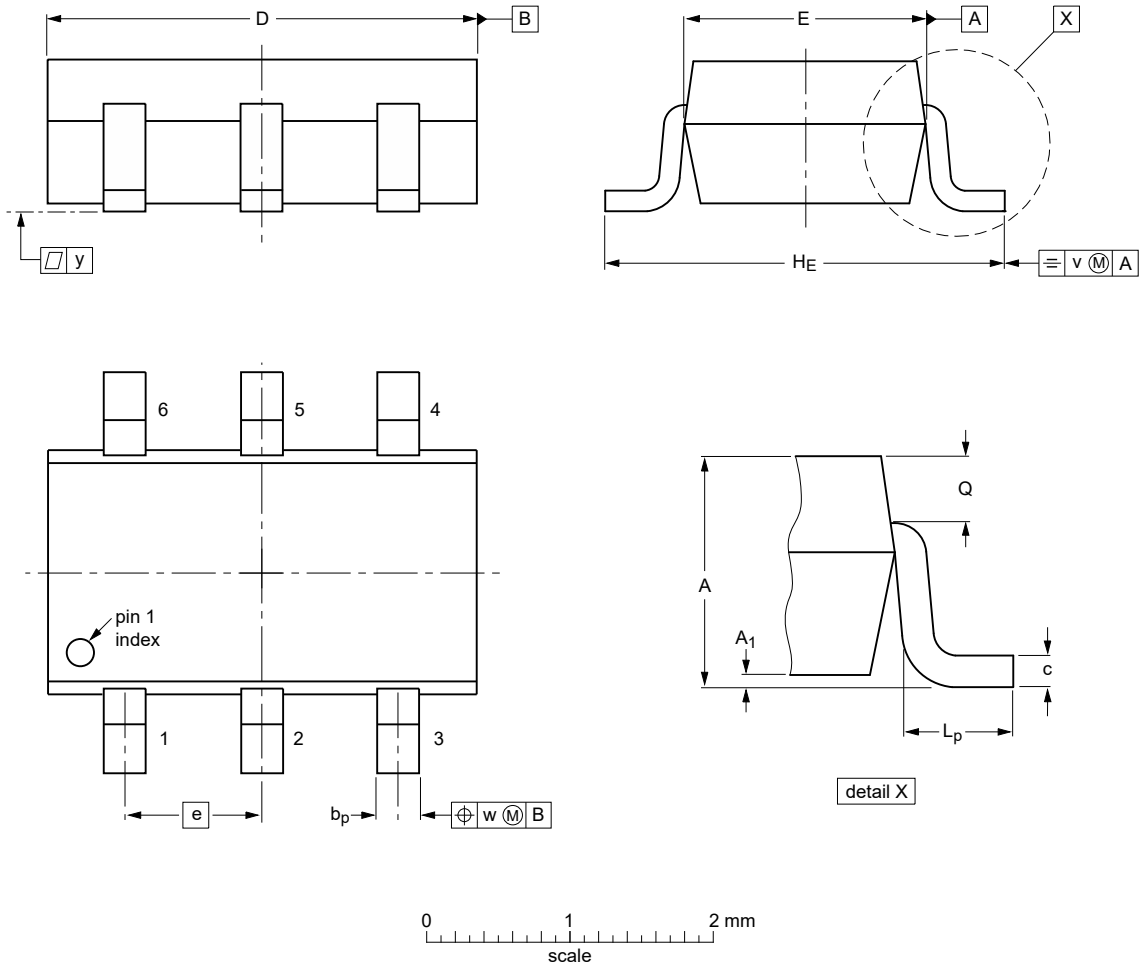
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT363-2		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 19. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads **SOT457**



Dimensions (mm are the original dimensions)

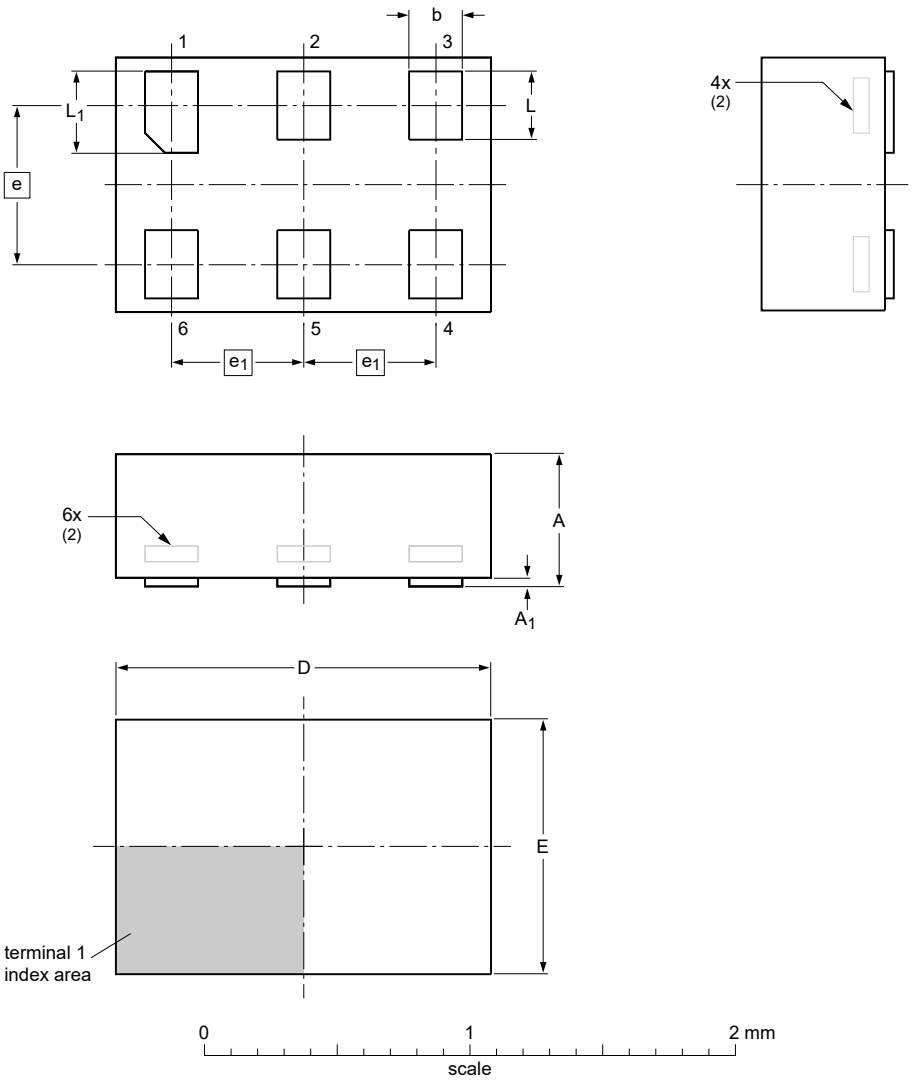
Unit		A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	max	1.1	0.1	0.40	0.26	3.1	1.7		3.0	0.6	0.33	0.2	0.2	0.1
	nom							0.95						
	min	0.9	0.013	0.25	0.10	2.7	1.3		2.5	0.2	0.23			

sot457_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~06-03-16~~ 18-11-27

Fig. 20. Package outline SOT457 (SC-74; TSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

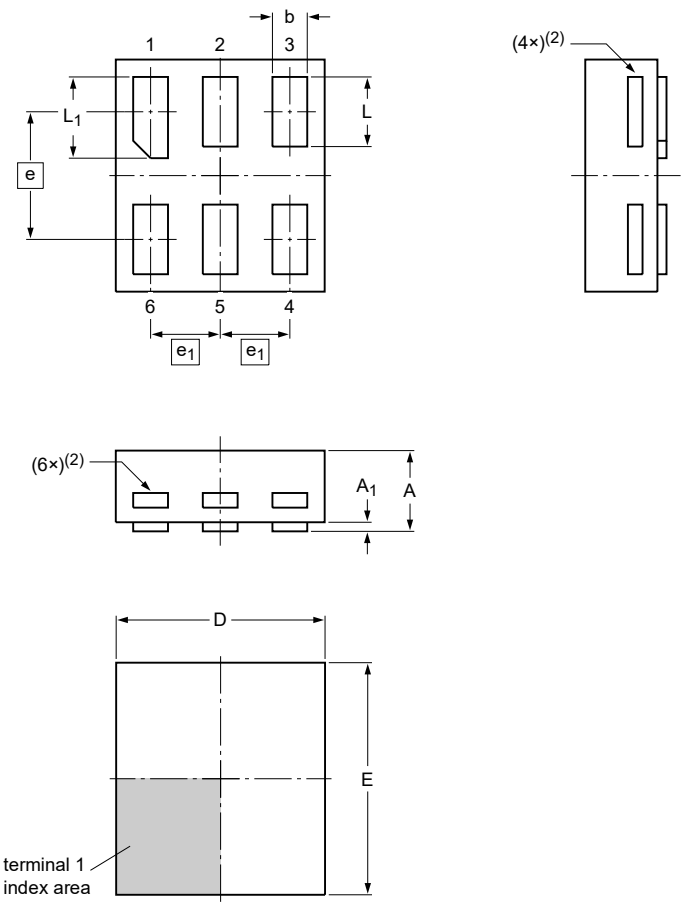
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 21. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

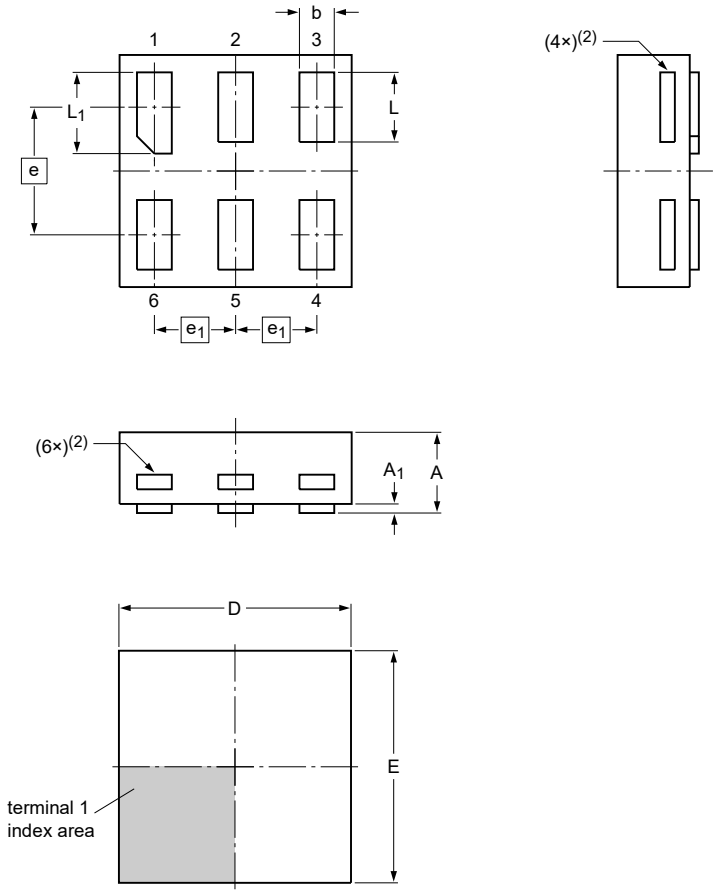
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig. 22. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig. 23. Package outline SOT1202 (XSON6)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G58 v.11	20220201	Product data sheet	-	74LVC1G58 v.10
Modifications:	• Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6).			
74LVC1G58 v.10	20210607	Product data sheet	-	74LVC1G58 v.9
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVC1G58GF (SOT891 / XSON6) removed. • Section 1 and Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated. • Fig. 20: Package outline drawing SOT457 (SC-74; TSOP6) updated.			
74LVC1G58 v.9	20161207	Product data sheet	-	74LVC1G58 v.8
Modifications:	• Table 8: The maximum limits for leakage current and supply current have changed.			
74LVC1G58 v.8	20140422	Product data sheet	-	74LVC1G58 v.7
Modifications:	• Package outline drawing of SOT886 (Fig. 21) modified.			
74LVC1G58 v.7	20111206	Product data sheet	-	74LVC1G58 v.6
Modifications:	• Legal pages updated.			
74LVC1G58 v.6	20110923	Product data sheet	-	74LVC1G58 v.5
74LVC1G58 v.5	20101015	Product data sheet	-	74LVC1G58 v.4
74LVC1G58 v.4	20090427	Product data sheet	-	74LVC1G58 v.3
74LVC1G58 v.3	20070827	Product data sheet	-	74LVC1G58 v.2
74LVC1G58 v.2	20070222	Product data sheet	-	74LVC1G58 v.1
74LVC1G58 v.1	20040915	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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