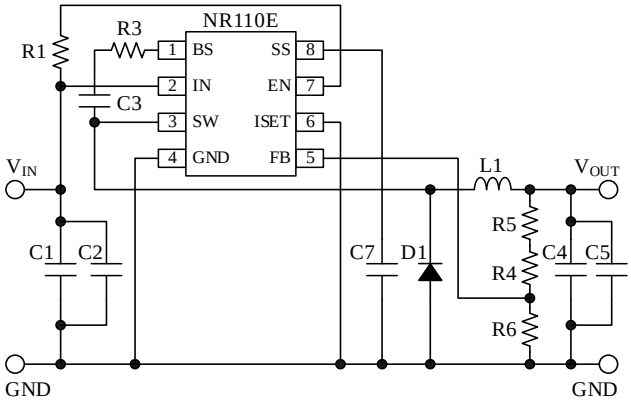
Description

The NR110E series are buck converter ICs that integrate the power MOSFET. With the current mode control, ultra low ESR capacitors such as ceramic capacitors can be used. The ICs have protection functions such as Overcurrent Protection (OCP), Undervoltage Lockout (UVLO) and Thermal Shutdown (TSD). An adjustable Soft-start by an external capacitor prevents the excessive inrush current in startup. The feature increasing efficiency at light loads allows the device to be used in the energy-saving applications. The ICs integrate phase compensation circuit which reduces the number of external components and simplifies the design of customer application. The IC has the enable function by the EN pin that turns the regulator on or off. The package of NR110E series is the eSOIC8 with an exposed thermal pad on the back side.

Features

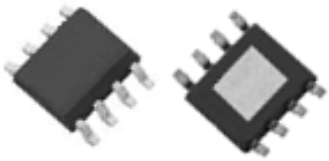
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Up to 94% Efficiency
  Up to 68% Efficiency at Maximum at Light Load
  (V_{IN} = 12 V, V_O = 5 V, I_O = 20 mA)
- Current mode PWM control
- Stable with Low ESR Ceramic Output Capacitors
- No External Components Required by Incorporating Phase Compensation
- Soft-start Function
  Adjustable Soft-start time with an External Capacitor
- Enable Function
- Protection Functions:
  Overcurrent Protection (OCP): Drooping, auto-restart
  Thermal Shutdown (TSD): Auto-restart
  Undervoltage Lockout (UVLO)

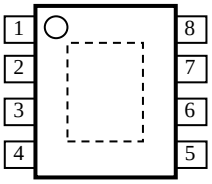
Typical Application



Package

eSOIC8





Not to scale

Selection Guide

- Specifications
  Input Voltage, V_{IN}: 6.5 V to 31 V
  Output Voltage, V_O: 0.8 V to 24 V

Part Number	I_{OUT} (max.)	f_{OSC} (typ.)
NR111E	4 A	350 kHz
NR119E	2 A	364 kHz

Applications

- AV Equipment
- Auxiliary Power Supply

Contents

1. Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
DC Input Voltage	V_{IN}		35	V	
BS Pin Voltage	V_{BS}		44	V	
BS–SW Voltage	V_{BS-SW}	DC	8	V	
		Pulse width ≤ 30ns	12		
SW Pin Voltage	V_{SW}		35	V	
FB Pin Voltage	V_{FB}		5.5	V	
EN Pin Voltage	V_{EN}		35	V	
SS Pin Voltage	V_{SS}		5.5	V	
Power Dissipation (1)	P_D	The IC is mounted on the glass-epoxy board (30 mm × 30 mm) with copper area (25 mm × 25 mm) by reflow soldering $T_{J(MAX)}$ = 150 °C	1.76	W	
Junction Temperature (2)	T_J		–40 to 150	°C	
Storage Temperature	T_{STG}		–40 to 150	°C	
Thermal Resistance (junction–GND Pin)	θ_{JP}		26	°C/W	
Thermal Resistance (junction–ambient air)	θ_{JA}	The IC is mounted on the glass-epoxy board (30 mm × 30 mm) with copper area (25 mm × 25 mm) by reflow soldering	71	°C/W	

(1) Limited by thermal shutdown.
(2) The temperature detection of thermal shutdown is about 160 °C.

2. Recommended Operating Conditions

Parameter	Symbol	Ratings		Units	Remarks
		Min.	Max.		
DC Input Voltage (1)	V_{IN}	6.5	31	V	
DC Output Current (2)(3)	Io	0	4.0	A	NR111E
		0	2.0	A	NR119E
Output Voltage	V_O	0.8	24	V	
Ambient Operating Temperature (3)	T_{OP}	–40	85	°C	

(1) The minimum value of input voltage is taken as the larger one of either 6.5 V or V_O +3 V.
(2) See Typical Application Circuit for recommended circuit.
(3) To be used within the allowable package power dissipation characteristics.

3. Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Reference Voltage		V_{REF}	V_{IN} = 12 V, I_O = 1.0 A	0.784	0.800	0.816	V	
Output Voltage Temperature Coefficient		$\Delta V_{REF}/\Delta T$	V_{IN} = 12 V, I_O = 1.0 A, –40 °C to 85 °C	—	±0.05	—	mV/°C	
Switching Frequency		f_{OSC}	V_{IN} = 12 V, V_O = 5 V, I_O = 1.0 A	280	350	420	kHz	NR111E
				291	364	437	kHz	NR119E
Line Regulation (4)		V_{Line}	V_{IN} = 8 V to 30 V, V_O = 5 V, I_O = 1.0 A	—	50	—	mV	
Load Regulation (4)		V_{Load}	V_{IN} = 12 V, V_O = 5 V, I_O = 0.1 A to 2.0 A	—	50	—	mV	
Overcurrent Protection Threshold		I_S	V_{IN} = 12 V, V_O = 5 V, ISET = GND	—	5.5	—	A	NR111E
			V_{IN} = 12 V, V_O = 5 V, ISET = GND	—	2.8	—	A	NR119E
Supply Current		I_{IN}	V_{IN} = 12 V, V_O = 5 V, I_O = 0 A	—	1.0	—	mA	
Shutdown Supply Current		$I_{IN(off)}$	V_{IN} = 12 V, V_O = 5 V, I_O = 0 A, V_{EN} = 0 V	—	1.0	—	µA	
SS Pin	Source current at Low Level Voltage	$I_{EN/SS}$	V_{SS} = 0 V, V_{IN} = 12 V	6	10	14	µA	
EN Pin	Sink Current	I_{EN}	V_{EN} = 10 V	—	20	50	µA	
	Threshold Voltage	V_{EN}	V_{IN} = 12 V	0.7	1.4	2.1	V	
Max On-duty (4)		D_{MAX}		—	90	—	%	
Minimum On-time (4) (5)		$t_{ON(MIN)}$		—	150	—	ns	NR111E
				—	220	—	ns	NR119E
Thermal Shutdown Threshold Temperature (4)		TSD		151	165	—	°C	
Thermal Shutdown Restart Hysteresis of Temperature (4)		TSD_hys		—	20	—	°C	
High-side Switch On Resistance (4)		$R_{ON(H)}$		—	85	—	mΩ	NR111E
				—	150	—	mΩ	NR119E

(4) Guaranteed by design, not tested.
(5) Input/ Output conditions are controlled by the minimum on time.

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.08	—	g

5. Typical Performance Characteristics

5.1. NR111E

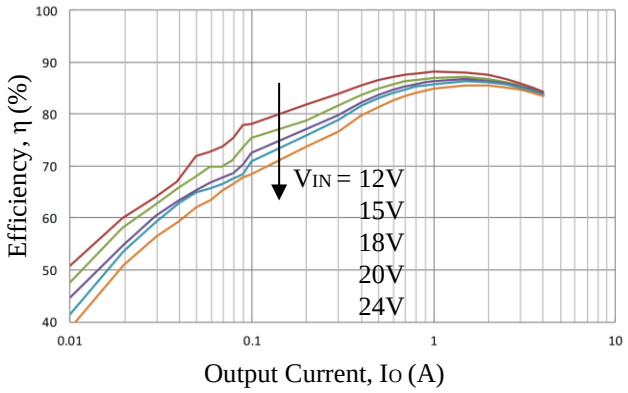


Figure 5-1. Efficiency (Vo = 3.3 V)

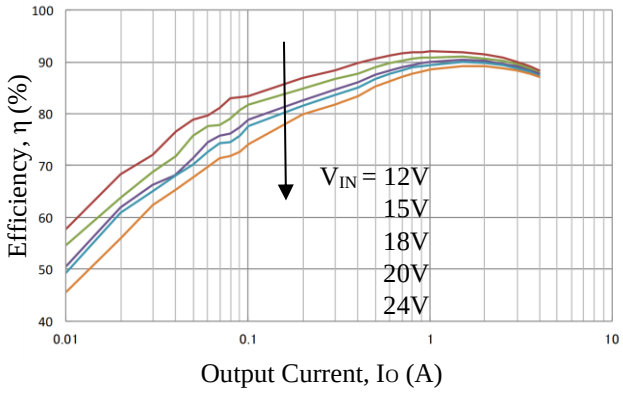


Figure 5-2. Efficiency (Vo = 5.0 V)

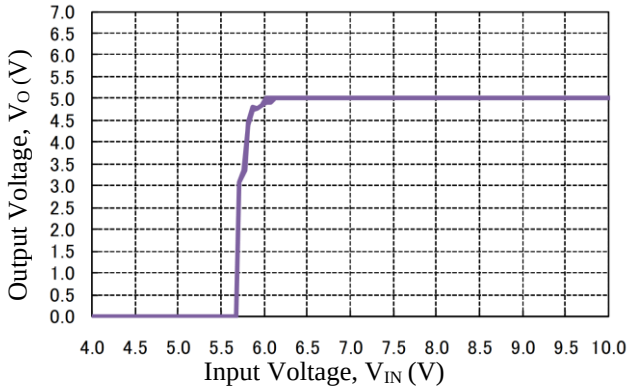


Figure 5-3. Output Startup (Load = CR)

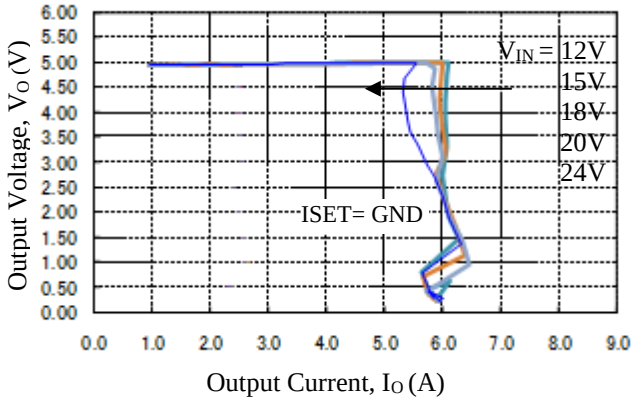


Figure 5-4. Overcurrent Protection

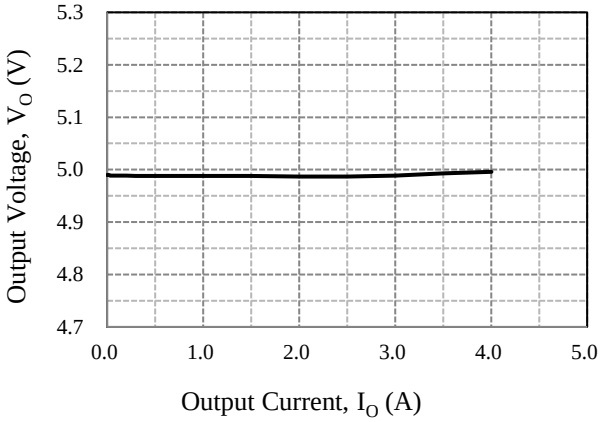


Figure 5-5. Load Regulation

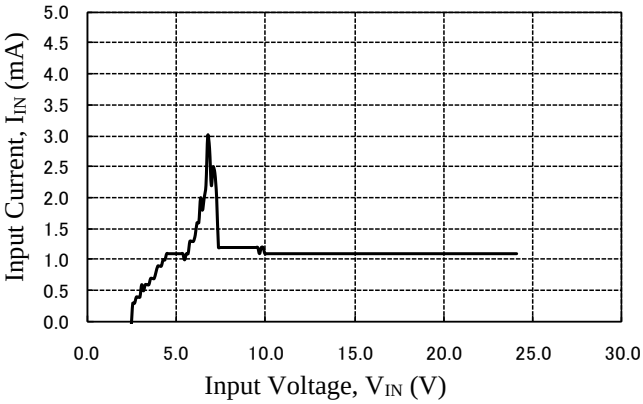


Figure 5-6. IN Pin Sink Current at No Load

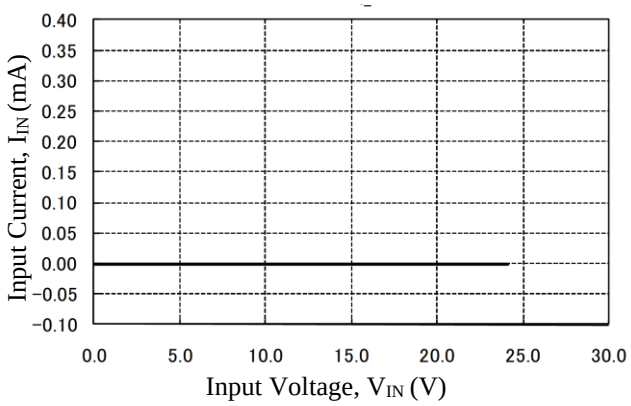


Figure 5-7. Quiescent Current

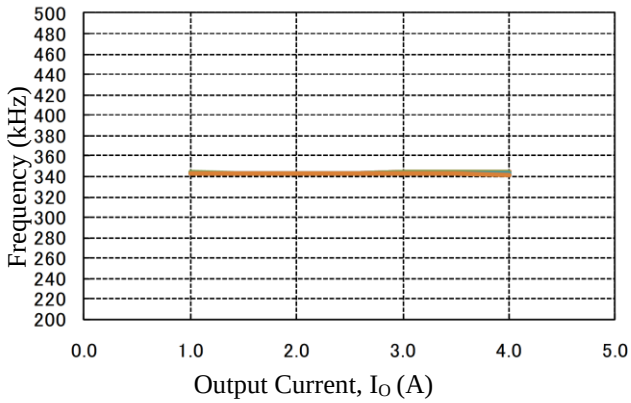


Figure 5-8. Operating Frequency

5.2. NR119E

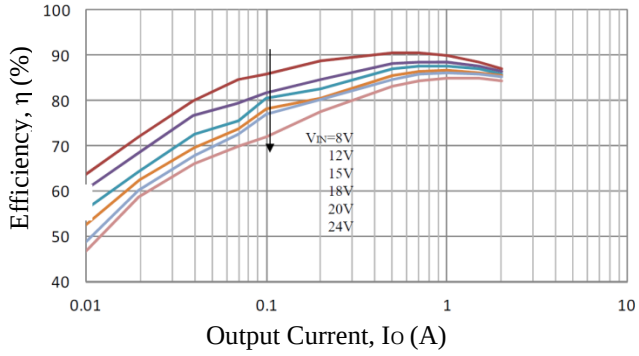


Figure 5-9. Efficiency (Vo = 3.3 V)

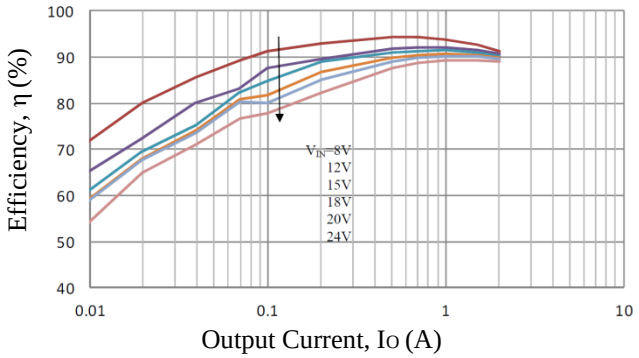


Figure 5-10. Efficiency (Vo = 5.0 V)

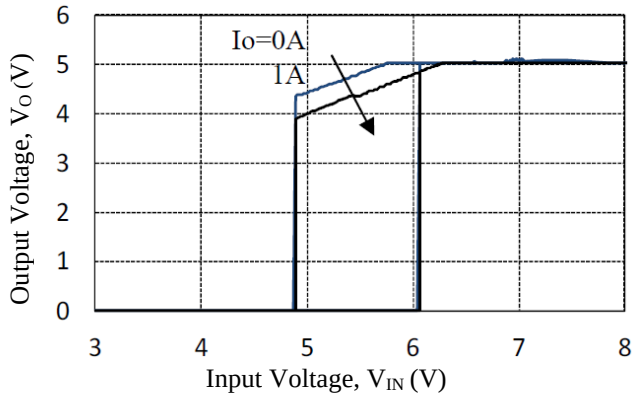


Figure 5-11. Output Startup (Load = CR)

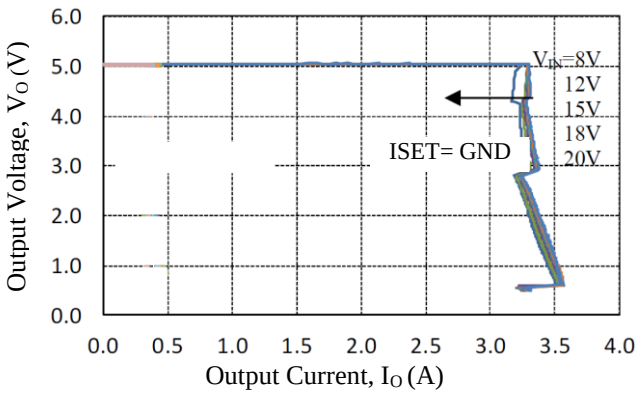


Figure 5-12. Overcurrent Protection

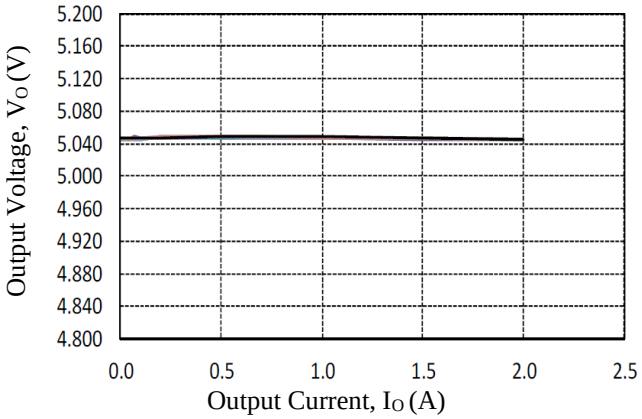


Figure 5-13. Load Regulation

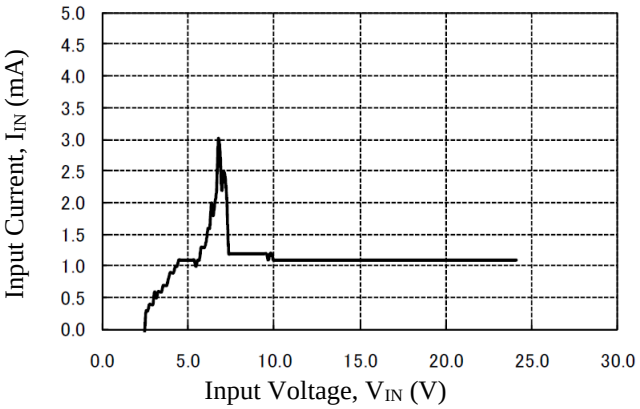


Figure 5-14. IN Pin Sink Current at No Load

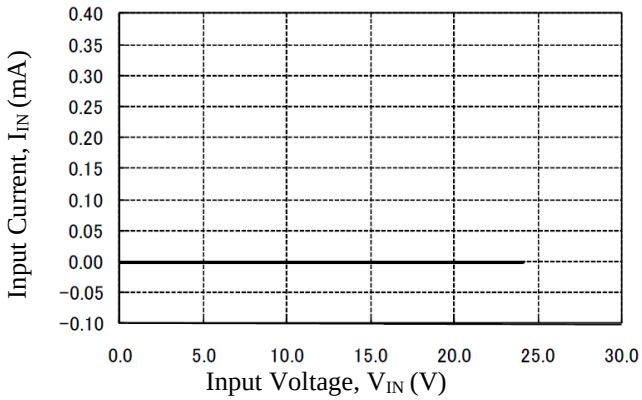


Figure 5-15. Quiescent Current

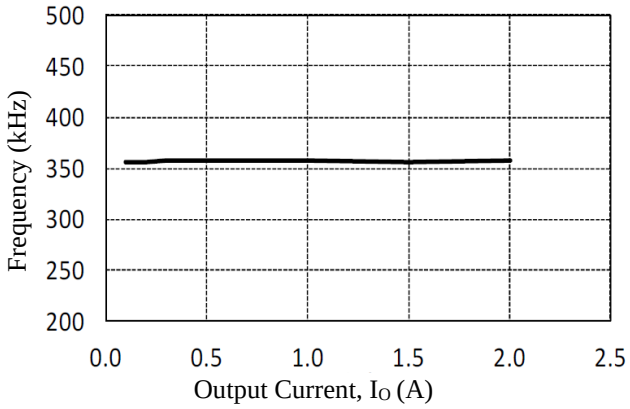
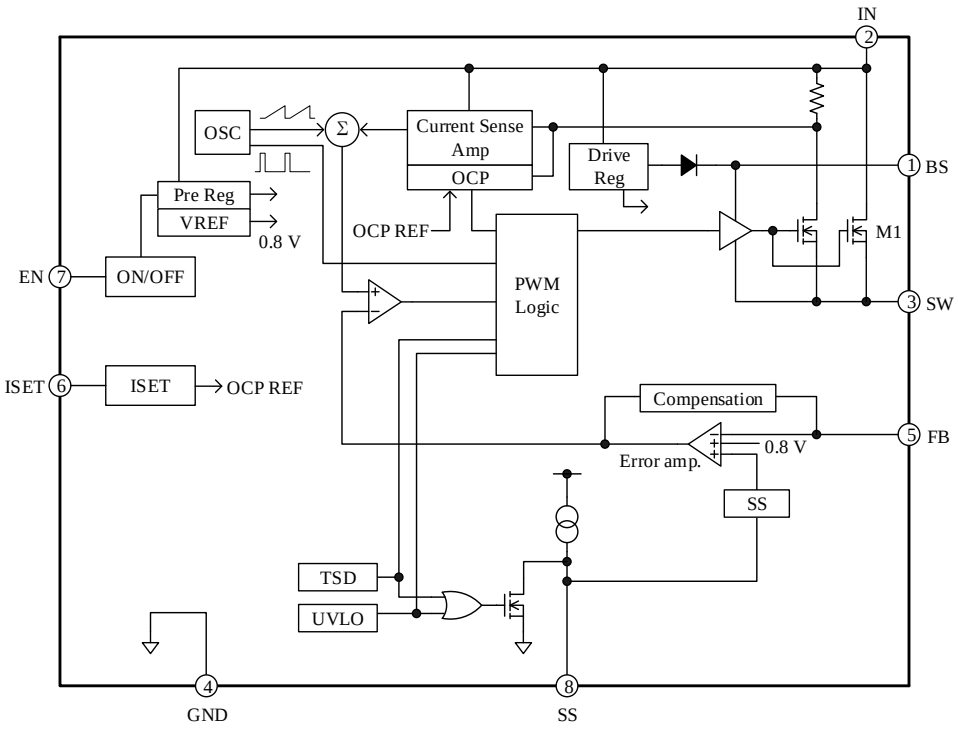
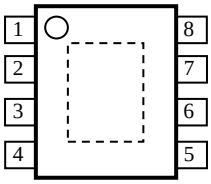


Figure 5-16. Operating Frequency

6. Block Diagram

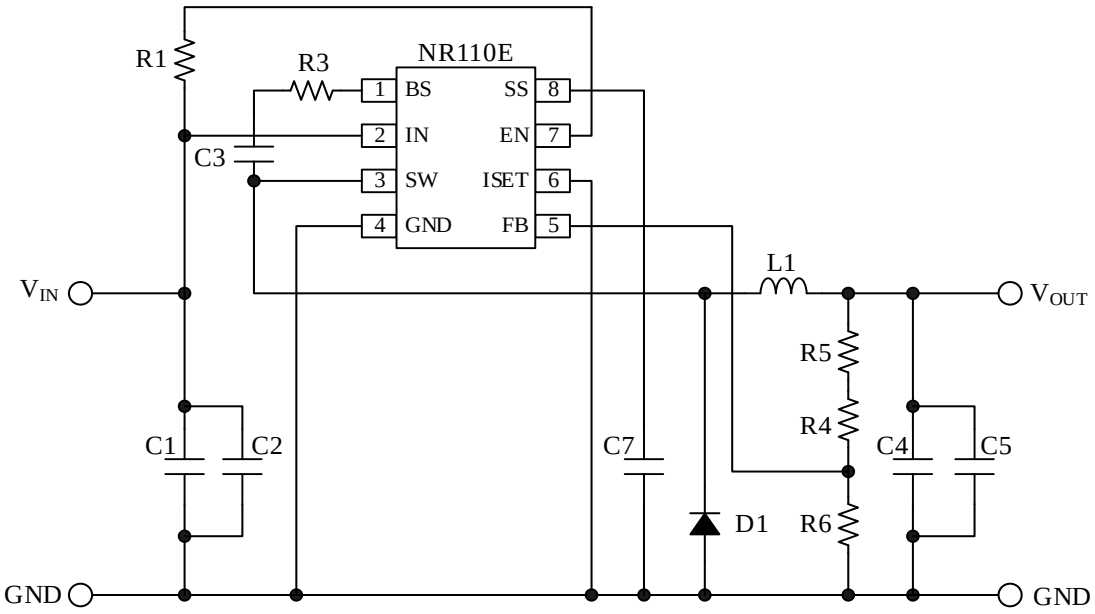


7. Pin Configuration Definitions



Pin	Name	Descriptions
1	BS	High-side boost input pin. The power is supplied to the driver of high-side N-channel MOSFET through the BS pin. A capacitor and a resistor are connected in series between the SW pin and the BS pin.
2	IN	This pin is input pin. The power is supplied to the IC through the IN pin.
3	SW	This pin is output pin. The power is output through the SW pin. Connect the LC filter for the output to this pin. A capacitor is required to be connected between this pin and the BS pin to supply the power to the high-side MOSFET.
4	GND	Ground pin. The exposed pad must be connected to the GND pin.
5	FB	To control constant voltage, the output voltage is input to the FB pin, and is compared with internal reference voltage. The feedback threshold voltage is 0.8 V. The output voltage is set by resistors connected to the FB pin. R5 and R6 are connected between the FB pin and output line. R4 is connected between the FB pin and the GND pin.
6	ISET	OCP setting pin. This pin must be shorted to the ground.
7	EN	Enable signal input pin. When high signal is input to this pin, the internal regulator turns on. When low signal is input to this pin, the internal regulator turns off.
8	SS	Soft-start input. The soft-start period can be adjusted by the capacitor connected between the SS pin and the GND pin. The soft-start operation reduces the over-shoot of the output voltage and rush current.

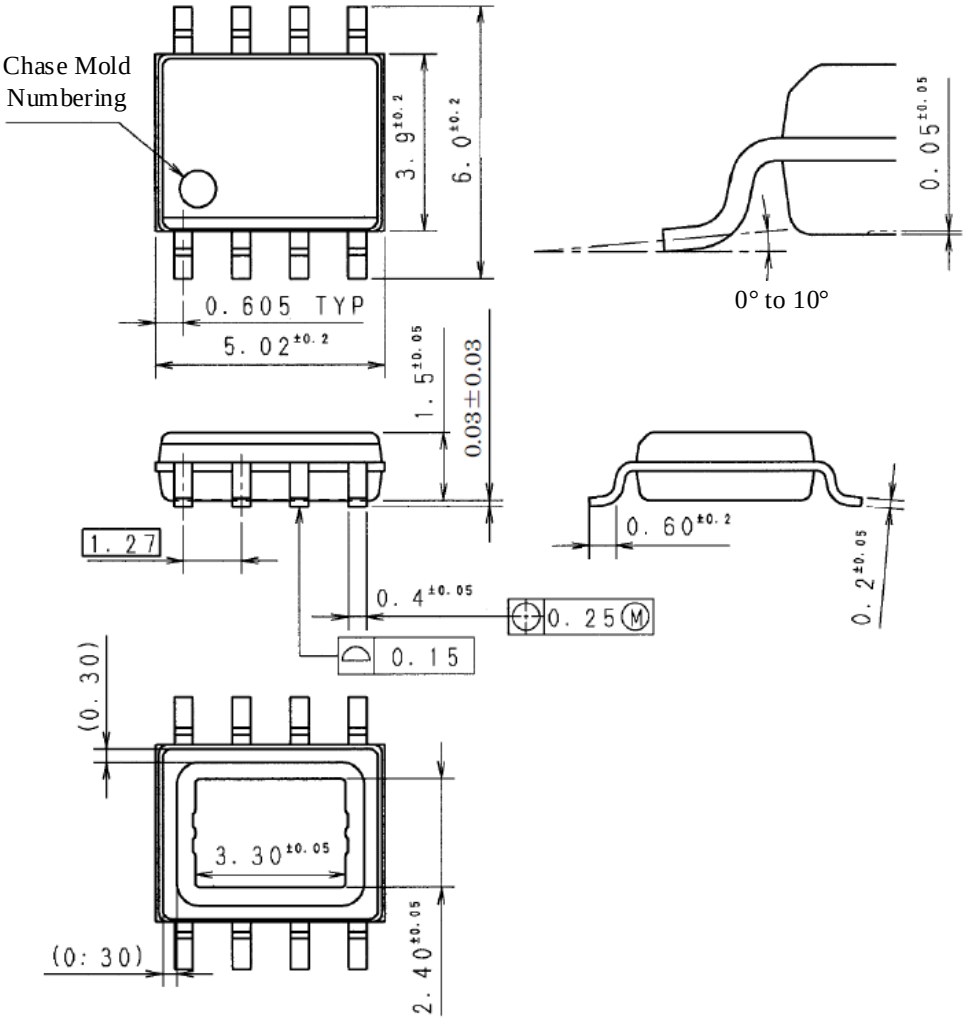
8. Typical Application



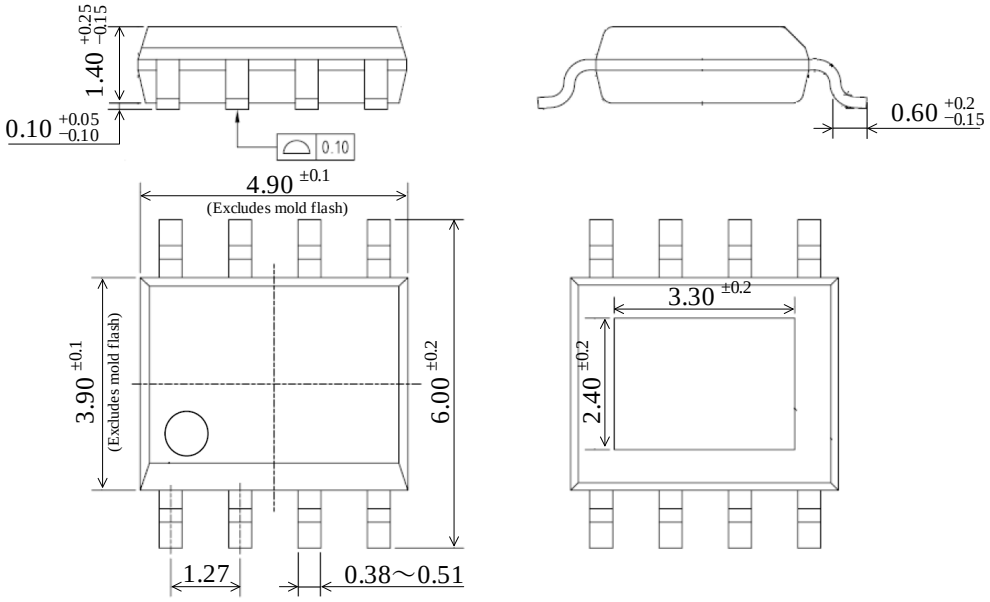
Symbol	Ratings	Symbol	Ratings
C1	10 µF / 35 V	R1	510 kΩ
C2	10 µF / 35 V	R3	22 Ω
C3	0.1 µF	R4	18 kΩ
C4	22 µF / 16 V	R5	2.7 kΩ (Vo = 5.0 V)
C5	22 µF / 16 V	R6	3.9 kΩ
C7	0.1 µF	L1	10 µH
		D1	40 V, 5 A (Schottky diode)

9. Physical Dimensions

● eSOIC8 (NR111E)



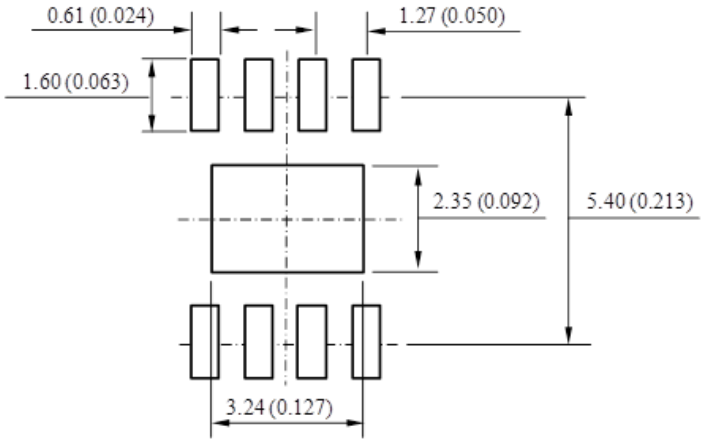
● eSOIC8 (NR119E)



NOTES:

- Dimensions in millimeters
- Not to scale
- Bare lead frame: Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Reflow
  Preheat: 150 °C to 200 °C / 60 s to 120 s
  Solder heating: 255 °C / 30 s, 3 times (260 °C peak)
  Soldering iron: 350 °C / 3.5 s, 1 time

● Recommended Land Pattern

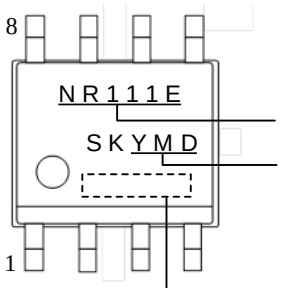


NOTES:

- Dimensions in millimeters (inches)
- Not to scale

10. Marking Diagram

● NR111E

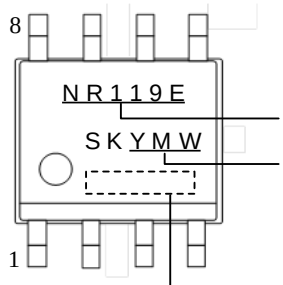


Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is the period of days represented by:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

● NR119E



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
W is the week of the month (1 to 5)

Control Number

11. Operational Description

11.1. PWM Output Control

The IC consists of total three blocks; two feedback loop systems (current control and voltage control) and one slope compensation. For the voltage control feedback, divided output voltage by resistor is input to the FB pin. The internal error amplifier compares the FB pin voltage with the reference voltage V_{REF} = 0.8V.

For the current control feedback, the loop makes the coil current feedback to the PWM control. The coil current that is branched by using sense MOSFET is detected by the current sense amplifier. In addition, the slope compensation is made for current control slope in order to prevent subharmonic oscillations.

The PWM control with current control method is achieved by calculating the voltage control feedback, the current control feedback and the slope compensation signals. (See Figure 11-1.)

When UVLO is released or the EN pin or the SS pin voltage exceeds the threshold, the IC starts the switching operation.

The IC starts switching operation with minimum on-duty or maximum on-duty. The high-side switching MOSFET, M1, is for supplying output power.

At startup of IC, the SW pin becomes low status during short time to charge the boost capacitor, C3, for M1 driving.

When M1 is on-status, the coil current is increased by applying the voltage the SW pin and the coil. In addition, the output of the current sense amplifier also increases.

Signal A is sum of the current sense amplifier output and slope compensation signal. The comparator compares the signal A with the error amplifier output. When the signal A exceeds the output voltage of the error amplifier (Error Amp.), the current comparator output becomes “H” and the RS flip-flop circuit in PWM logic is reset. Then, M1 turns off, and the regenerative current flows through the Schottky diode, D1.

The set signal is generated in each cycle, and set the RS flip-flop circuit.

If the signal A does not exceed the output voltage of the error amplifier (Error Amp.), the signal of off duty circuit sets RS flip-flop circuit.

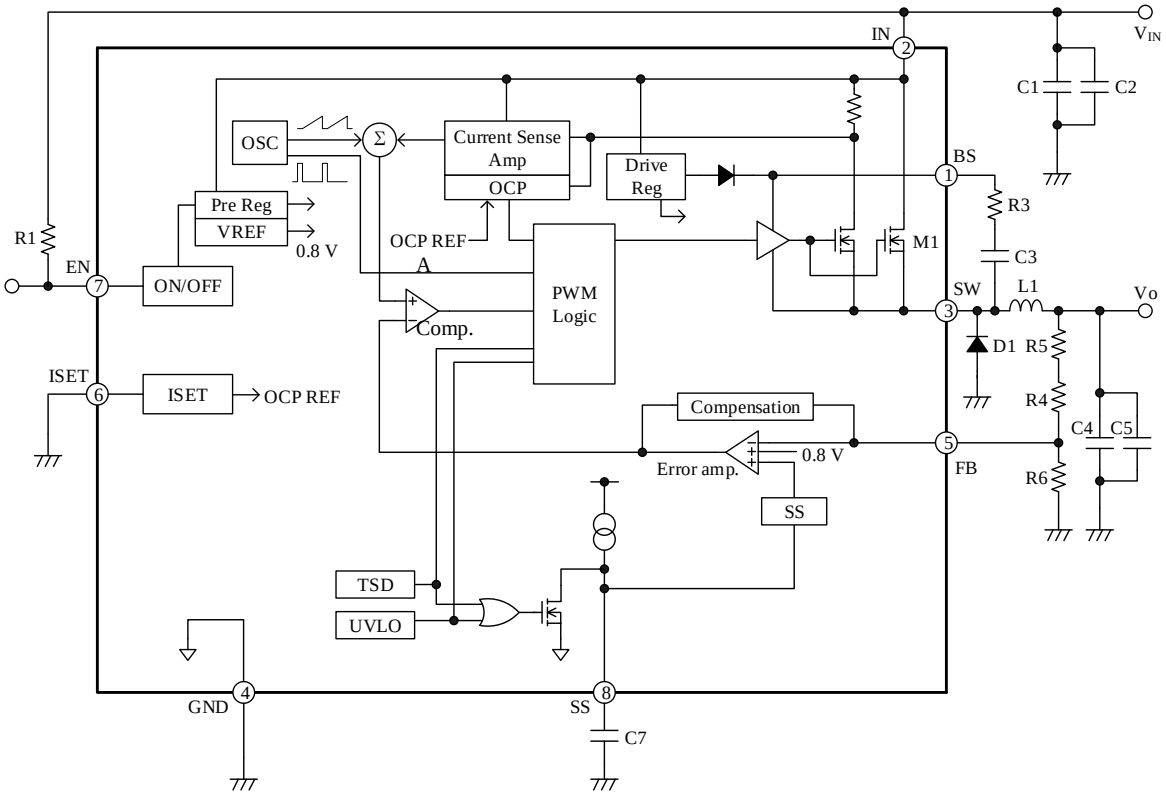


Figure 11-1. Basic Structure of Chopper Type Regulator with PWM Control by Current Control

11.2. Soft Start Function

Figure 11-2 shows the SS pin internal circuit.

When capacitor, C_{SS}, is connected to the SS pin, the IC operates in soft start at startup. The output voltage, V_O, increases depending on the charged voltage of C_{SS}.

Delay time, t_{DELAY} is calculated by Equation (1). Soft start time, t_{SS} is calculated by Equation (2).

If the soft start function is unused, the SS pin is unconnected (open status).

$$t_{DLAY} = C_{SS} \times \frac{0.9\ (V)}{I_{SS}} \quad (1)$$

$$t_{SS} = C_{SS} \times \frac{1.8\ (V) - 0.9\ (V)}{0.9 \times I_{SS}} \quad (2)$$

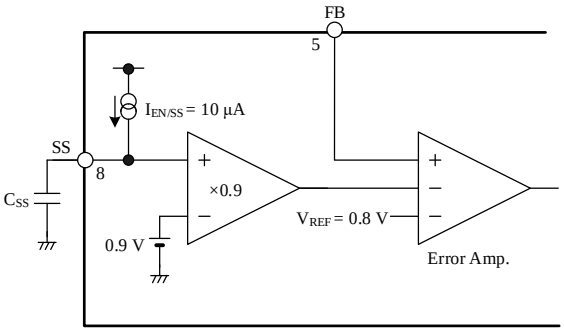


Figure 11-2. SS Pin Internal Circuit

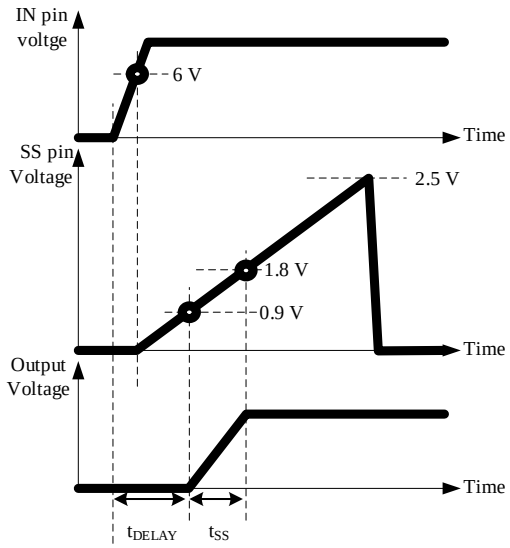


Figure 11-3. Soft Start Operation Waveform

SS pin voltage at open is 3.0 V. Figure 11-4 shows the relationship between the C_{SS} discharge time and C_{SS} capacitance. C_{SS} discharge time is require time that the SS pin voltage decreases to 0 V from 3.0 V

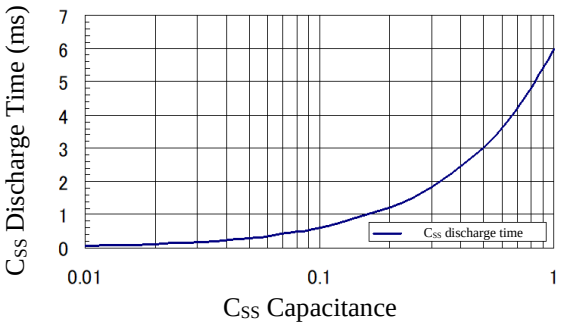


Figure 11-4. C_{SS} Discharge Time vs. C_{SS} Capacitance

In case the C_{SS} is short circuit status or the C_{SS} value is set too small, the output capacitor is charged by the output current that is limited by overcurrent protection threshold current, Is.

In the case, the time constant is calculated by Equation (3). This time constant is in no load status. When the circuit has some load, the load current is subtracted from Is.

$$t = \frac{C_{OUT} \times V_O}{I_S} \quad (3)$$

11.3. Enable Function

When the external signal is input to EN pin, the IC turns on/off the output.

When the EN pin voltage is decreased to V_{EN} = 1.4 V or less by open collector switch as shown in Figure 11-5, the switching operation stops.

When the enable function is unused, pull up the EN pin to the IN pin by resister (510 kΩ) as shown in Figure 11-6.

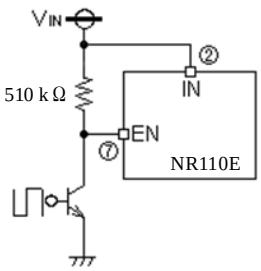


Figure 11-5. Enable Function

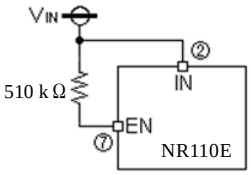


Figure 11-6. Enable Function Disabled

11.4. Overcurrent Protection

The IC has an overcurrent protection (OCP) circuit. The OCP circuit detects the peak current of the switching transistor. When the peak current exceeds the setting current, the IC limits the current by forcibly shortening the on-time of transistor and decreasing the output voltage (see Figure 11-7). When the overcurrent state is released, the output voltage automatically returns.

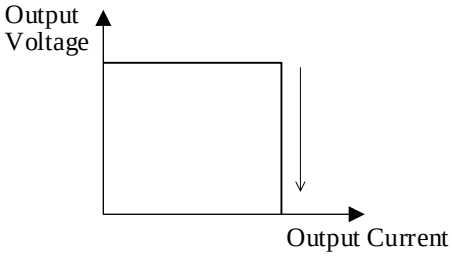


Figure 11-7. Output Voltage Characteristics at Overcurrent

The output current, I_O, can be calculated using the OCP operation current, I_P as shown in Equation (6) or Equation (8).

When the on-duty is 50% or less, the inductance, L, is recommended to be the value that ΔI_L is 0.3 A to 1.2 A.

You must set the inductance that satisfies output current, I_O, from the specifications (input voltage and output voltage) and I_P.

The ripple current of the choke coil, ΔI_L, is calculated as follows:

$$\Delta I_L = \frac{(V_{IN} - V_O)}{L \times V_{IN} \times f} \times V_O \quad (4)$$

where,
V_{IN} is input voltage,
V_O is output voltage,
L is inductance the choke coil, and
f is switching frequency.

In the continuous conduction mode (CCM), output current, I_O, is calculated as follows:

$$I_O \geq \frac{\Delta I_L}{2} \quad (5)$$

$$I_O = I_P - \frac{\Delta I_L}{2} \quad (6)$$

In the discontinuous conduction mode (DCM), output current, I_O, is calculated as follows:

$$I_O < \frac{\Delta I_L}{2} \quad (7)$$

$$I_O = \frac{L \times V_{IN} \times f}{2 \times V_O \times (V_{IN} - V_O)} \times {I_P}^2 = \frac{1}{2 \times \Delta I_L} \times {I_P}^2 \quad (8)$$

11.5. Thermal Shutdown

The thermal shutdown (TSD) circuit detects the junction temperature of the IC. When the junction temperature exceeds about 160 °C, TSD circuit is activated and stops the switching of the output transistor. Then, the output voltage decreases.

When the junction temperature decreases about 20 °C from the TSD circuit activation temperature, the output voltage automatically returns.

The TSD circuit protects from the heat generation for short time such as momentary short circuit. The operation and the reliabilities of the IC are not guaranteed under the continuous heat generation conditions such as short circuit for a long time.

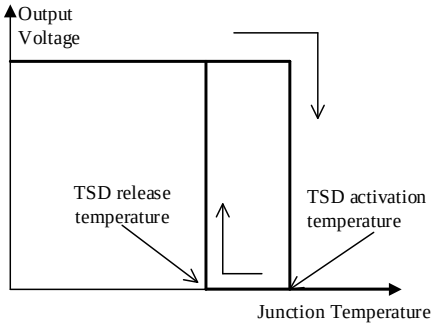


Figure 11-8. Output Voltage Characteristics of Thermal Shutdown

12. Design Notes

12.1. External Components

Take care to use properly rated, including derating as necessary and proper type of components.

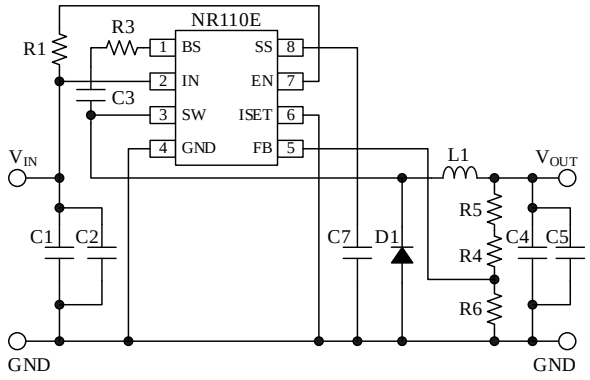


Figure 12-1. The IC Peripheral Circuit

12.1.1. Choke Coil, L1

The choke coil, L1, is the most important component in chopper type switching regulators. In order to keep the stabilized regulator operation, the coil must be avoided the unsafe operation including the saturation condition or the over-heat excessively.

If the winding resistance of the choke coil is too high, the efficiency decreases and may not be the setting value.

The overcurrent protection threshold of NR111E is 5.5 A (Typ.). The overcurrent protection threshold of NR119E is 2.8 A (Typ.). You must consider about the self-heating of the choke coil at the status including overload and the momentary short circuit. The selection points of the choke coil are as follows:

- **Select choke coil for switching regulator.**
  It is not recommended to use the coil for noise filter, since its power dissipation becomes high and causes high heat generation.

- **Avoid a sub-harmonic oscillations.**
  The current control that detects peak current may cause a sub-harmonic oscillation theoretically in the condition that the on-duty is over 50%.
  In the sub-harmonic oscillation, coil current is changed by the integer multiple of switching frequency. Thus, the IC compensates the coil current in internal to operate stably.
  Therefore, the inductance must be selected properly according to output voltage.
  Figure 12-2 shows the inductance selection range to avoid a sub-harmonic oscillation in the on-duty over 50%. The value in Figure 12-2 is reference value, since the maximum inductance is changed by some conditions including input voltage, output voltage and output current.

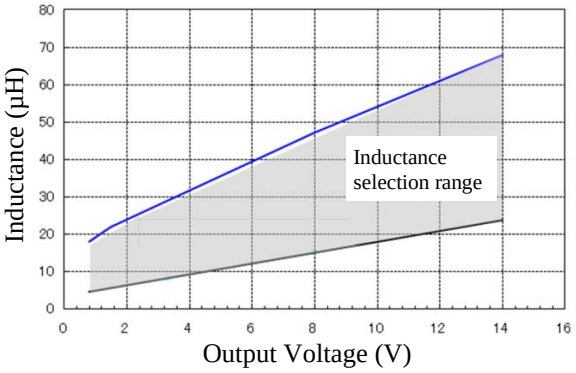


Figure 12-2. Inductance Selection Range in f = 30 kHz

ΔI_L is the ripple current of the choke coil. I_{LP} is the peak current of the choke coil.

ΔI_L and I_{LP} are calculated by following equations.

$$\Delta I_L = \frac{(V_{IN} - V_O)}{L \times V_{IN} \times f} \times V_O \quad (9)$$

$$I_{LP} = \frac{\Delta I_L}{2} \times I_{OUT} \quad (10)$$

As above equations, ΔI_L and I_{LP} increase according to decreasing the inductance, L. Thus, too small inductance setting may cause the unstable operation of the switching regulator because the coil current ripple becomes large.

You must consider that the inductance of the choke coil decreases in the magnetic saturation condition such as overload and short circuit of load.

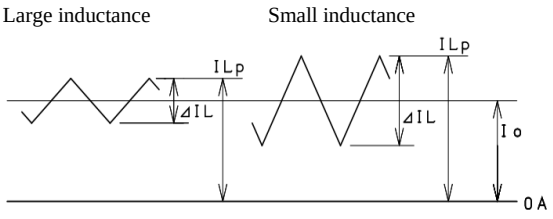


Figure 12-3. Ripple Current of Choke Coil

- **Fulfill the rated current.**
  The rated current value of the choke coil must be set larger than the maximum load current, which is used.
  If the load current exceeds to the rated current value of the coil, the inductance of the coil decreaes rapidly and large current flows.

- **Select the low noise type.**
  The open magnetic circuit type core like a drum type may generate noise in peripheral circuit due to the magnetic flux passing outside of coil.
  It is recommended to use the Coils of closed magnetic circuit type core such as toroidal type, EI type and EE type.

12.1.2. Input Capacitor, C_{IN}

The input capacitor, C_{IN}, shows C1 and C2.

C_{IN} is the bypass capacitor of input circuit. It supplies the current of short pulses to the regulator during switching and compensates the input voltage drop. Thus, C_{IN} should be placed as close the IC as possible. Even if the rectifying capacitor of an AC/DC convertor circuit is in input circuit, C_{IN} is required when the rectifying capacitor is not placed near the IC.

Since large ripple current flows through C_{IN}, C_{IN} must be used the capacitor for the switching regulator, which is for high frequency and has low impedance characteristics. The selection points of C_{IN} are as follows:

- Fulfill the breakdown voltage rating.
- Fulfill sufficient allowable ripple current rating.

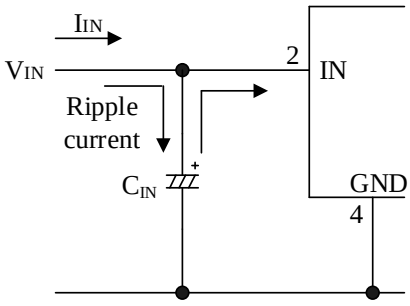


Figure 12-4. Current Flow of Input Capacitor

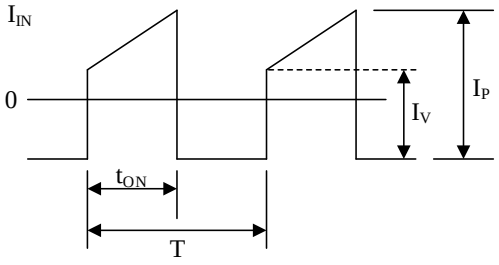


Figure 12-5. Current Waveform of Input Capacitor

If the C_{IN} voltage and ripple current is over the rating of the breakdown voltage and the allowable ripple current, or you does not consider derating for these rating, the following problem may be occurred. Thus, you must consider derating for breakdown voltage and the allowable ripple current.

- The capacitor life time short (burst, capacitance decreasing, equivalent impedance increasing, etc.)
- The unstable switching operation of the IC.

The ripple current of C_{IN} increases depending on the load current. The effective value of the ripple current, $I_{INR(RMS)}$, is calculated by Equation (11).

$$I_{INR(RMS)} \approx 1.2 \times \frac{V_O}{V_{IN}} \times I_O \quad (11)$$

If V_{IN} is 20 V, I_O is 3 A, V_O is 5 V,

$$I_{INR(RMS)} \approx 1.2 \times \frac{5\ (V)}{20\ (V)} \times 3\ (A) = 0.9\ (A)$$

In the case, you must select the capacitor that the allowable ripple current is more than 0.9 A.

12.1.3. Output Capacitor, C_{OUT}

The output capacitor, C_{OUT}, shows C4 and C5.

In the current control method, the feedback loop which detects the inductor current is added to the voltage control method. The stable operation is achieved without considering the effect of the secondary delay factor of LC filter.

Thus, the capacitance of the capacitor of the LC filter can be reduced. The IC can achieve the stable operation using the low ESR capacitor (ceramic capacitor).

The C_{OUT} is the rectifying capacitor of switching output, and composes the LC low-pass filter with choke coil, L1.

The current that is same of the ripple current of choke coil, ΔI_L, flows through C_{OUT}. Therefore, you must consider derating for breakdown voltage and the allowable ripple current (See Section 12.1.2 Input Capacitor).

Since large ripple current flows through C_{OUT}, C_{OUT} must be used the capacitor for the switching regulator, which is for high frequency and has low impedance characteristics.

If the impedance of C_{OUT} is high, the IC may be occurred unstable switching operation in low temperature environment.

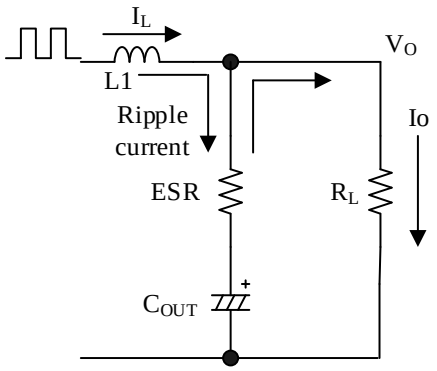


Figure 12-6. Current Flow of Output Capacitor

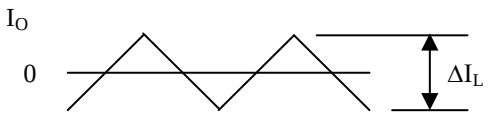


Figure 12-7. Current Waveform of Output Capacitor

The ripple current of C_{OUT} is same with the ripple current of the choke coil, and does not depend on the load current. Thus, the effective value of the ripple current, $I_{OR(RMS)}$, is calculated by Equation (12).

$$I_{OR(RMS)} = \frac{\Delta I_L}{2\sqrt{3}} \quad (12)$$

If ΔI_L is 0.5 A,

$$I_{OR(RMS)} = \frac{0.5\ (A)}{2\sqrt{3}} \approx 0.14\ (A)$$

In the case, you must select the capacitor that the allowable ripple current is more than 0.14 A.

The output ripple voltage of the IC, V_{RIP}, is calculated by Equation (13).

$$V_{RIP} = \Delta I_L \times C_{OUT}ESR \quad (13)$$

Where, ΔI_L is the ripple current of the choke coil (same of the ripple current of C_{OUT}), and $C_{OUT}ESR$ is the equivalent series resistance (ESR) of C_{OUT}.

From Equation (13), you should set the low ESR capacitor in order to reduce the output ripple voltage.

In same family of the electrolytic capacitor, the larger capacitance in same the rating voltage, or the higher rating voltage (the larger package size) in same capacitance is, the lower the ESR generally becomes.

If ΔI_L is 0.5 A, V_{RIP} is 40 mV,

$$C_{OUT}ESR = \frac{V_{RIP}}{\Delta I_L} = \frac{40(mV)}{0.5\ (A)} = 80\ (m\Omega) \quad (14)$$

In the case, you must select the capacitor that the ESR is less than 80 mΩ

In addition, the ESR depends on temperature, and generally increases in low temperature. Thus, you should check the ESR at the actual used temperature. The ESR characteristic is shown in each capacitor maker.

12.1.4. Freewheel Diode, D1

Flywheel diode, D1, is for discharging energy that is charged choke coil in off-status.

External flywheel diode, D1, improves efficiency, and must be used a Schottky-barrier diode. If the fast recovery diode is used, the IC may be damaged by the reverse voltage that is caused by the surge at turn-on or the forward voltage in on-status.

Since the output voltage of the SW pin (3 pin) is nearly same with input voltage, the reverse breakdown voltage of D1 is required more than the input voltage.

You must not use ferrite beads for the flywheel diode.

12.1.5. Output Voltage, V_O, and Output Capacitor

The output capacitor determines according to the output voltage V_O. In each voltage, Table 12-1 shows the capacitance that the IC can operate stable. The values are reference. The ESR of the electrolytic capacitor is about 100 mΩ. See Section 12.1.1 about the inductance, L, setting.

Table 12-1. Output Voltage, V_O, vs. Output Capacitor (NR111E: 350 kHz)

V_O (V)	Output Capacitor (µF)	
	Ceramic Capacitor	Electrolytic Capacitor (ESR ≈ 100 mΩ)
1.2	22～100	4.7～330
1.8		4.7～470
3.3	10～68	4.7～330
5	4.7～47	4.7～220
9		
12		
16		

12.2. Allowable Power Dissipation

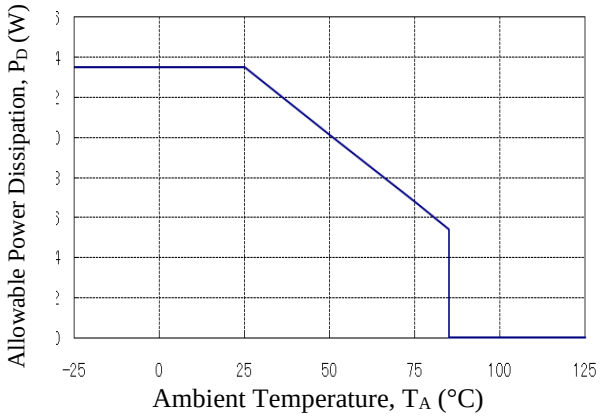
The power dissipation of the IC must be within the allowable power dissipation shown in Figure 12-8, and is calculated by Equation Figure 12-8.

$$P = V_O \times I_O \times \left(\frac{100}{\eta x} - 1\right) - V_F \times I_O \times \left(1 - \frac{V_O}{V_{IN}}\right) \quad (15)$$

where,
V_O is output voltage,
V_{IN} is Input voltage,
I_O is output curent,
V_F is diode forward voltage, and
ηx is efficiency (%).

Since the efficiency determines from the input voltage and output current, it shall be obtained from the efficiency curve and substituted in percent.

The heat release setting of the freewheel diode is required separately.



NOTES

- Glass-epoxy board, 30 mm × 30 mm
- Copper area, 25 mm × 25 mm
- The power dissipation is calculated at the junction temperature 125 °C.

Figure 12-8. Allowable Power Dissipation Curve

12.2.1. Power Supply Stability

The phase characteristics of a chopper type regulator are the synthesis of follows.

The internal phase characteristics of a regulator IC, the output capacitor, and the load resistance.

Internal phase characteristics of a regulator IC are generally determined by the delay time of control block and the phase characteristics of the output error amplifier. Therefore, the phase delay due to the delay time of the control block rarely causes problems in actual use.

The IC has phase compensation for output error amplifier. See Section 12.1.5 about the output voltage setting and the output current setting for stable operation.

12.2.2. Spike Noise Reduction

This section shows how to reduce spike noises.

Extra attentions should be paid when you measure spike noises using an oscilloscope.

The ground lead of a probe should be as short as possible, and should be connected to root of output capacitor. When the ground lead is long, the noises may be measured larger than actual noises because the ground lead becomes an antenna.

- **Add a resistance to the BS pin in series.**
  When the resister, R3, is added between the BS pin and SW pin as shown in Figure 12-9, the turn-on switching speed of the internal power MOSFET becomes slow. The spike noises is reduced according to decreasing switching speed.
  The maximum value of R3 is 22 Ω.

If R3 is set too large, the following event may be occured.
Start-up failure.
The IC is damaged by self-heating due to decreasing the gate voltage of internal power MOSFET.

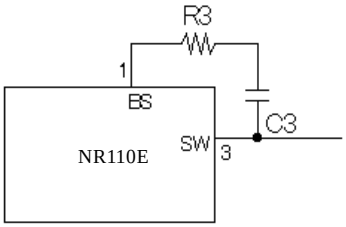


Figure 12-9. BS pin peripheral circuit

- **Add a snubber circuit.**
  When an RC snubber (a resistor and a capacitor) is added to the SW pin as shown in Figure 12-10, the spike noises are reduced because the slopes of output waveform and the recovery current waveform of the diode become shallow.
  Note that the efficiency is decreased as the swiching loss of the internal power MOSFET increases.

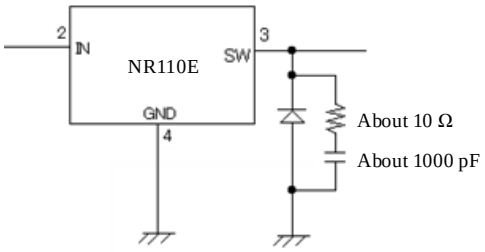


Figure 12-10. SW pin peripheral circuit

- Note when you add bead cores
  Bead cores incruding ferrite beads must not be used in the broken line in Figure 12-11.
  When you layouts the PCB trace of the switching regurator, the parasitic inductance of PCB trace should be as small as possible. If bead cores are added, the the inductance of the bead cores is added to the parasitic inductance of PCB trace. It may causes the malfunction or break of the IC by the unstable status including negative potential grounding due to surge voltage.
  The noise reduction method should be chosen from above method (add the BS pin resistor or the snubber ciecuit).

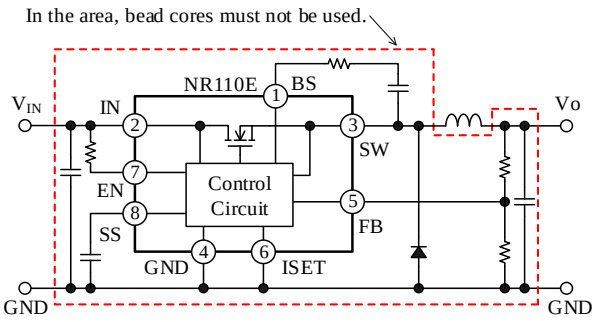


Figure 12-11. Note when you add bead cores

12.2.3. Reverse Bias Condition

When the IN pin voltage becomes higher than the SW pin voltage (battery charger application, etc.), the diode for reverse bias protection must be connected between the IN pin and SW pin as shown in Figure 12-12.

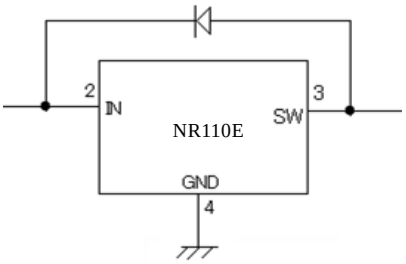


Figure 12-12. When the IN pin voltage becomes higher than the SW pin voltage

12.3. Pattern Layout

12.3.1. Large Current Trace

Since large current flows through the bold line in Figure 12-13, these PCB traces must be as wide and small loop as possible.

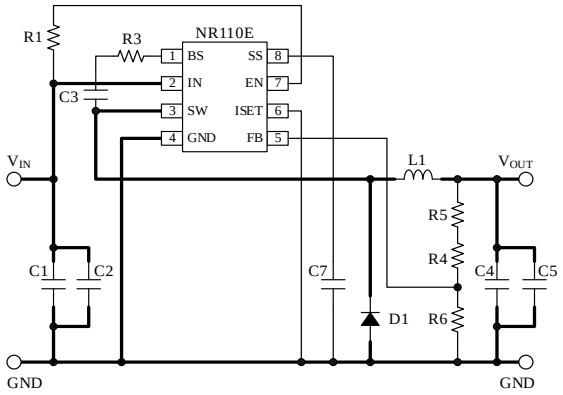


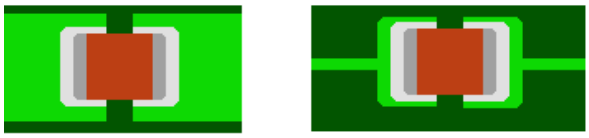
Figure 12-13. Large Current Line

12.3.2. Input and Output Capacitor

Input capacitors (C1 and C2) and output capacitors (C4 and C5) are placed as close the IC as possible.

Even if the rectifying capacitor of an AC/DC convertor circuit is in input circuit, input capacitors are required when the rectifying capacitor is not placed near the IC.

The traces of these capacitors are drawn wide (see Figure 12-14-(a), Proper Trace)



(a) Proper Trace (b) Improper Trace

Figure 12-14. Trace Example of Capacitors

12.3.3. FB Pin Setting (Output Voltage Setting)

The FB pin detects the feedback signal to control the output voltage, and should be placed as close the output capacitor as possible. If the FB pin is far from the output capacitor, the unstable operation may be occurred by the regulation decreasing and the switching ripple increasing.

The output voltage is set by the resisters connected to the FB pin (R4, R5 and R6). The minimum current flowing through the FB pin, I_{FB}, should be set about 0.2 mA. The maximum value of I_{FB} should be set considering about the efficiency.

The output voltage, V_O, and the value of R4, R5 and R6 are calculated by the following equations.

$$I_{FB} = \frac{V_{FB}}{R6} \tag{16}$$

where, V_{FB} is 0.8 V ± 2%.

$$R4 + R5 = \frac{V_O - V_{FB}}{I_{FB}} = \frac{V_O - 0.8}{0.2 \times 10^{-3}}\ (\Omega) \tag{17}$$

$$R6 = \frac{V_{FB}}{I_{FB}} = \frac{0.8}{0.2 \times 10^{-3}} \approx 3.9\ (k\Omega) \tag{18}$$

$$V_O = (R4 + R5) \times \frac{V_{FB}}{R6} + V_{FB} \tag{19}$$

If the output voltage is set to 0.8 V that is same voltage with V_{FB}, R6 should be connected to operate stable.

The relationship between input voltage and output voltage is determined by the on-time of the SW pin. The on-time is recommended to set to more than 200 ns.

The traces connected to the FB pin and the R4, R5, R6 must not be placed in parallel with the trace connected to the freewheel diode, because switching noise affects to the feedback detection voltage, and may occur unstable operations.

Especially, the trace between FB pin and R6 must be as short as possible.

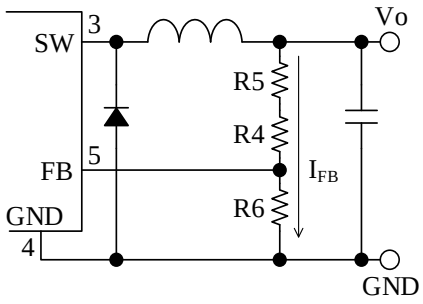
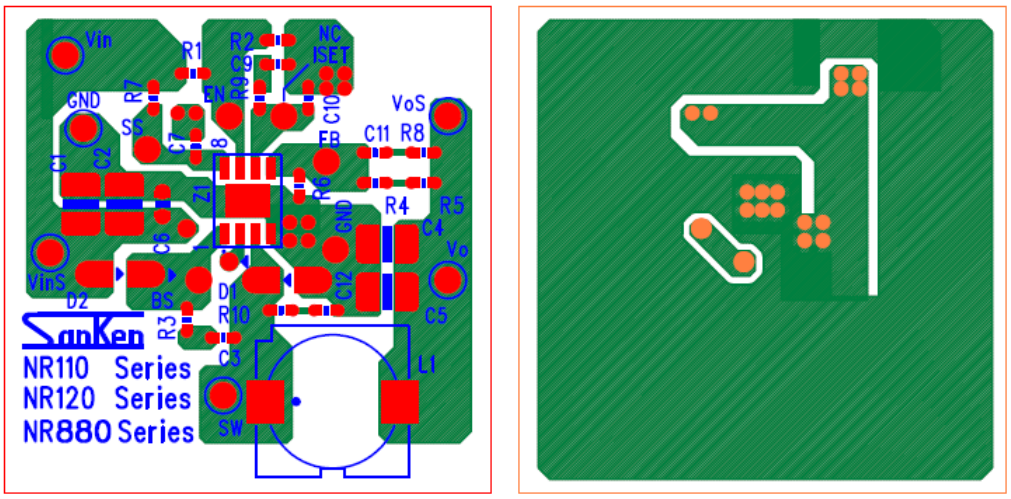


Figure 12-15. FB pin peripheral circuit

13. Pattern Layout Example

Ground trace must be connected as short as possible to the GND pin at single point grounding. The exposed pad on the back side of the package is connected to the ground trace. The larger copper plane can improve the heat release capability.

Note that the pattern layout example only uses the parts illustrated in the circuit diagram below because this board is used for some other products.



(a) Front Side (Components is mounted) (b) Back Side (Ground pattern)

Figure 13-1. Pattern Layout Example (PCB size: 40 mm × 40 mm)

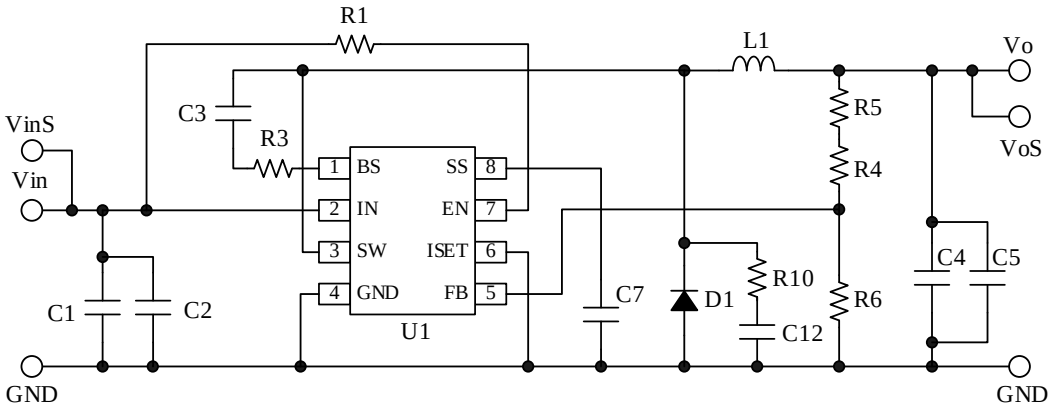


Figure 13-2. Pattern Layout Example Circuit

Table 13-1. Bill of Materials

Symbol	Part	Reference Value	Remarks
C1	Chip ceramic capacitor	10 µF, 50 V, 3216	
C2	Chip ceramic capacitor	10 µF, 50 V, 3216	
C3	Chip ceramic capacitor	0.1 µF, 50 V, 1608	
C4	Chip ceramic capacitor	22 µF, 25 V, 3225	低 ESR タイプ
C5	Chip ceramic capacitor	22 µF, 25 V, 3225	低 ESR タイプ
C7	Chip ceramic capacitor	0.1 µF, 50 V, 1608	
C12	Chip ceramic capacitor	Open	Adjustment capacitor
D1	Schottky diode	40 V, 5.0 A	SJPW-T4 (Sanken)
L1	Inductor	68 µH	SLF12575T-6R8N5R9-PF (TDK)
R1	Chip resistor	510 kΩ, 0.1 W, 1608	
R3	Chip resistor	22 Ω, 0.1 W, 1608	
R4	Chip resistor	10 kΩ, 0.1 W, 1608	
R5	Chip resistor	2.5 kΩ, 0.1 W, 1608	
R6	Chip resistor	2.2 kΩ, 0.1 W, 1608	
R10	Chip resistor	Open	Adjustment resistor
U1	Buck converter	eSOIC8	NR111E (Sanken)

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