

**GENERAL DESCRIPTION**

The F2933 is a high reliability, low insertion loss, 50 Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50 MHz to 8000 MHz. In addition to providing low insertion loss, the F2933 also delivers high linearity and high isolation performance while providing a 50 Ω termination to the unused RF input port.

The F2933 uses a single positive supply voltage of 2.7 V to 5.5 V supporting three states using either 3.3 V or 1.8 V control logic.

**COMPETITIVE ADVANTAGE**

The F2933 provides the following advantages

- ✓ Insertion Loss = 0.79 dB\*
  - ✓ RFX to RFC Isolation = 67 dB\*
  - ✓ IIP3 = +64 dBm\*
  - ✓ Active Port Operating Power Handling = 34 dBm
  - ✓ Term Port Operating Power Handling = 27 dBm
  - ✓ Extended Temperature Range = -40°C to 105°C
- \* 2 GHz

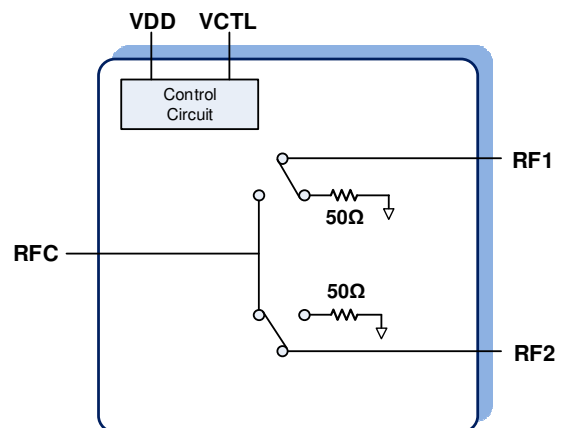
**APPLICATIONS**

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Test / ATE Equipment

**FEATURES**

- High Isolation:
  - 70 dB @ 1 GHz
  - 67 dB @ 2 GHz
  - 65 dB @ 3 GHz
  - 66 dB @ 4 GHz
- High Linearity:
  - IIP2 of 111 dBm
  - IIP3 of 64 dBm @ 2 GHz
- Wide Single Positive Supply Voltage Range
- 3.3 V and 1.8 V compatible control logic
- Operating temperature -40 °C to +105 °C
- 4 mm x 4 mm 16 pin QFN package

**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

**F2933NBGP8**

↗ Tape & Reel

↓ Green

## ABSOLUTE MAXIMUM RATINGS

Parameter / Condition		Symbol	Min	Max	Unit
V <sub>DD</sub> to GND		V <sub>DD</sub>	-0.3	+6.0	V
VCTL to GND		V <sub>logic</sub>	-0.3	Lower of 3.6, V <sub>DD</sub> +0.3	V
RF1, RF2, RFC to GND		V <sub>RF</sub>	-0.3	+0.3	V
RF Input Power <sup>1</sup>	RF1 or RF2 as an input (Connected to RFC)	P <sub>RF12</sub>		36	dBm
	RFC as an input (Connected to RF1 or RF2)	P <sub>RF12</sub>		36	
	RF1 or RF2 as input (Terminated states)	P <sub>RF12_TERM</sub>		30	
Maximum Junction Temperature		T <sub>Jmax</sub>		+140	°C
Storage Temperature Range		T <sub>ST</sub>	-65	+150	°C
Lead Temperature (soldering, 10s)		T <sub>LEAD</sub>		+260	°C
ESD Voltage– HBM (Per JESD22-A114)		V <sub>ESDHBM</sub>		Class 2 (2000V)	
ESD Voltage – CDM (Per JESD22-C101)		V <sub>ESDCDM</sub>		Class C3 (1000V)	

Note 1: V<sub>DD</sub> = 2.7 V to 5.5 V, 50 MHz ≤ F<sub>RF</sub> ≤ 8000 MHz, T<sub>c</sub> = 105 °C, Z<sub>s</sub> = Z<sub>L</sub> = 50 ohms.

Note 2: Each port.

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ <sub>JA</sub> (Junction – Ambient)	60 °C/W
θ <sub>JC</sub> (Junction – Case) The Case is defined as the exposed paddle	3.9 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

**F2933 RECOMMENDED OPERATING CONDITIONS**

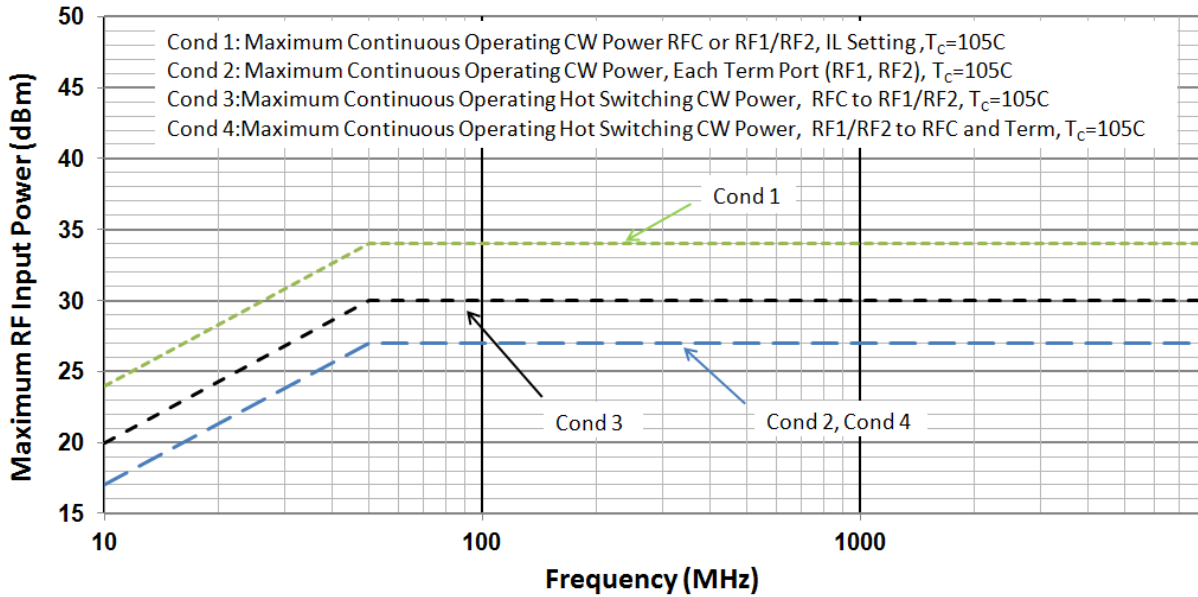
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	$V_{DD}$		2.7		5.5	V
Operating Temp Range	$T_{CASE}$	Exposed Paddle Temperature	-40		+105	$^{\circ}C$
RF Frequency Range	$F_{RF}$		50		8000	MHz
RF Continuous Input CW Power (Non-Switched) <sup>1</sup>	$P_{RF}$	RFC connected to RF1 or RF2 <sup>2</sup>	$T_C = 85\ ^{\circ}C$		34	dBm
			$T_C = 105\ ^{\circ}C$		34	
		RF1/ RF2 Input Terminated State <sup>3,4</sup>	$T_C = 85\ ^{\circ}C$		27	
			$T_C = 105\ ^{\circ}C$		27	
RF Continuous Input Power (RF Hot Switching CW) <sup>1</sup>	$P_{RFSW}$	RFC Input, switching between RF1 and RF2	$T_C = 85\ ^{\circ}C$		30	dBm
			$T_C = 105\ ^{\circ}C$		30	
		RF1 or RF2 as input, switched between RFC and Term.	$T_C = 85\ ^{\circ}C$		27	
			$T_C = 105\ ^{\circ}C$		27	
RF1/2 Port Impedance	$Z_{RFx}$			50		$\Omega$
RFC Port Impedance	$Z_{RFC}$			50		$\Omega$

Note 1: Levels based on:  $V_{DD} = 3.1\text{ V to }5.5\text{ V}$ ,  $50\text{ MHz} \leq F_{RF} \leq 8000\text{ MHz}$ ,  $Z_S = Z_L = 50\text{ ohms}$ . See Figure 1 for power handling derating vs. RF frequency.

Note 2: Input could be: RFC, RF1, or RF2 (applied to only one input).

Note 3: Any RF1 / RF2 termination state. Power level specified is for each port.

Note 4: Power level specified is for each port.



**Figure 1: Maximum RF Input Operating Power vs. RF Frequency**

## F2933 SPECIFICATION

Typical Application Circuit,  $V_{DD} = 5.0\text{ V}$ ,  $T_C = +25\text{ }^\circ\text{C}$ ,  $F_{RF} = 2000\text{ MHz}$ , Driven Port = RF1 or RF2, input power = 10 dBm,  $Z_S = Z_L = 50\text{ ohms}$ , PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Input High Threshold	$V_{IH}$		<b>1.1</b>		<b>Lower of (3.6, <math>V_{DD}</math>)</b>	V
Logic Input Low Threshold	$V_{IL}$		-0.3		<b>0.6</b>	V
Logic Current	$I_{IH}, I_{IL}$	For each control pin	<b>-1</b>		<b>+1</b>	$\mu\text{A}$
DC Current	$I_{DD}$	$V_{DD} = 3.3\text{ V}$		200	<b>260<sup>1</sup></b>	$\mu\text{A}$
		$V_{DD} = 5.0\text{ V}$		260	<b>325</b>	
Insertion Loss RFC to RF1 / RF2	IL	50 MHz		0.68		dB
		1 GHz		0.73		
		2 GHz		0.79	<b>1.1</b>	
		3 GHz		0.82		
		4 GHz		0.93		
		6 GHz		1.06		
		8 GHz		1.6		
Isolation RFC to RF1 / RF2	ISOC	50 MHz	<b>77<sup>2</sup></b>	79		dB
		1 GHz	68	70		
		2 GHz	63	67		
		3 GHz	62	65		
		4 GHz	60	66		
		6 GHz	53	63		
		8 GHz		45		
Isolation RF1 to RF2	ISOX	50 MHz		86		dB
		1 GHz		64		
		2 GHz		58		
		3 GHz		54		
		4 GHz		51		
		6 GHz		45		
		8 GHz		37		
Return Loss RFC, RF1, RF2	$RF_{RL}$	50 MHz		25		dB
		1 GHz		25		
		2 GHz		23		
		3 GHz		24		
		4 GHz		20		
		6 GHz		18		
		8 GHz		14		
Return Loss RF1, RF2 Terminated	$RF_{RLTERM}$	50 MHz		40		dB
		1 GHz		31		
		2 GHz		35		
		3 GHz		23		
		4 GHz		17		
		6 GHz		19		
		8 GHz		22		

Note 1: Items in min/max columns in **bold italics** are Guaranteed by Test.

Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

## F2933 SPECIFICATION (CONT.)

Typical Application Circuit,  $V_{DD} = 5.0\text{ V}$ ,  $T_C = +25\text{ }^\circ\text{C}$ ,  $F_{RF} = 2000\text{ MHz}$ , Driven Port = RF1 or RF2, input power = 10 dBm,  $Z_S = Z_L = 50\text{ ohms}$ , PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input 1dB Compression <sup>3</sup>	ICP <sub>1dB</sub>	50 MHz		33.2		dBm
		1 GHz		35.5		
		2 GHz		36.5		
		3 GHz		36.1		
		4 GHz		35.3		
Input 0.1dB Compression <sup>3</sup>	ICP <sub>0.1dB</sub>	$V_{DD} = 5.0\text{ V}$	50 MHz		30.4	dBm
			2 GHz		32.3	
			3 GHz		32.6	
			4 GHz		32.2	
	$V_{DD} = 3.1\text{ V}$	50 MHz		30.1		
		2 GHz		32.1		
		3 GHz		32.6		
		4 GHz		32.1		
Input IP2	IIP2	$F_{RF1} = 2000\text{ MHz}$ , $F_{RF2} = 1990\text{ MHz}$ $RF_{IN} = RF1\text{ or }RF2$ $P_{IN} = +20\text{ dBm / tone}$ $F_{IP2} = F_{RF1} + F_{RF2}$		111		dBm
Input IP3	IIP3	RF Input = RF1 or RF2 $P_{IN} = +15\text{ dBm/tone}$ $\Delta F = 1\text{ MHz}$	50 MHz		58	dBm
			1 GHz		64	
			2 GHz		64	
			2.5 GHz		63.4	
			4 GHz		63.6	
Non-RF Driven Spurious <sup>4</sup>		At any RF port when externally terminated into 50 $\Omega$		-114		dBm
Switching Time <sup>5</sup>	T <sub>SW</sub>	50% control to 90% RF		210		ns
		50% control to 10% RF		115		
		50% control to RF settled to within +/- 0.1 dB of I.L. value		225		
Maximum Switching Rate <sup>6</sup>	SW <sub>RATE</sub>			25		kHz
Maximum Video Feed-through on RF Ports	VID <sub>FT</sub>	5 MHz to 1000 MHz Measured with 20 ns risetime, 0 to 3.3 V control pulse		12		mV <sub>pp</sub>

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.

Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3: The input 1 dB compression point is a linearity figure of merit. Refer to the Recommended Operating Conditions section for the specified maximum operating power levels.

Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 5.2 MHz.

Note 5:  $F_{RF} = 1\text{ GHz}$ .

Note 6: Minimum time required between switching of states = 1/ (Maximum Switching Rate).

## Control Mode

**Table 1 - Switch Control Truth Table**

VCTL	RFC to RF1	RFC to RF2
0	ON	OFF
1	OFF	ON

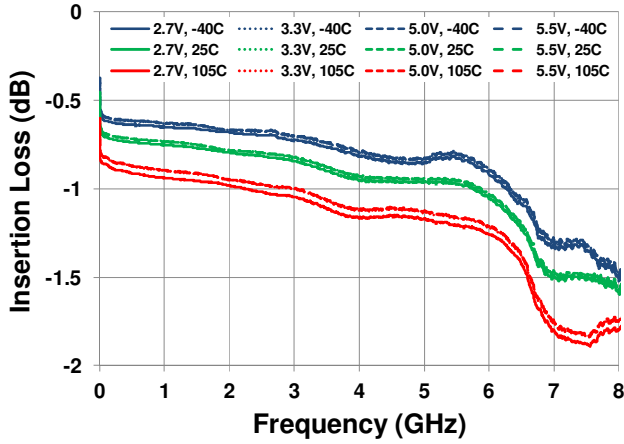
## TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

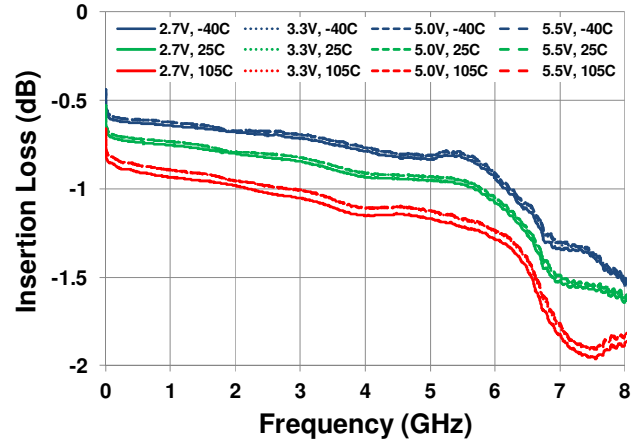
- **$V_{DD} = 3.3 \text{ V}$**
- **$T_C = +25 \text{ }^\circ\text{C}$  ( $T_C = \text{Temperature of Exposed Paddle}$ )**
- **$F_{RF} = 2000 \text{ MHz}$**
- **$Z_S = Z_L = 50 \text{ } \Omega$**
- **$P_{IN} = +10 \text{ dBm}$  for all small signal tests.**
- **$P_{IN} = +15 \text{ dBm/}$ tone applied to RF1 or RF2 port for two tone linearity tests.**
- **Two tone frequency spacing = 1 MHz.**
- **RF1 or RF2 is the driven RF port and RFC is the output port.**
- **All unused RF ports terminated into 50 ohms.**
- **For Insertion Loss and Isolation plots, RF trace and connector losses are de-embedded (see EVKIT Board and Connector loss plot).**
- **Plots for Isolation and Insertion Loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.**

TYPICAL OPERATING CONDITIONS (- 1 -)

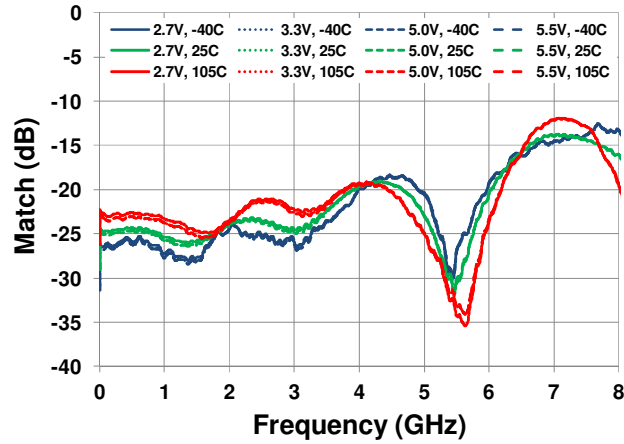
RF1 to RFC Insertion Loss



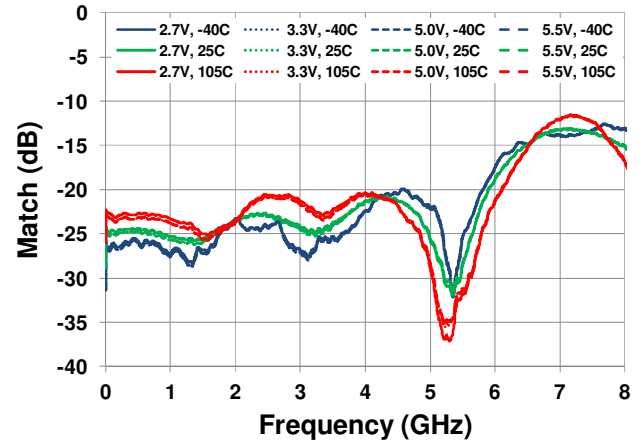
RF2 to RFC Insertion Loss



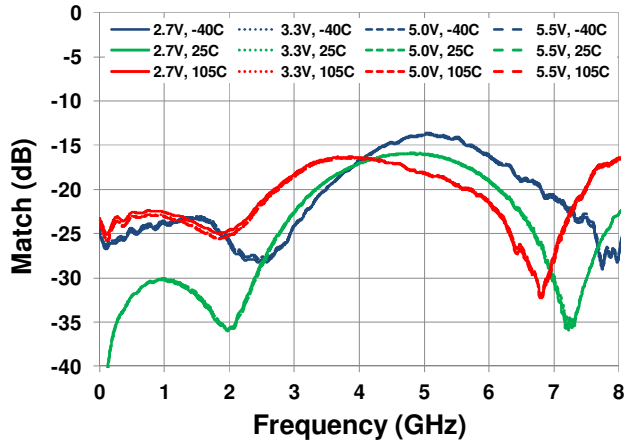
RF1 Port Match [On State]



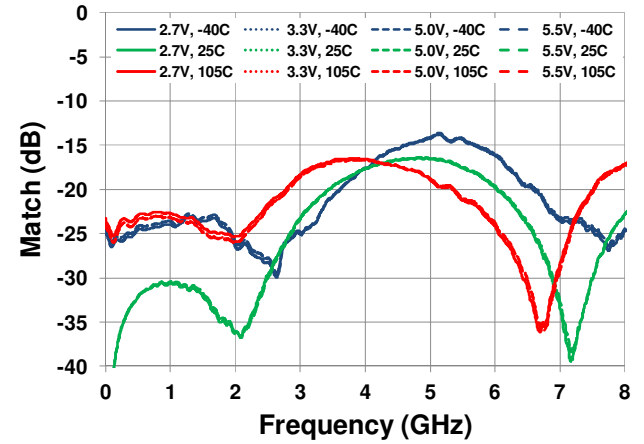
RF2 Port Match [On State]



RF1 Port Match [Terminated State]

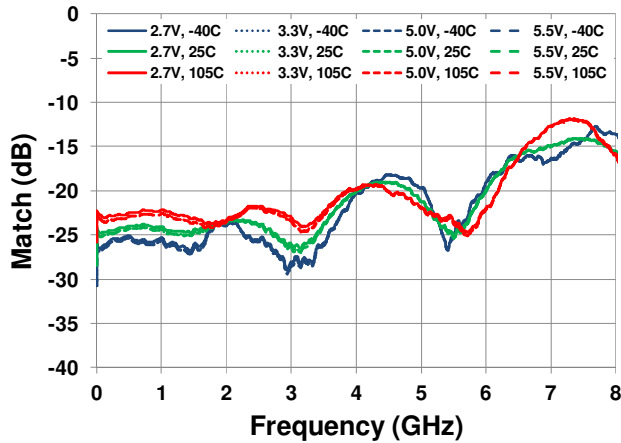


RF2 Port Match [Terminated State]

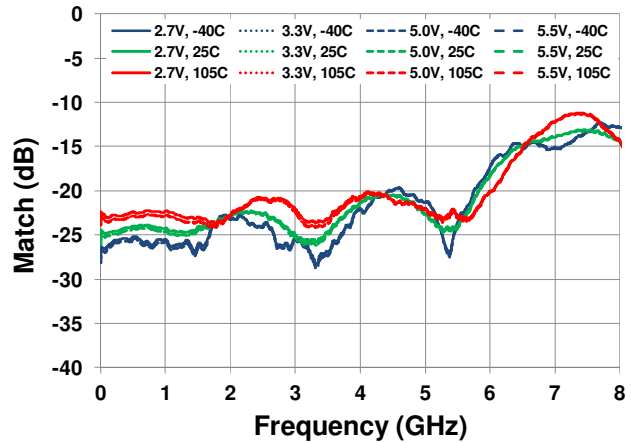


TYPICAL OPERATING CONDITIONS (- 2 -)

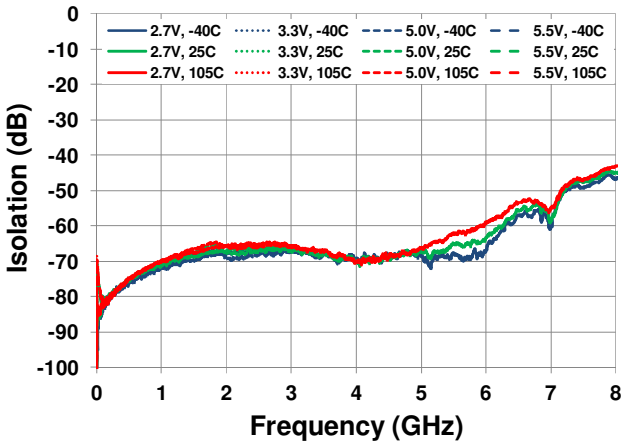
RFC Port Match [RF1 On State]



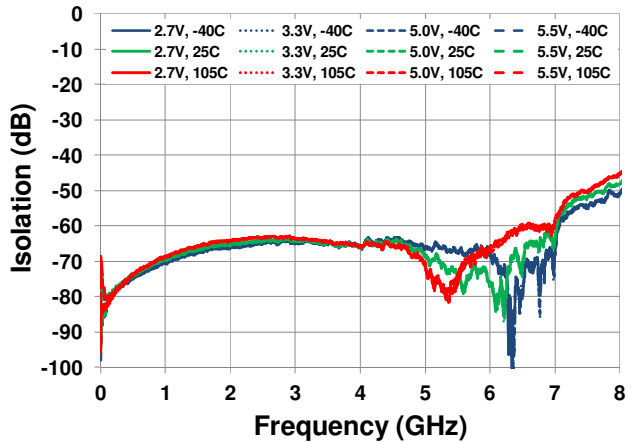
RFC Port Match [RF2 On State]



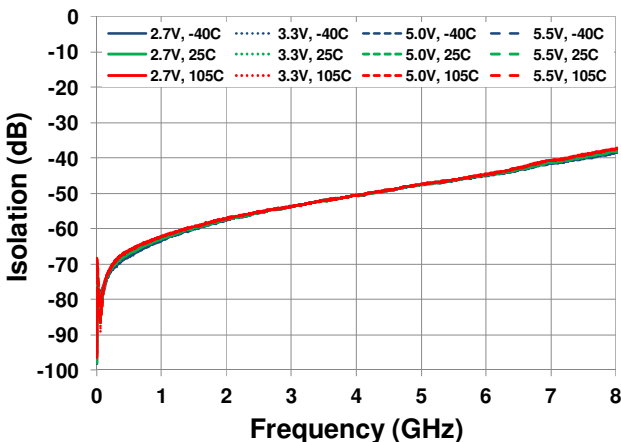
RF1 to RFC Isolation [RF2 On State]



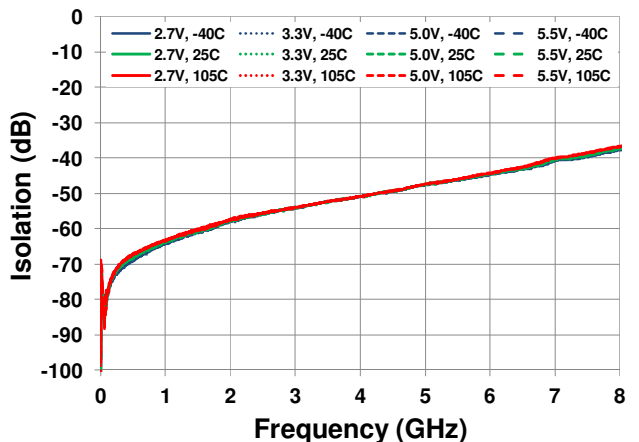
RF2 to RFC Isolation [RF1 On State]



RF1 to RF2 Isolation [RF1 On State]



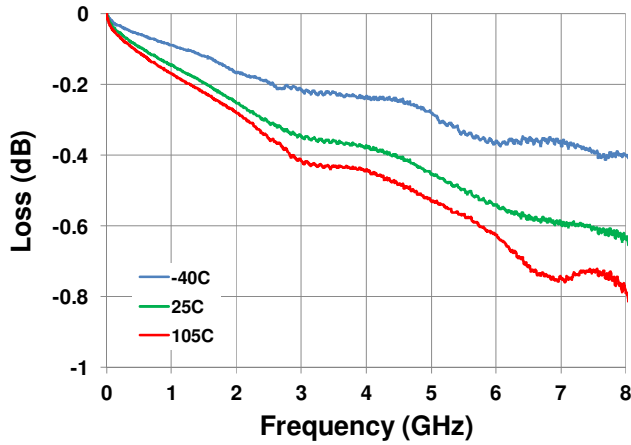
RF2 to RF1 Isolation [RF2 On State]



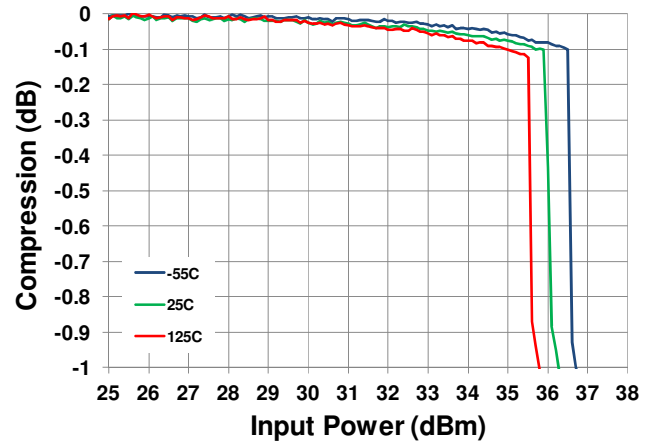


TYPICAL OPERATING CONDITIONS (- 3 -)

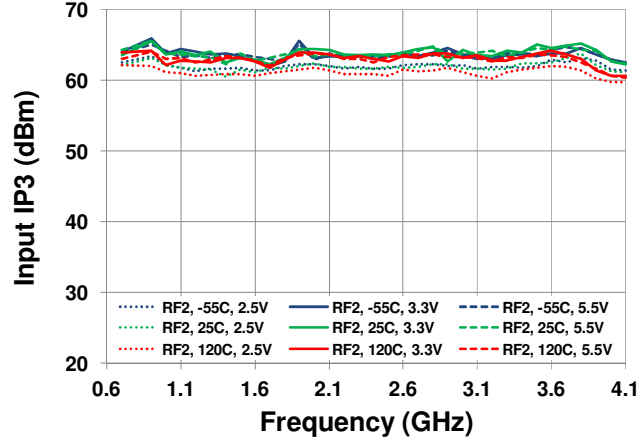
**EVKIT PCB and Connector Thru Loss**



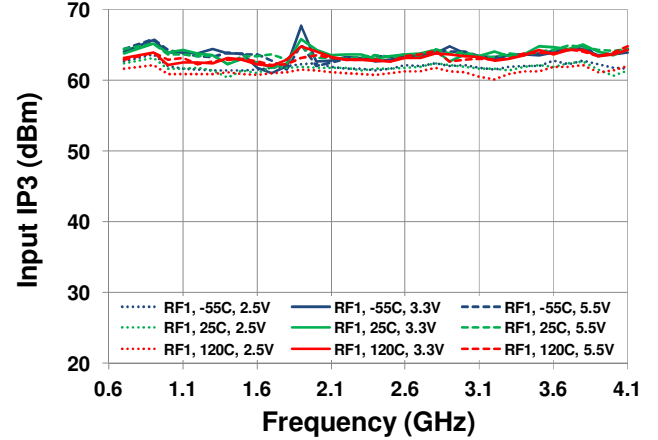
**Input P1dB [1GHz] [T<sub>c</sub> operating = -40C to 105C]**



**Input IP3 RF1 Port [T<sub>c</sub> operating = -40C to 105C]**



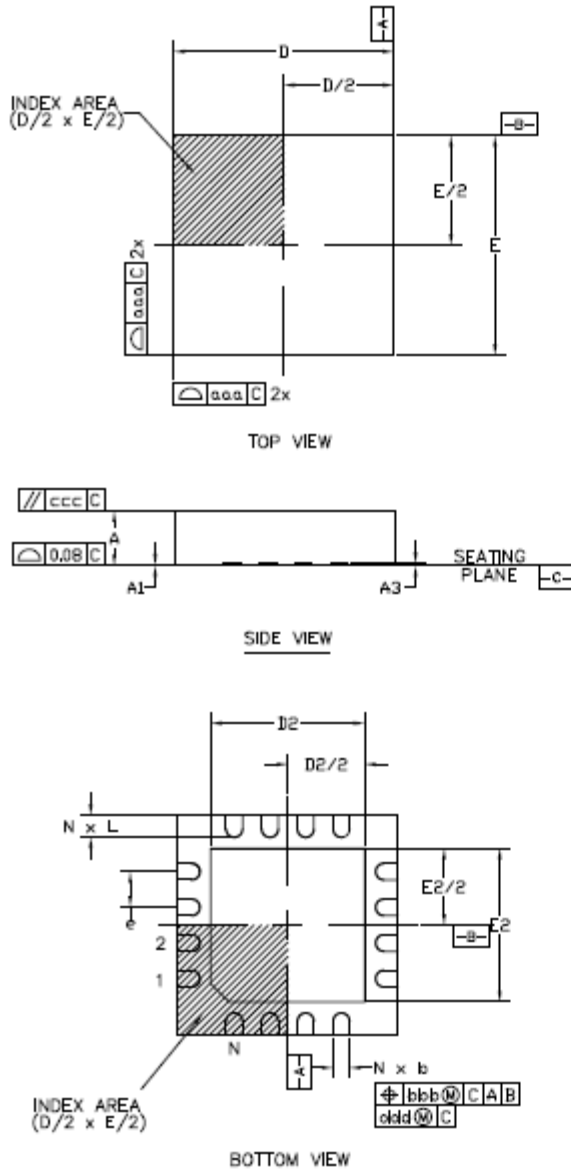
**Input IP3 RF2 Port [T<sub>c</sub> operating = -40C to 105C]**



**PACKAGE DRAWING**

(4 mm x 4 mm 16-pin QFN), NBG16

**Note: The F2933 uses EPAD Option P2 and Lead Option Z2**



SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.02 ref		
b	0.25	0.30	0.35
D	4.0		
E	4.0		
e	0.65		
N	16		
ND	4		
NE	4		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		

EPAD OPTION:

	P2		
	MIN	NOM	MAX
D2	2.55	2.70	2.80
E2	2.55	2.70	2.80

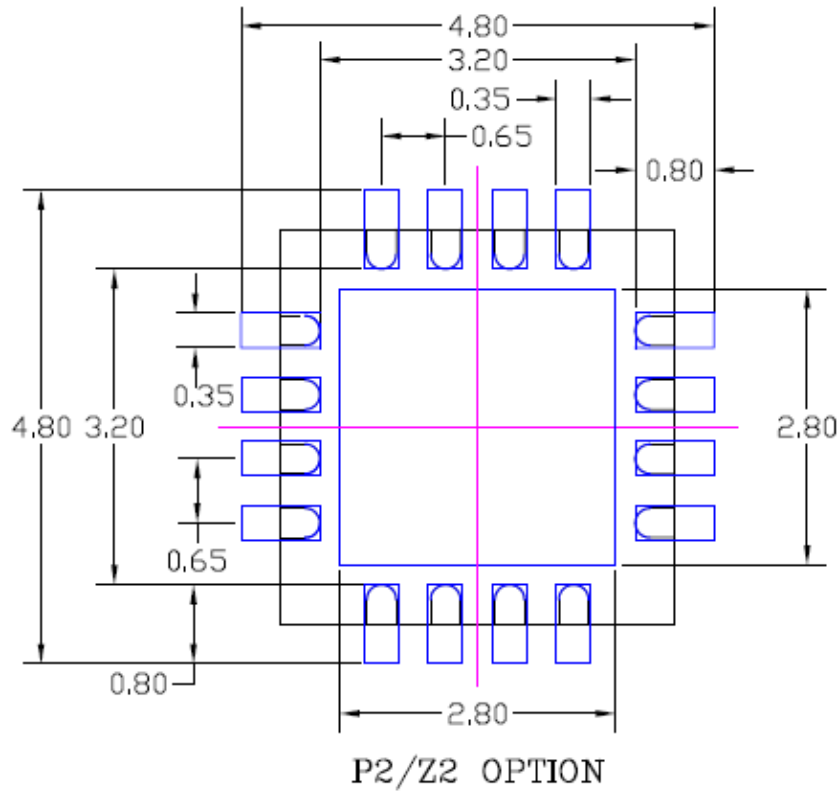
LEAD OPTION:

	Z2		
	MIN	NOM	MAX
L	0.30	0.40	0.50

NOTES:

1. All dimensions in mm.
2. The dimension and tolerancing meet ASME Y-14.5M-1994.

LAND PATTERN DIMENSION

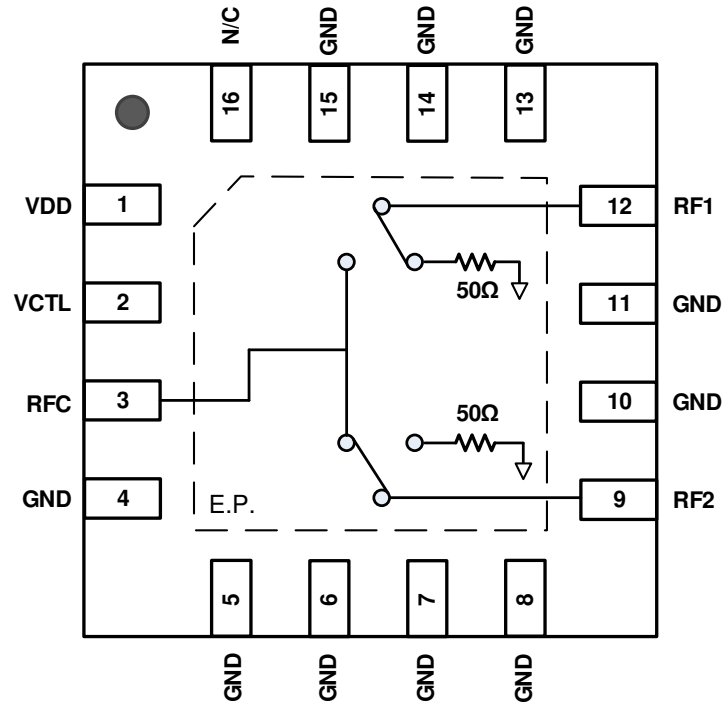


RECOMMENDED LAND PATTERN DIMENSION

NOTE:

- 1) ALL dimensions are in mm, Angles in degrees.
- 2) Top down view, as view on PCB.
- 3) Land Pattern in BLUE.NSMD Land Pattern Assumed
- 4) Land Pattern Recommendation as per IPC-7351B generic requirement for surface mount design and Land Pattern.

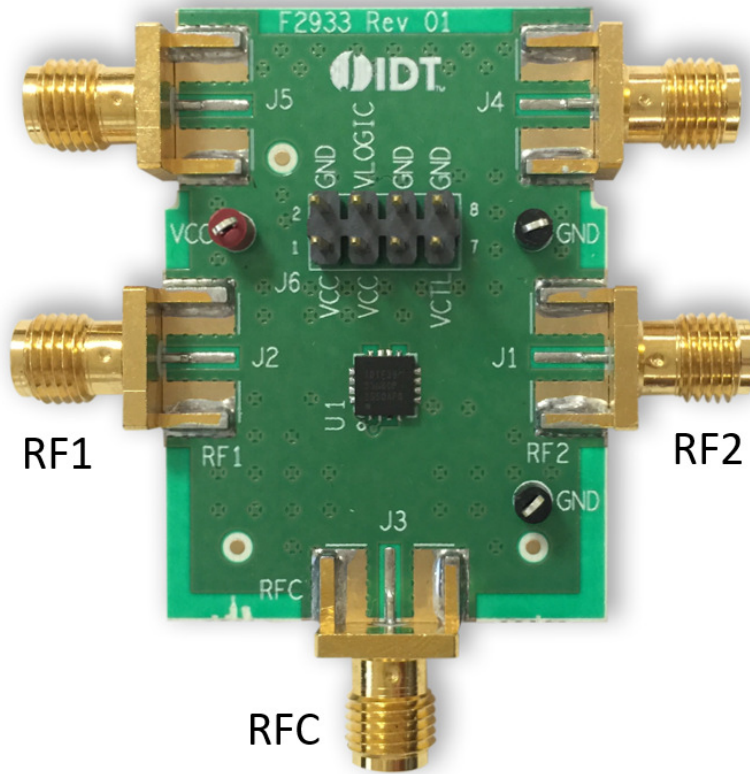
PIN DIAGRAM



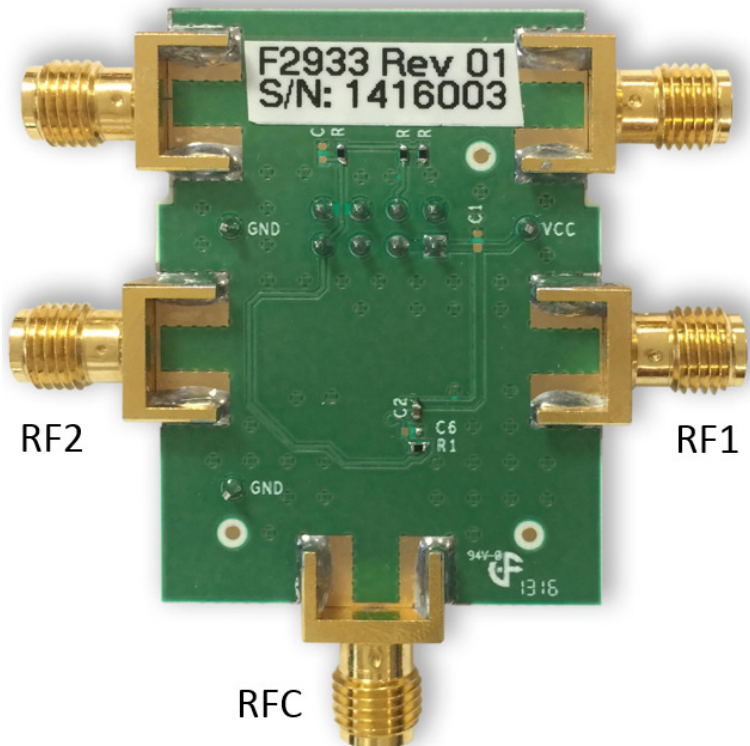
PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VDD	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
2	VCTL	Logic control pin. See Table 1.
3	RFC	RF Common Port. Matched to 50 Ω when one of the 2 RF ports is selected. If this pin is not 0 V DC, then an external coupling capacitor must be used.
4, 5, 6, 7, 8, 10, 11, 13, 14, 15, 16	GND	Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible.
9	RF2	RF2 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used.
12	RF1	RF1 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used.
17	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

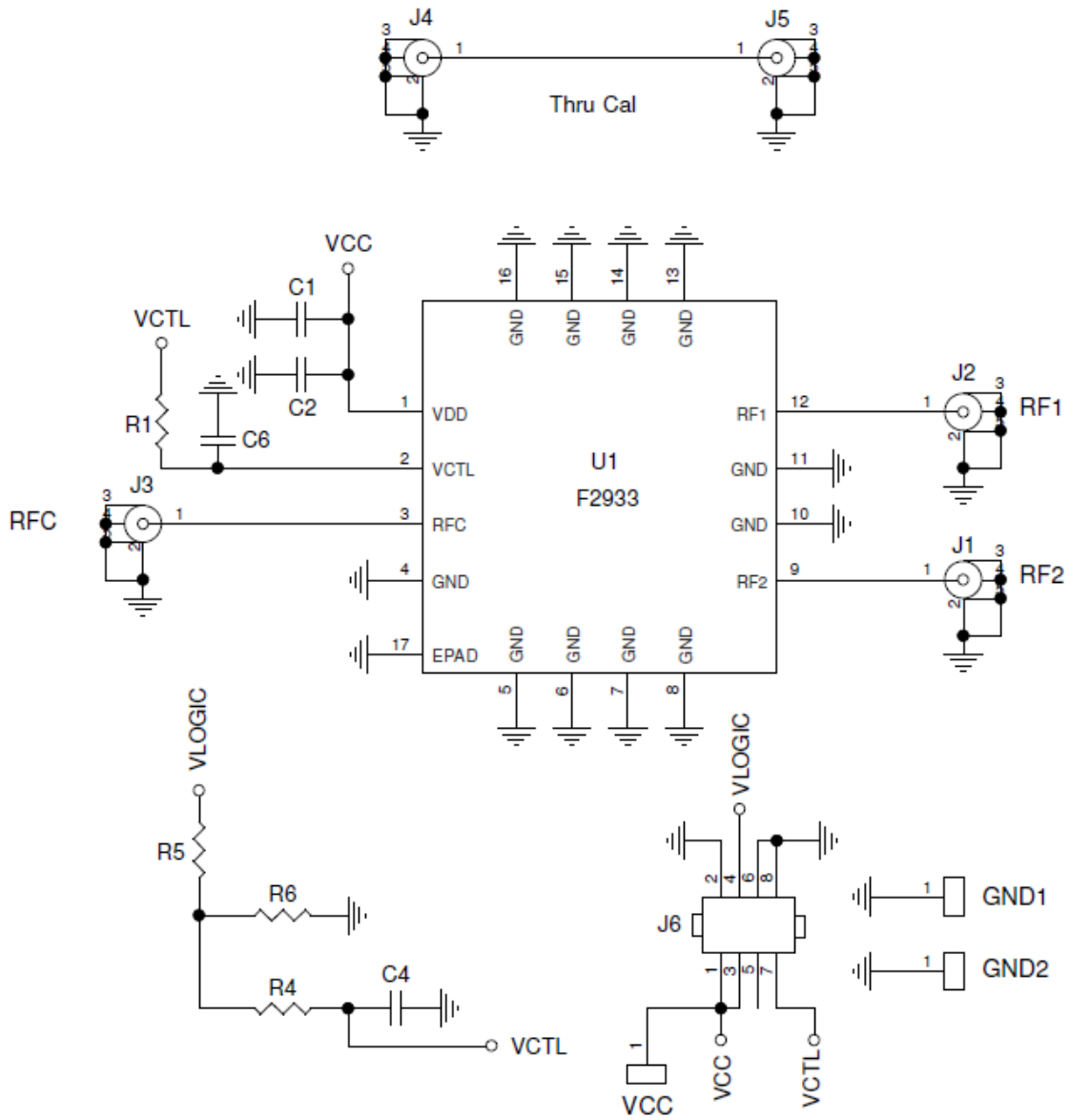
EVKIT PICTURE (TOP)



EVKIT PICTURE (BOTTOM)



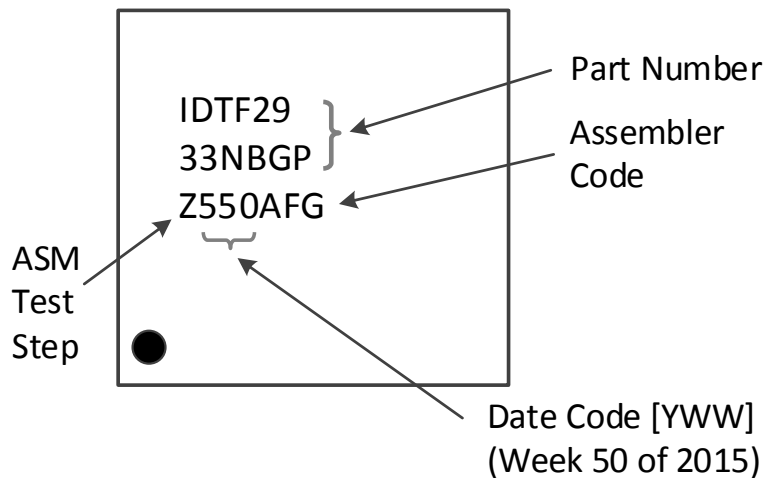
EVKIT / APPLICATIONS CIRCUIT



## EVKIT BOM

Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1	0	Not Installed (0402)		
C2	1	0.1 $\mu$ F $\pm$ 10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C4, C6	0	Not Installed (0402)		
R1	1	100 $\Omega$ $\pm$ 1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R4	1	100k $\Omega$ $\pm$ 1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
R5	1	15k $\Omega$ $\pm$ 1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R6	1	18k $\Omega$ $\pm$ 1%, 1/10W, Resistor (0402)	ERJ-2RKF1802X	Panasonic
J1 – J5	5	SMA Edge Launch (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J6	1	CONN HEADER VERT 4x2 POS GOLD	67997-108HLF	FCI
U1	1	SP2T Switch 4 mm x 4 mm QFN16-EP	F2933NBGP	IDT
VCC	1	Test Point Loop (Red)	5000	Keystone Electronics
GND1, GND2	2	Test Point Loop (Black)	5001	Keystone Electronics
	1	Printed Circuit Board	F2933 EVKIT REV 1	IDT

## TOP MARKINGS



**APPLICATIONS INFORMATION**

**Default Start-up**

There is no internal pull-up or pull-down resistor on the VCTL pin.

**Logic Control**

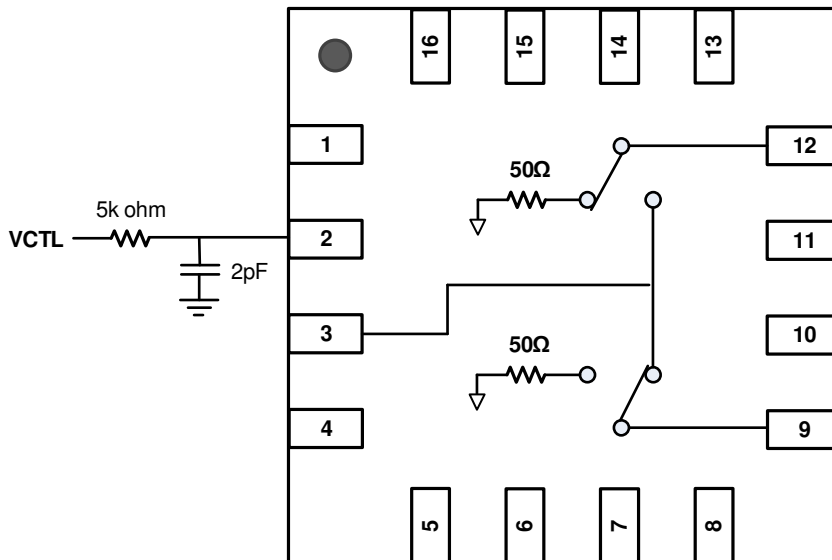
The VCTL pin is used to set the state of the SP2T switch (see Table 1).

**Power Supplies**

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20  $\mu$ s. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

**Control Pin Interface**

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit is recommended at the input of control pin 2 (VCTL). See figure below.





## **EVKIT OPERATION**

### **External Supply Setup**

Set up a VCC power supply in the voltage range of 2.7 V to 5.5 V and disable the power supply output.

### **Logic Control Setup**

#### **Using the EVKIT to manually set the control logic:**

On connector J6 connect a 2-pin shunt from pin 3 (VCC) to pin 4 (VLOGIC). This connection provides the VCC voltage supply to the Eval Board logic control pull up network. Resistors R5 and R6 form a voltage divider to set the Vhigh level over the 2.7 V to 5.5 V VCC range for manual logic control.

Connector J6 has one logic input pin: VCTL (pin 7). See Table 1 for Logic Truth Table. With the pullup network enabled (as noted above) this pin can be left open to provide a logic high through pull up resistor R4. To set a logic low for VCTL connect a 2-pin shunt on J6 from pin 7 (VCTL) to pin 8 (GND).

Note that when using the on board R5 / R6 voltage divider the current draw from the VCC supply will be higher by approximately  $VCC / 33k \Omega$ .

#### **Using external control logic:**

Pins 3, 4, 5, 6, and 8 of J6 should have no external connection. External logic control is applied to J6 pin 7 (VCTL). See Table 1 for Logic Truth Table.

### **Turn on Procedure**

Setup the supplies and Eval Board as noted in the **External Supply Setup** and **Logic Control Setup** sections above.

Connect the preset disabled VCC power supply to the red VCC loop and ground to GND1 or GND2.

Enable the VCC supply.

Set the desired logic setting using J6 pin 7 (VCTL) to achieve the desired Table 1 setting. Note that external control logic should not be applied without VCC being present.

### **Turn off Procedure**

If using external control logic for VCTL then set it to a logic low.

Disable the VCC supply.

**Revision History Sheet**

<b>Rev</b>	<b>Date</b>	<b>Page</b>	<b>Description of Change</b>
0	2016-May-04		Initial Release



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.