

# MC33260

## GreenLine™ Compact Power Factor Controller: Innovative Circuit for Cost Effective Solutions

The MC33260 is a controller for Power Factor Correction preconverters meeting international standard requirements in electronic ballast and off-line power conversion applications. Designed to drive a free frequency discontinuous mode, it can also be synchronized and in any case, it features very effective protections that ensure a safe and reliable operation.

This circuit is also optimized to offer extremely compact and cost effective PFC solutions. While it requires a minimum number of external components, the MC33260 can control the follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered.

Also able to function in a traditional way (constant output voltage regulation level), any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

### General Features

- Standard Constant Output Voltage or “Follower Boost” Mode
- Switch Mode Operation: Voltage Mode
- Latching PWM for Cycle-by-Cycle On-Time Control
- Constant On-Time Operation That Saves the Use of an Extra Multiplier
- Totem Pole Output Gate Drive
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Improved Regulation Block Dynamic Behavior
- Synchronization Capability
- Internally Trimmed Reference Current Source
- These are Pb-Free Devices

### Safety Features

- Overvoltage Protection: Output Overvoltage Detection
- Undervoltage Protection: Protection Against Open Loop
- Effective Zero Current Detection
- Accurate and Adjustable Maximum On-Time Limitation
- Overcurrent Protection
- ESD Protection on Each Pin

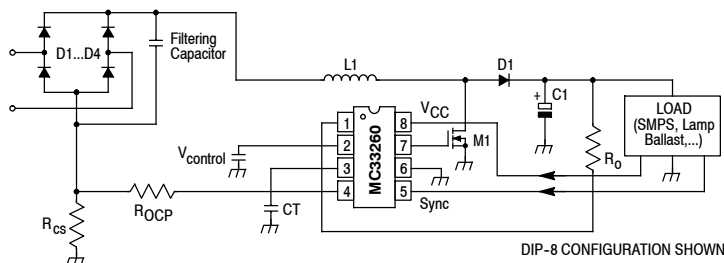


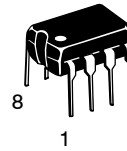
Figure 1. Typical Application



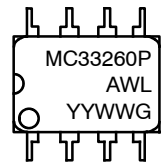
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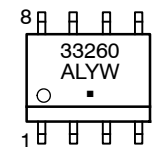
### MARKING DIAGRAMS



PDIP-8  
P SUFFIX  
CASE 626

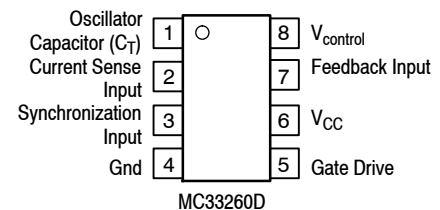
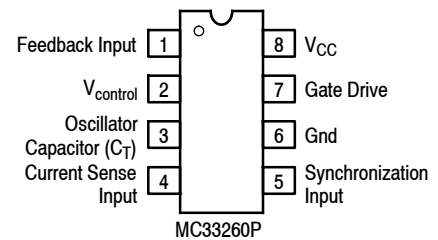


SO-8  
D SUFFIX  
CASE 751



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

# MC33260

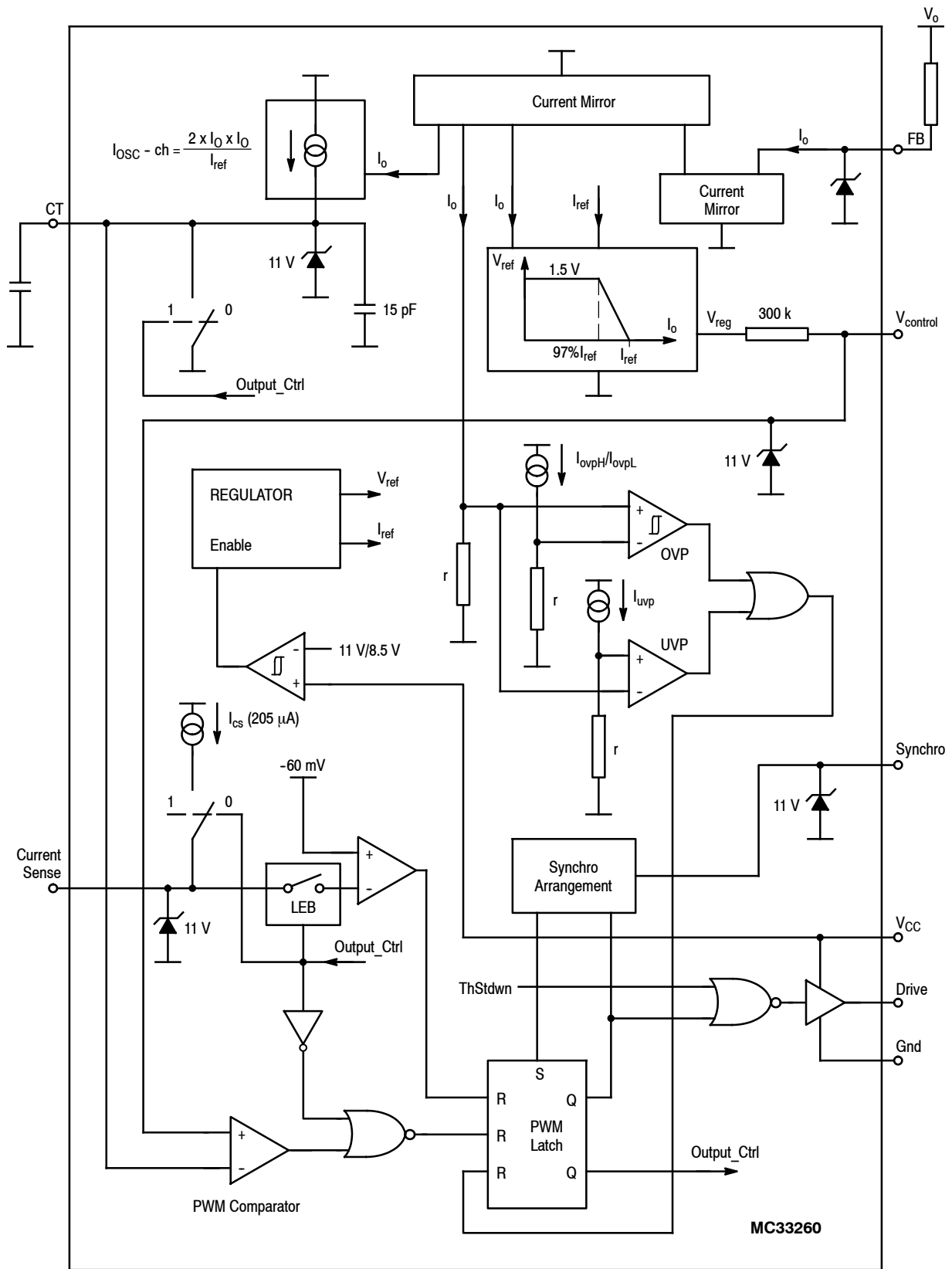


Figure 2. Block Diagram

# MC33260

## MAXIMUM RATINGS

Rating	Pin # PDIP-8	Pin # SO-8	Symbol	Value	Unit
Gate Drive Current* Source Sink	7	5	$I_{O(\text{Source})}$ $I_{O(\text{Sink})}$	-500 500	mA
V <sub>CC</sub> Maximum Voltage	8	6	(V <sub>CC</sub> ) <sub>max</sub>	16	V
Input Voltage			V <sub>in</sub>	-0.3 to +10	V
Power Dissipation and Thermal Characteristics P Suffix, PDIP Package Maximum Power Dissipation @ T <sub>A</sub> = 85°C Thermal Resistance Junction-to-Air			P <sub>D</sub> R <sub>θJA</sub>	600 100	mW °C/W
Operating Junction Temperature			T <sub>J</sub>	150	°C
Operating Ambient Temperature			T <sub>A</sub>	-40 to +105	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 13 V, T<sub>J</sub> = 25°C for typical values, T<sub>J</sub> = -40 to 105°C for min/max values unless otherwise noted.)

Characteristic	Pin # PDIP-8	Pin # SO-8	Symbol	Min	Typ	Max	Unit
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## GATE DRIVE SECTION

Gate Drive Resistor Source Resistor @ I <sub>Drive</sub> = 100 mA Sink Resistor @ I <sub>Drive</sub> = 100 mA	7	5	R <sub>OL</sub> R <sub>OH</sub>	10 5	20 10	35 25	Ω
Gate Drive Voltage Rise Time (From 3.0 V Up to 9.0 V) (Note 1)	7	5	t <sub>r</sub>	-	50	-	ns
Output Voltage Falling Time (From 9.0 V Down to 3.0 V) (Note 1)	7	5	t <sub>f</sub>	-	50	-	ns

## OSCILLATOR SECTION

Maximum Oscillator Swing	3	1	ΔV <sub>T</sub>	1.4	1.5	1.6	V
Charge Current @ I <sub>FB</sub> = 100 μA	3	1	I <sub>charge</sub>	87.5	100	112.5	μA
Charge Current @ I <sub>FB</sub> = 200 μA	3	1	I <sub>charge</sub>	350	400	450	μA
Ratio Multiplier Gain Over Maximum Swing @ I <sub>FB</sub> = 100 μA	3	1	K <sub>osc</sub>	5600	6400	7200	1/(V.A)
Ratio Multiplier Gain Over Maximum Swing @ I <sub>FB</sub> = 200 μA	3	1	K <sub>osc</sub>	5600	6400	7200	1/(V.A)
Average Internal Oscillator Pin Capacitance Over Oscillator Maximum Swing (C <sub>T</sub> Voltage Varying From 0 Up to 1.5 V) (Note 2)	3	1	C <sub>int</sub>	10	15	20	pF
Discharge Time (C <sub>T</sub> = 1.0 nF)	3	1	T <sub>disch</sub>	-	0.5	1.0	μs

## REGULATION SECTION

Regulation High Current Reference	1	7	I <sub>regH</sub>	192	200	208	μA
Ratio (Regulation Low Current Reference)/I <sub>regH</sub>	1	7	I <sub>regL</sub> /I <sub>regH</sub>	0.965	0.97	0.98	-
V <sub>control</sub> Impedance	1	7	Z <sub>Vcontrol</sub>	-	300	-	kΩ

NOTE: I<sub>FB</sub> is the current that is drawn by the Feedback Input Pin.

- 1.0 nF being connected between the Pin 7 and ground for PDIP-8, between Pin 5 and ground for SO-8.
- Guaranteed by design.

# MC33260

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 13\text{ V}$ ,  $T_J = 25^\circ\text{C}$  for typical values,  $T_J = -40$  to  $105^\circ\text{C}$  for min/max values unless otherwise noted.)

Characteristic	Pin # PDIP-8	Pin # SO-8	Symbol	Min	Typ	Max	Unit
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## REGULATION SECTION (continued)

Feedback Pin Clamp Voltage @ $I_{FB} = 100\ \mu\text{A}$	1	7	$V_{FB-100}$	1.5	2.1	2.5	V
Feedback Pin Clamp Voltage @ $I_{FB} = 200\ \mu\text{A}$	1	7	$V_{FB-200}$	2.0	2.6	3.0	V

## CURRENT SENSE SECTION

Zero Current Detection Comparator Threshold	4	2	$V_{ZCD-th}$	-90	-60	-30	mV
Negative Clamp Level ( $I_{CS-pin} = -1.0\ \text{mA}$ )	4	2	Cl-neg	-	-0.7	-	V
Bias Current @ $V_{cs} = V_{ZCD-th}$	4	2	$I_{b-cs}$	-0.2	-	-	$\mu\text{A}$
Propagation Delay ( $V_{cs} > V_{ZCD-th}$ ) to Gate Drive High	7	5	$T_{ZCD}$	-	500	-	ns
Current Sense Pin Internal Current Source	4	2	$I_{OCP}$	192	205	218	$\mu\text{A}$
Leading Edge Blanking Duration			$\tau_{LEB}$	-	400	-	ns
OverCurrent Protection Propagation Delay ( $V_{cs} < V_{ZCD-th}$ to Gate Drive Low)	7	5	$T_{OCP}$	100	160	240	ns

## SYNCHRONIZATION SECTION

Synchronization Threshold PDIP-8 SO-8	5 -	- 3	$V_{sync-th}$ $V_{sync-th}$	0.8 0.8	1.0 1.0	1.2 1.4	V V
Negative Clamp Level ( $I_{sync} = -1.0\ \text{mA}$ )	5	3	Cl-neg	-	-0.7	-	V
Minimum Off-Time	7	5	$T_{off}$	1.5	2.1	2.7	$\mu\text{s}$
Minimum Required Synchronization Pulse Duration	5	3	$T_{sync}$	-	-	0.5	$\mu\text{s}$

## OVERVOLTAGE PROTECTION SECTION

OverVoltage Protection High Current Threshold and $I_{regH}$ Difference	1	7	$I_{OVPH} - I_{regH}$	8.0	13	18	$\mu\text{A}$
OverVoltage Protection Low Current Threshold and $I_{regH}$ Difference	1	7	$I_{OVPL} - I_{regH}$	0	-	-	-
Ratio ( $I_{OVPH}/I_{OVPL}$ )	1	7	$I_{OVPH}/I_{OVPL}$	1.02	-	-	-
Propagation Delay ( $I_{FB} > 110\% I_{ref}$ to Gate Drive Low)	7	5	$T_{OVP}$	-	500	-	ns

## UNDERVOLTAGE PROTECTION SECTION

Ratio (UnderVoltage Protection Current Threshold) / $I_{regH}$	1	7	$I_{UVP}/I_{regH}$	12	14	16	%
Propagation Delay ( $I_{FB} < 12\% I_{ref}$ to Gate Drive Low)	7	5	$T_{UVP}$	-	500	-	ns

## THERMAL SHUTDOWN SECTION

Thermal Shutdown Threshold	7	5	$T_{stdwn}$	—	150	-	$^\circ\text{C}$
Hysteresis	7	5	$\Delta T_{stdwn}$	-	30	-	$^\circ\text{C}$

## V<sub>CC</sub> UNDERVOLTAGE LOCKOUT SECTION

Startup Threshold	8	6	$V_{stup-th}$	9.7	11	12.3	V
Disable Voltage After Threshold Turn-On	8	6	$V_{disable}$	7.4	8.5	9.6	V

## TOTAL DEVICE

Power Supply Current Startup ( $V_{CC} = 5\ \text{V}$ with $V_{CC}$ Increasing) Operating @ $I_{FB} = 200\ \mu\text{A}$	8	6	$I_{CC}$	- -	0.1 4.0	0.25 8.0	mA
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NOTE:  $V_{cs}$  is the Current Sense Pin Voltage and  $I_{FB}$  is the Feedback Pin Current.

Pin Numbers are Relevant to the PDIP-8 Version

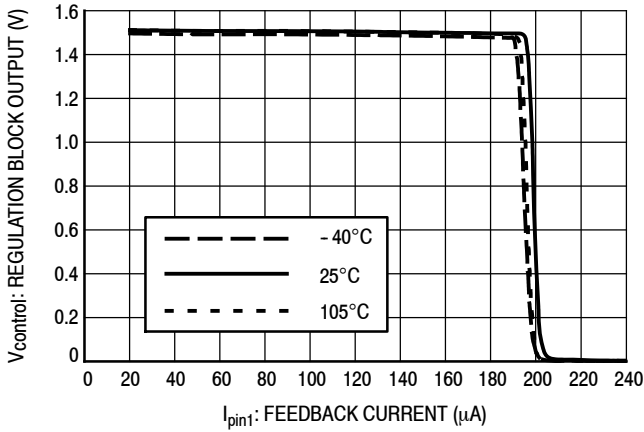


Figure 3. Regulation Block Output versus Feedback Current

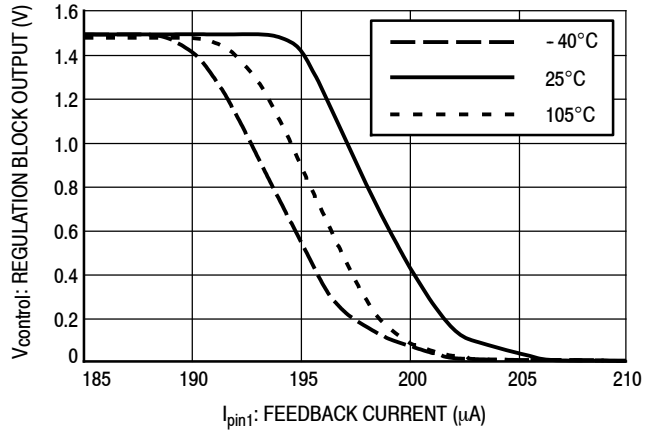


Figure 4. Regulation Block Output versus Feedback Current

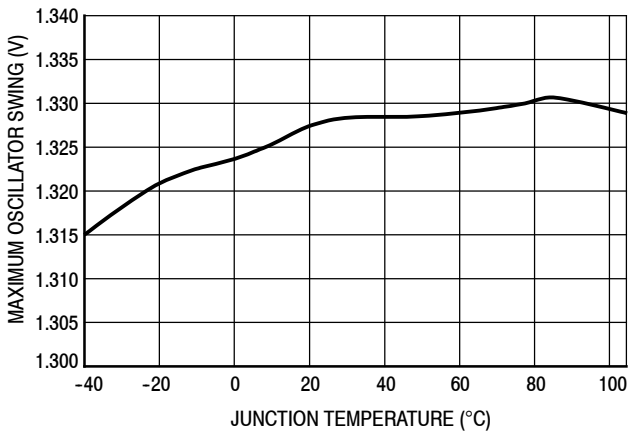


Figure 5. Maximum Oscillator Swing versus Temperature

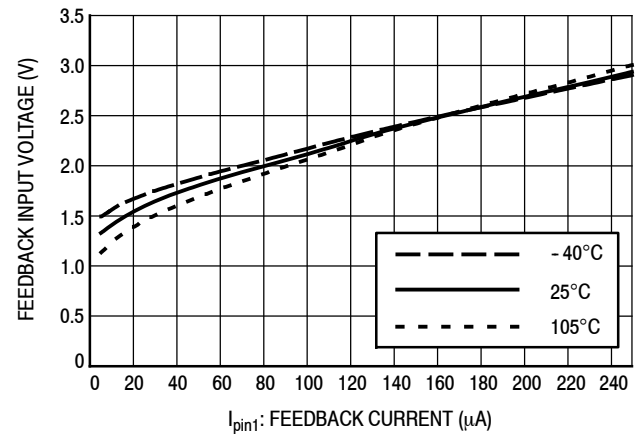


Figure 6. Feedback Input Voltage versus Feedback Current

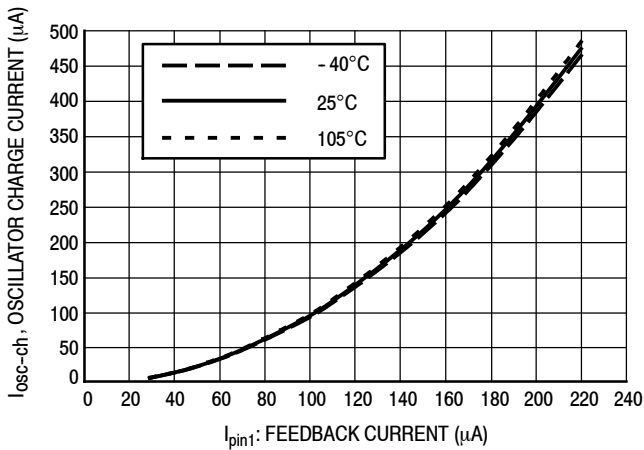


Figure 7. Oscillator Charge Current versus Feedback Current

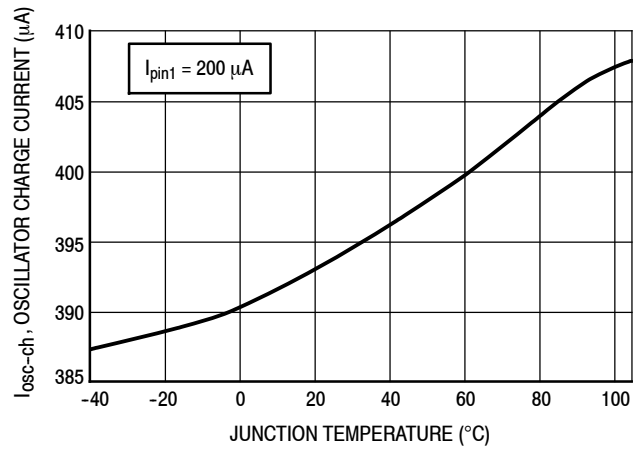


Figure 8. Oscillator Charge Current versus Temperature

Pin Numbers are Relevant to the PDIP-8 Version

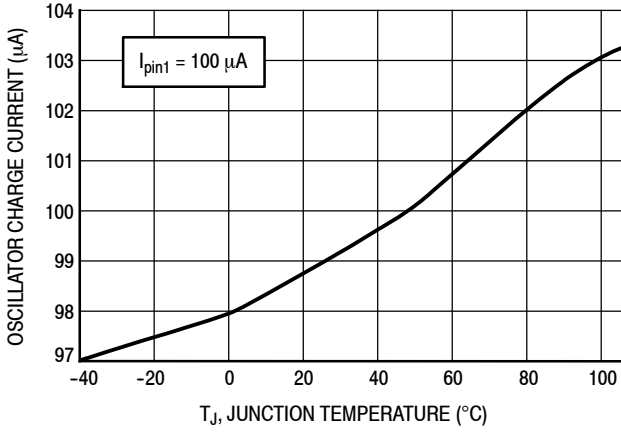


Figure 9. Oscillator Charge Current versus Temperature

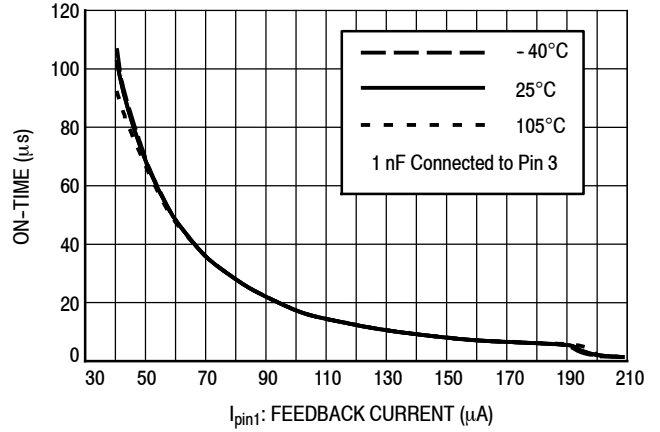


Figure 10. On-Time versus Feedback Current

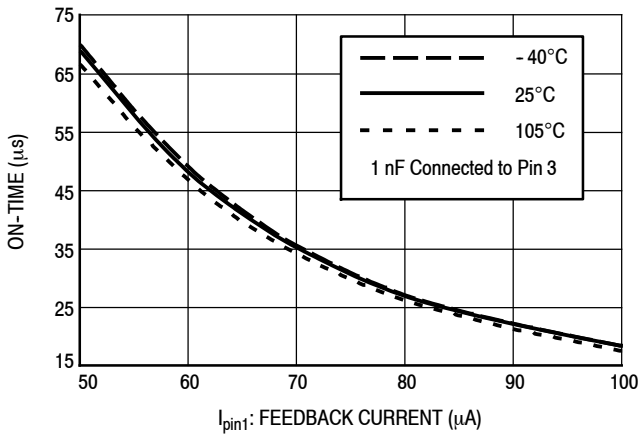


Figure 11. On-Time versus Feedback Current

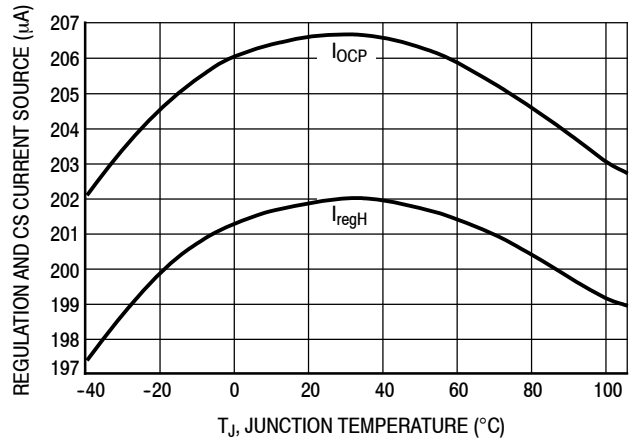


Figure 12. Internal Current Sources versus Temperature

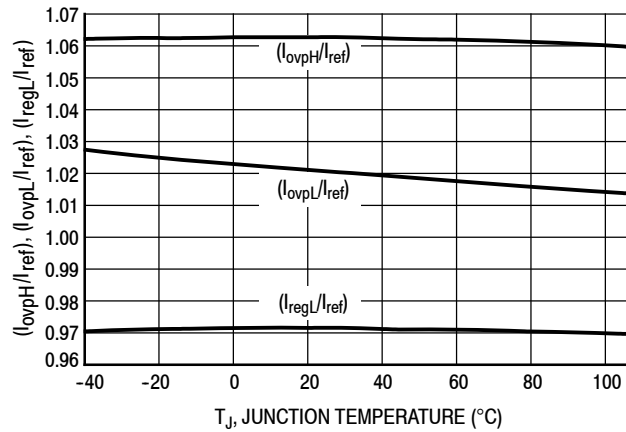


Figure 13.  $(I_{ovpH}/I_{ref})$ ,  $(I_{ovpL}/I_{ref})$ ,  $(I_{regL}/I_{ref})$  versus Temperature

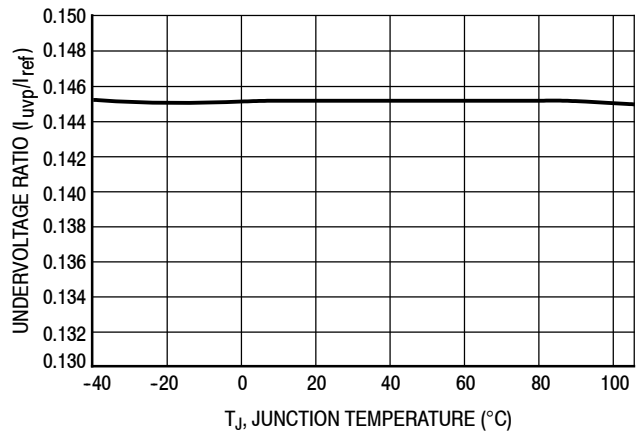


Figure 14. Undervoltage Ratio versus Temperature

Pin Numbers are Relevant to the PDIP-8 Version

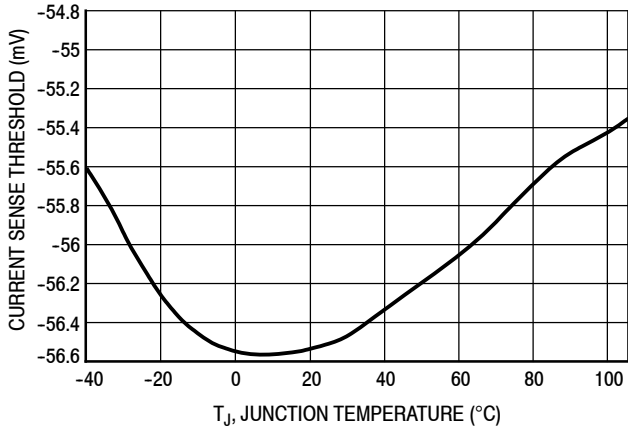


Figure 15. Current Sense Threshold versus Temperature

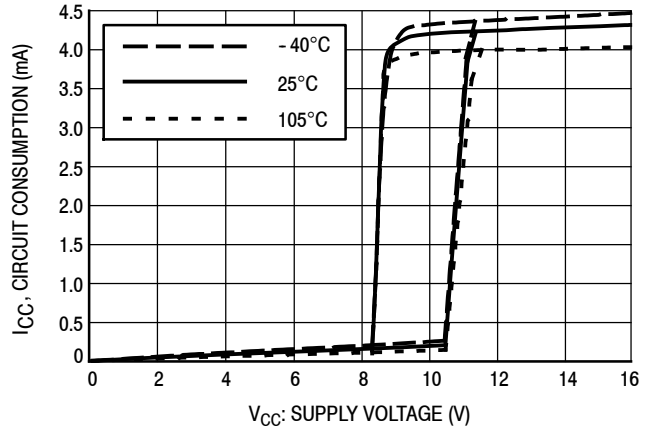


Figure 16. Circuit Consumption versus Supply Voltage

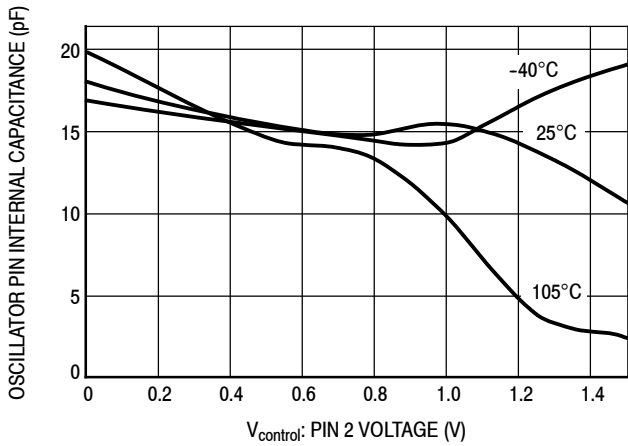


Figure 17. Oscillator Pin Internal Capacitance

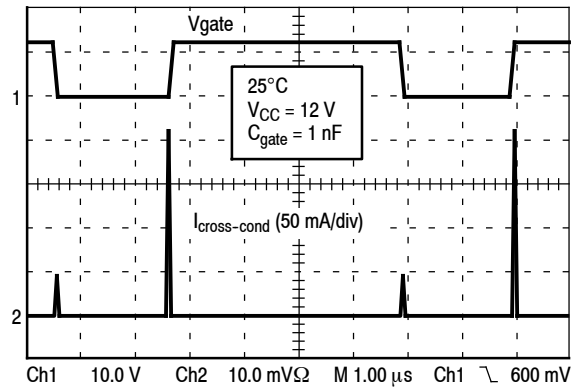


Figure 18. Gate Drive Cross Conduction

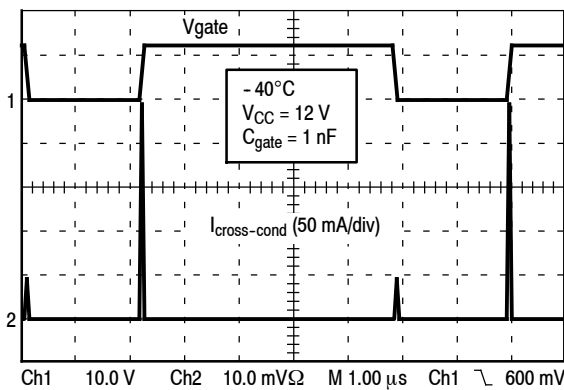


Figure 19. Gate Drive Cross Conduction

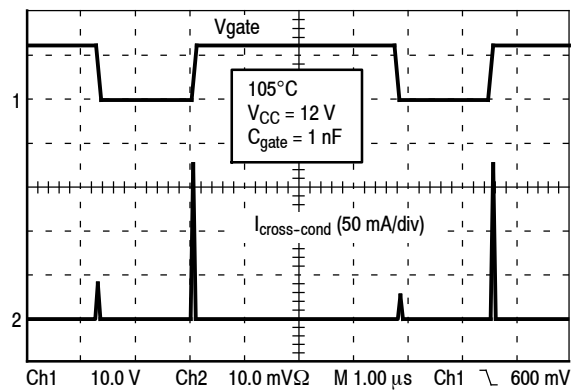


Figure 20. Gate Drive Cross Conduction

# MC33260

## PIN FUNCTION DESCRIPTION

Pin # PDIP-8	Pin # SO-8	Function	Description
1	7	Feedback Input	This pin is designed to receive a current that is proportional to the preconverter output voltage. This information is used for both the regulation and the overvoltage and undervoltage protections. The current drawn by this pin is internally squared to be used as oscillator capacitor charge current.
2	8	$V_{control}$	This pin makes available the regulation block output. The capacitor connected between this pin and ground, adjusts the control bandwidth. It is typically set below 20 Hz to obtain a nondistorted input current.
3	1	Oscillator Capacitor ( $C_T$ )	The circuit uses an on-time control mode. This on-time is controlled by comparing the $C_T$ voltage to the $V_{control}$ voltage. $C_T$ is charged by the squared feedback current.
4	2	Zero Current Detection Input	This pin is designed to receive a negative voltage signal proportional to the current flowing through the inductor. This information is generally built using a sense resistor. The Zero Current Detection prevents any restart as long as the Pin 4 voltage is below (-60 mV). This pin is also used to perform the peak current limitation. The overcurrent threshold is programmed by the resistor connected between the pin and the external current sense resistor.
5	3	Synchronization Input	This pin is designed to receive a synchronization signal. For instance, it enables to synchronize the PFC preconverter to the associated SMPS. If not used, this pin must be grounded.
6	4	Ground	This pin must be connected to the preregulator ground.
7	5	Gate Drive	The gate drive current capability is suited to drive an IGBT or a power MOSFET.
8	6	$V_{CC}$	This pin is the positive supply of the IC. The circuit turns on when $V_{CC}$ becomes higher than 11 V, the operating range after startup being 8.5 V up to 16 V.

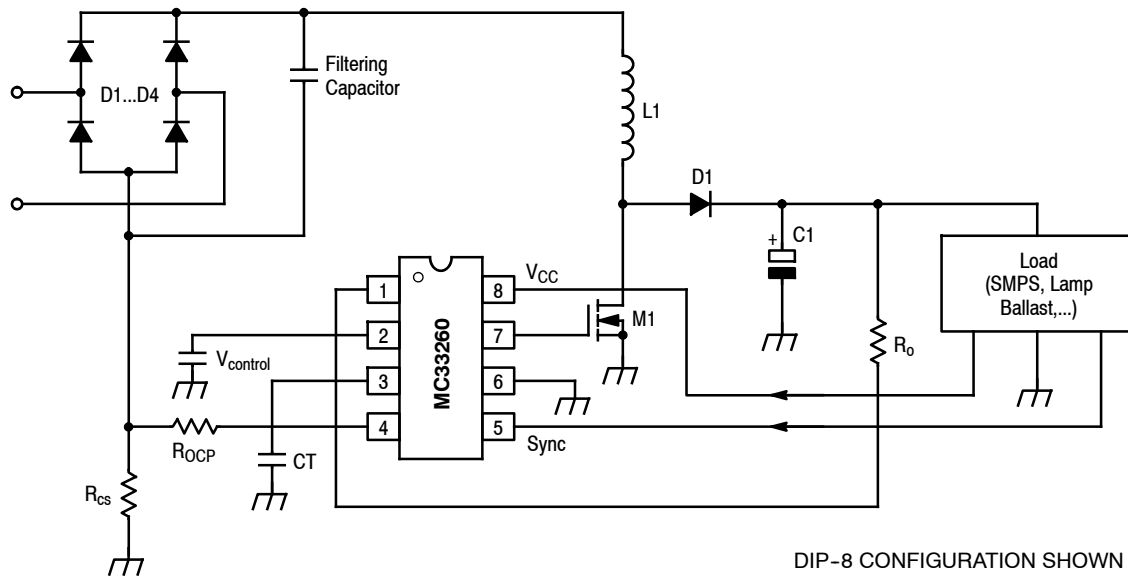


Figure 21. Application Schematic

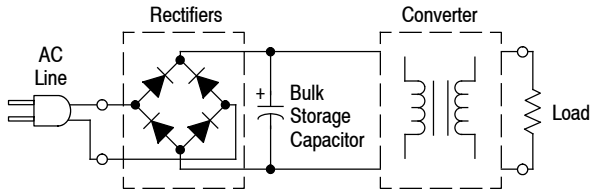


**FUNCTIONAL DESCRIPTION**  
**Pin Numbers are Relevant to the PDIP-8 Version**

**INTRODUCTION**

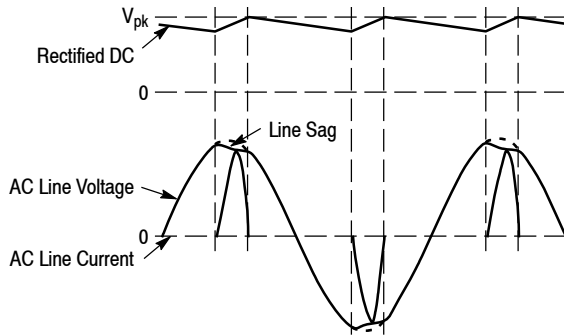
The need of meeting the requirements of legislation on line current harmonic content, results in an increasing demand for cost effective solutions to comply with the Power Factor regulations. This data sheet describes a monolithic controller specially designed for this purpose.

Most off-line appliances use a bridge rectifier associated to a huge bulk capacitor to derive raw dc voltage from the utility ac line.



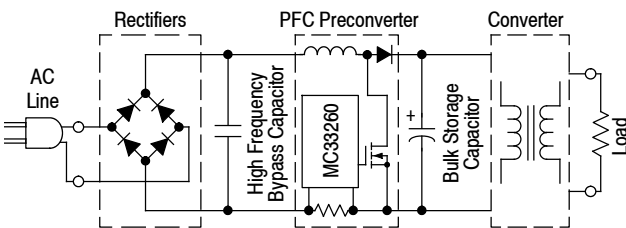
**Figure 22. Typical Circuit Without PFC**

This technique results in a high harmonic content and in poor power factor ratios. In effect, the simple rectification technique draws power from the mains when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike. Consequently, a poor power factor (in the range of 0.5 - 0.7) is generated, resulting in an apparent input power that is much higher than the real power.



**Figure 23. Line Waveforms Without PFC**

Active solutions are the most popular way to meet the legislation requirements. They consist of inserting a PFC pre-regulator between the rectifier bridge and the bulk capacitor. This interface is, in fact, a step-up SMPS that outputs a constant voltage while drawing a sinusoidal current from the line.



**Figure 24. PFC Preconverter**

The MC33260 was developed to control an active solution with the goal of increasing its robustness while lowering its global cost.

**OPERATION DESCRIPTION**

The MC33260 is optimized to just as well drive a free running as a synchronized discontinuous voltage mode.

It also features valuable protections (overvoltage and undervoltage protection, overcurrent limitation, ...) that make the PFC preregulator very safe and reliable while requiring very few external components. In particular, it is able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage (startup, overload, ...).

In addition to the low count of elements, the circuit can control an innovative mode named "Follower Boost" that permits to significantly reduce the size of the preconverter inductor and power MOSFET. With this technique, the output regulation level is not forced to a constant value, but can vary according to the a.c. line amplitude and to the power. The gap between the output voltage and the ac line is then lowered, what allows the preconverter inductor and power MOSFET size reduction. Finally, this method brings a significant cost reduction.

A description of the functional blocks is given below.

**REGULATION SECTION**

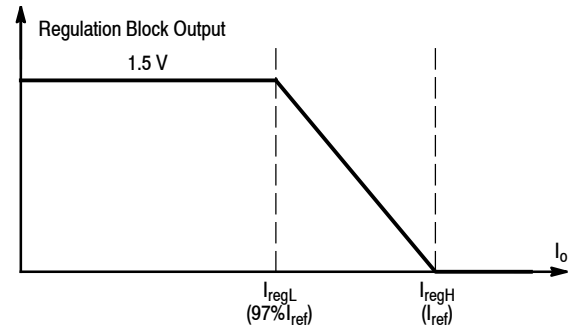
Connecting a resistor between the output voltage to be regulated and the Pin 1, a feedback current is obtained. Typically, this current is built by connecting a resistor between the output voltage and the Pin 1. Its value is then given by the following equation:

$$I_{pin1} = \frac{V_o - V_{pin1}}{R_o}$$

where:

- R<sub>o</sub> is the feedback resistor,
- V<sub>o</sub> is the output voltage,
- V<sub>pin1</sub> is the Pin 1 clamp value.

The feedback current is compared to the reference current so that the regulation block outputs a signal following the characteristic depicted in Figure 25. According to the power and the input voltage, the output voltage regulation level varies between two values (V<sub>o</sub>)<sub>regL</sub> and (V<sub>o</sub>)<sub>regH</sub> corresponding to the I<sub>regL</sub> and I<sub>regH</sub> levels.



**Figure 25. Regulation Characteristic**

The feedback resistor must be chosen so that the feedback current should equal the internal current source I<sub>regH</sub> when the output voltage exceeds the chosen upper regulation voltage [(V<sub>o</sub>)<sub>regH</sub>].



Pin Numbers are Relevant to the PDIP-8 Version

This equation shows that the maximum on-time is inversely proportional to the squared output voltage. This property is used for follower boost operation (refer to **Follower Boost** section).

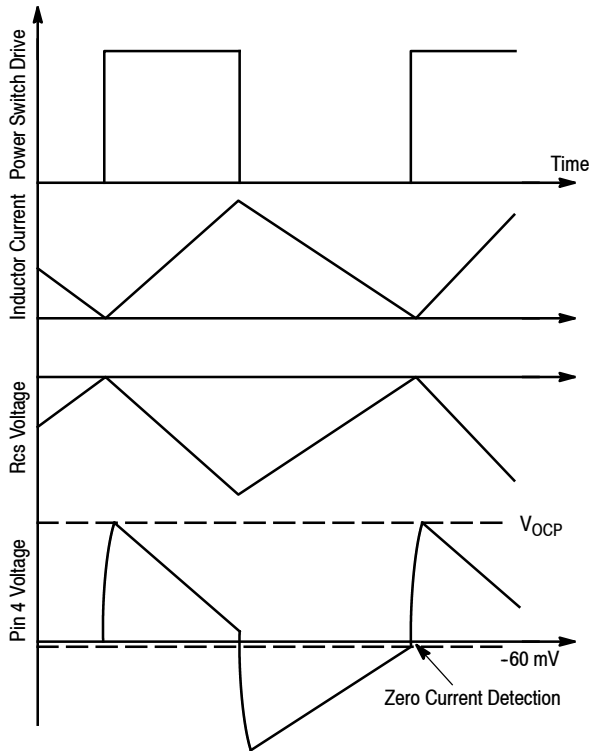
**CURRENT SENSE BLOCK**

The inductor current is converted into a voltage by inserting a ground referenced resistor ( $R_{CS}$ ) in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$V_{CS} = -(R_{CS} \times I_L)$$

where:

- $I_L$  is the inductor current,
- $R_{CS}$  is the current sense resistor,
- $V_{CS}$  is the measured  $R_{CS}$  voltage.



$V_{OCP} = R_{OCP} \times I_{OCP}$   
An overcurrent is detected if  $V_{pin4}$  crosses the threshold (-60 mV) during the Power Switch on state

**Figure 27. Current Sensing**

The negative signal  $V_{CS}$  is applied to the current sense through a resistor  $R_{OCP}$ . The pin is internally protected by a negative clamp (-0.7 V) that prevents substrate injection.

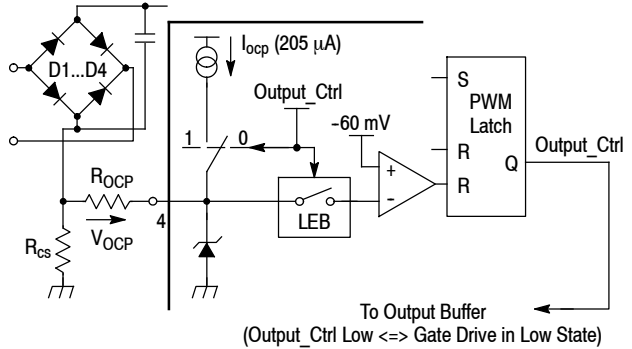
As long as the Pin 4 voltage is lower than (-60 mV), the Current Sense comparator resets the PWM latch to force the gate drive signal low state. In that condition, the power MOSFET cannot be on.

During the on-time, the Pin 4 information is used for the overcurrent limitation while it serves the zero current detection during the off time.

**Zero Current Detection**

The Zero Current Detection function guarantees that the MOSFET cannot turn on as long as the inductor current hasn't reached zero (discontinuous mode).

The Pin 4 voltage is simply compared to the (-60 mV) threshold so that as long as  $V_{CS}$  is lower than this threshold, the circuit gate drive signal is kept in low state. Consequently, no power MOSFET turn on is possible until the inductor current is measured as smaller than  $(60 \text{ mV}/R_{CS})$  that is, the inductor current nearly equals zero.



**Figure 28. Current Sense Block**

**Overcurrent Protection**

During the power switch conduction (i.e. when the Gate Drive Pin voltage is high), a current source is applied to the Pin 4. A voltage drop  $V_{OCP}$  is then generated across the resistor  $R_{OCP}$  that is connected between the sense resistor and the Current Sense Pin (refer to Figure 28). So, instead of  $V_{CS}$ , the sum  $(V_{CS} + V_{OCP})$  is compared to (-60 mV) and the maximum permissible current is the solution of the following equation:

$$-(R_{CS} \times I_{pk_{max}}) + V_{OCP} = -60 \text{ mV}$$

where:

- $I_{pk_{max}}$  is maximum allowed current,
- $R_{CS}$  is the sensing resistor.

The overcurrent threshold is then:

$$I_{pk_{max}} = \frac{(R_{OCP} \times I_{OCP}) + 60 \times 10^{-3}}{R_{CS}}$$

where:

- $R_{OCP}$  is the resistor connected between the pin and the sensing resistor ( $R_{CS}$ ),
- $I_{OCP}$  is the current supplied by the Current Sense Pin when the gate drive signal is high (power switch conduction phase).  $I_{OCP}$  equals 205  $\mu\text{A}$  typically.

Practically, the  $V_{OCP}$  offset is high compared to 60 mV and the precedent equation can be simplified. The maximum current is then given by the following equation:

$$I_{pk_{max}} \approx \frac{R_{OCP}(\text{k}\Omega)}{R_{CS}(\Omega)} \times 0.205 \text{ (A)}$$

Consequently, the  $R_{OCP}$  resistor can program the OCP level whatever the  $R_{CS}$  value is. This gives a high freedom in the choice of  $R_{CS}$ . In particular, the inrush resistor can be utilized.

Pin Numbers are Relevant to the PDIP-8 Version

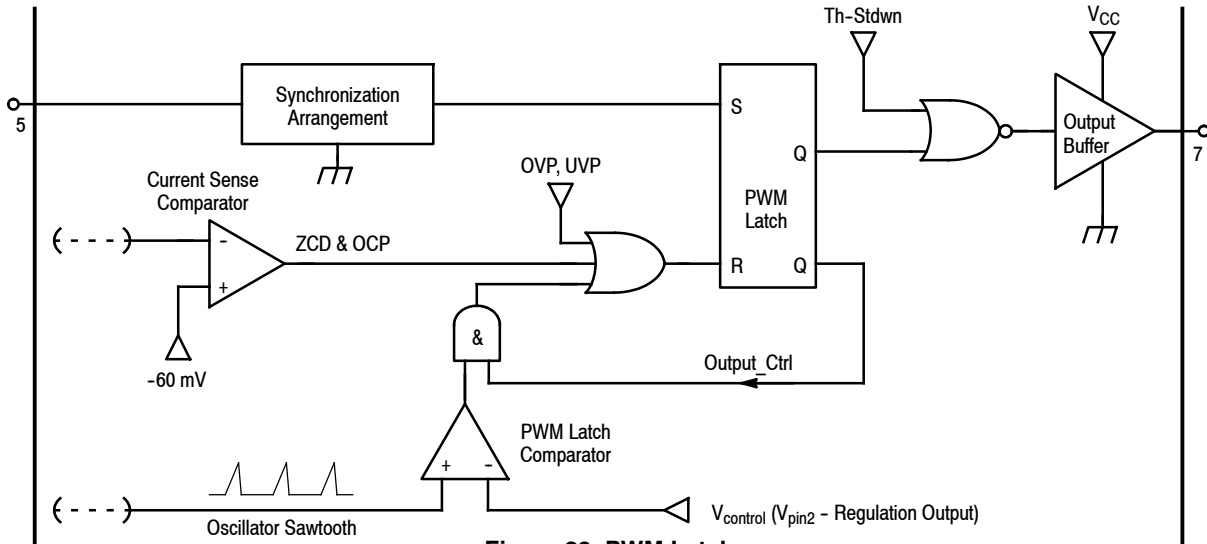


Figure 29. PWM Latch

A LEB (Leading Edge Blanking) has been implemented. This circuitry disconnects the Current Sense comparator from Pin 4 and disables it during the 400 first ns of the power switch conduction. This prevents the block from reacting on the current spikes that generally occur at power switch turn on. Consequently, proper operation does not require any filtering capacitor on Pin 4.

**PROTECTIONS**

**OCP (Overcurrent Protection)**

Refer to **Current Sense Block**.

**OVP (Overvoltage Protection)**

The feedback current ( $I_o$ ) is compared to a threshold current ( $I_{ovpH}$ ). If it exceeds this value, the gate drive signal is maintained low until this current gets lower than a second level ( $I_{ovpL}$ ).

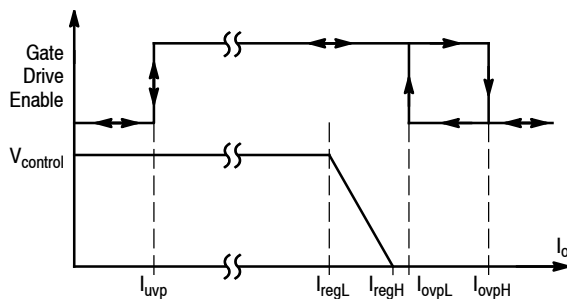


Figure 30. Internal Current Thresholds

So, the OVP upper threshold is:

$$V_{ovpH} = V_{pin1} + (R_o \times I_{ovpH})$$

where:

$R_o$  is the feedback resistor that is connected between Pin 1 and the output voltage,

$I_{ovpH}$  is the internal upper OVP current threshold,

$V_{pin1}$  is the Pin 1 clamp voltage.

Practically,  $V_{pin1}$  that is in the range of 2.5 V, can be neglected. The equation can then be simplified:

$$V_{ovpH} = R_o(M\Omega) \times I_{ovpH}(\mu A) (V)$$

On the other hand, the OVP low threshold is:

$$V_{ovpL} = V_{pin1} + (R_o \times I_{ovpL})$$

where  $I_{ovpL}$  is the internal low OVP current threshold. Consequently,  $V_{pin1}$  being neglected:

$$V_{ovpL} = R_o(M\Omega) \times I_{ovpL}(\mu A) (V)$$

The OVP hysteresis prevents erratic behavior.

$I_{ovpL}$  is guaranteed to be higher than  $I_{regH}$  (refer to parameters specification). This ensures that the OVP function doesn't interfere with the regulation one.

**UVP (Undervoltage Protection)**

This function detects when the feedback current is lower than 14% of  $I_{ref}$ . In this case, the PWM latch is reset and the power switch is kept off.

This protection is useful to:

- Protect the preregulator from working in too low mains conditions.
- To detect the feedback current absence (in case of a nonproper connection for instance).

The UVP threshold is:

$$V_{uvp} \approx V_{pin1} + (R_o(M\Omega) \times I_{uvp}(\mu A)) (V)$$

Practically ( $V_{pin1}$  being neglected),

$$V_{uvp} = R_o(M\Omega) \times I_{uvp}(\mu A) (V)$$

**Maximum On-Time Limitation**

As explained in **PWM Latch**, the maximum on-time is accurately controlled.

**Pin Protection**

All the pins are ESD protected.

## Pin Numbers are Relevant to the PDIP-8 Version

In particular, a 11 V Zener diode is internally connected between the terminal and ground on the following pins:

Feedback,  $V_{\text{control}}$ , Oscillator, Current Sense, and Synchronization.

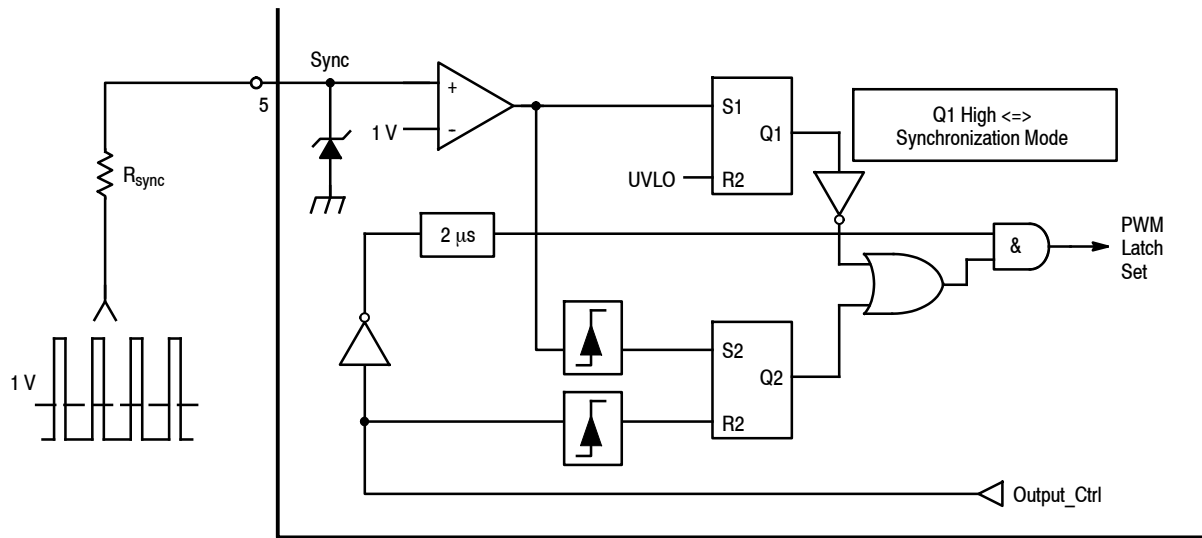


Figure 31. Synchronization Arrangement

### SYNCHRONIZATION BLOCK

The MC33260 features two modes of operation:

- Free Running Discontinuous Mode: The power switch is turned on as soon as there is no current left in the inductor (Zero Current Detection). This mode is simply obtained by grounding the synchronization terminal (Pin 5).
- Synchronization Mode: This mode is set as soon as a signal crossing the 1.0 V threshold, is applied to the Pin 5. In this case, operation in free running can only be recovered after a new circuit startup. In this mode, the power switch cannot turn on before the two following conditions are fulfilled.
  - Still, the zero current must have been detected.
  - The precedent turn on must have been followed by (at least) one synchronization raising edge crossing the 1.0 V threshold.

In other words, the synchronization acts to prolong the power switch off time.

Consequently, a proper synchronized operation requires that the current cycle (on-time + inductor demagnetization) is shorter than the synchronization period. Practically, the inductor must be chosen accordingly. Otherwise, the system will keep working in free running discontinuous mode. Figure 36 illustrates this behavior.

It must be noticed that whatever the mode is, a 2.0  $\mu\text{s}$  minimum off-time is forced. This delay limits the switching frequency in light load conditions.

### OUTPUT SECTION

The output stage contains a totem pole optimized to minimize the cross conduction current during high speed operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active. The rise and fall times have been controlled to typically equal 50 ns while loaded by 1.0 nF.

### REFERENCE SECTION

An internal reference current source ( $I_{\text{ref}}$ ) is trimmed to be  $\pm 4\%$  accurate over the temperature range (the typical value is 200  $\mu\text{A}$ ).  $I_{\text{ref}}$  is the reference used for the regulation ( $I_{\text{regH}} = I_{\text{ref}}$ ).

### UNDERVOLTAGE LOCKOUT SECTION

An Undervoltage Lockout comparator has been implemented to guarantee that the integrated circuit is operating only if its supply voltage ( $V_{\text{CC}}$ ) is high enough to enable a proper working. The UVLO comparator monitors the Pin 8 voltage and when it exceeds 11 V, the device gets active. To prevent erratic operation as the threshold is crossed, 2.5 V of hysteresis is provided.

The circuit off state consumption is very low: in the range of 100  $\mu\text{A}$  @  $V_{\text{CC}} = 5.0 \text{ V}$ . This consumption varies versus  $V_{\text{CC}}$  as the circuit presents a resistive load in this mode.

### THERMAL SHUTDOWN

An internal thermal circuitry is provided to disable the circuit gate drive and then to prevent it from oscillating, if the junction temperature exceeds 150°C typically.

The output stage is again enabled when the temperature drops below 120°C typically (30°C hysteresis).

Pin Numbers are Relevant to the PDIP-8 Version

**FOLLOWER BOOST**

Traditional PFC preconverters provide the load with a fixed and regulated voltage that generally equals 230 V or 400 V according to the mains type (U.S., European, or universal).

In the “Follower Boost” operation, the preconverter output regulation level is not fixed but varies linearly versus the ac line amplitude at a given input power.

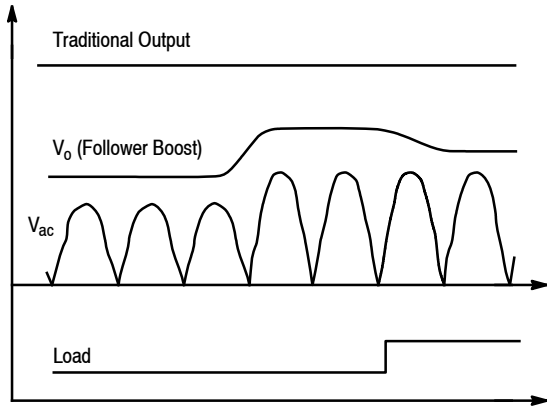


Figure 32. Follower Boost Characteristics

This technique aims at reducing the gap between the output and the input voltages to minimize the boost efficiency degradation.

**Follower Boost Benefits**

The boost presents two phases:

- The on-time during which the power switch is on. The inductor current grows up linearly according to a slope ( $V_{in}/L_p$ ), where  $V_{in}$  is the instantaneous input voltage and  $L_p$  the inductor value.
- The off-time during which the power switch is off. The inductor current decreases linearly according to the slope  $(V_o - V_{in})/L_p$ , where  $V_o$  is the output voltage. This sequence that terminates when the current equals zero, has a duration that is inversely proportional to the gap between the output and input voltages. Consequently, the off-time duration becomes longer in follower boost.

Consequently, for a given peak inductor current, the longer the off time, the smaller power switch duty cycle and then its conduction dissipation. This is the first benefit of this technique: the MOSFET on-time losses are reduced.

The increase of the off time duration also results in a switching frequency diminution (for a given inductor value). Given that in practise, the boost inductor is selected big enough to limit the switching frequency down to an acceptable level, one can immediately see the second benefit

of the follower boost: it allows the use of smaller, lighter and cheaper inductors compared to traditional systems.

Finally, this technique utilization brings a drastic system cost reduction by lowering the size and then the cost of both the inductor and the power switch.

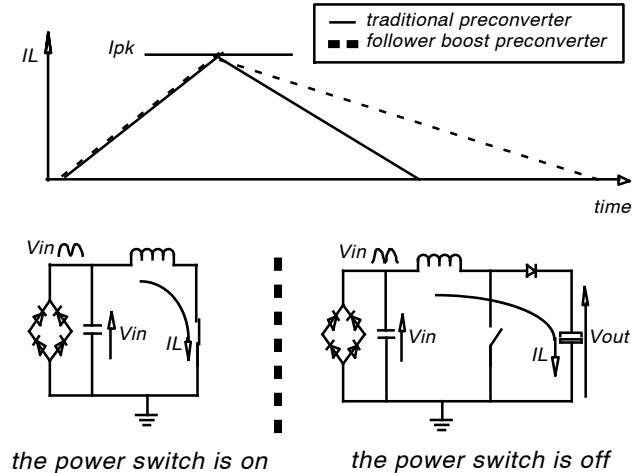


Figure 33. Off-Time Duration Increase

**Follower Boost Implementation**

In the MC33260, the on-time is differently controlled according to the feedback current level. Two areas can be defined:

- When the feedback current is higher than  $I_{regL}$  (refer to regulation section), the regulation block output ( $V_{control}$ ) is modulated to force the output voltage to a desired value.
- On the other hand, when the feedback current is lower than  $I_{regL}$ , the regulation block output and therefore, the on-time are maximum. As explained in **PWM Latch Section**, the on-time is then inversely proportional to the output voltage square. The Follower Boost is active in these conditions in which the on-time is simply limited by the output voltage level. Note: In this equation, the Feedback Pin voltage ( $V_{pin1}$ ) is neglected compared to the output voltage (refer to the **PWM Latch Section**).

$$t_{on} = (t_{on})_{max} = \frac{C_{pin3} \times R_o^2}{K_{osc} \times V_o^2}$$

where:

- $C_{pin3}$  is the total oscillator capacitor (sum of the internal and external capacitors -  $C_{int} + C_T$ ),
- $K_{osc}$  is the ratio (oscillator swing over oscillator gain),
- $V_o$  is the output voltage,
- $R_o$  is the feedback resistor.

Pin Numbers are Relevant to the PDIP-8 Version

On the other hand, the boost topology has its own rule that dictates the on-time necessary to deliver the required power:

$$t_{on} = \frac{4 \times L_p \times P_{in}}{V_{pk}^2}$$

where:

- $V_{pk}$  is the peak ac line voltage,
- $L_p$  is the inductor value,
- $P_{in}$  is the input power.

Combining the two equations, one can obtain the Follower Boost equation:

$$V_o = \frac{R_o}{2} \times \sqrt{\frac{C_{pin3}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$$

Consequently, a linear dependency links the output voltage to the ac line amplitude at a given input power.

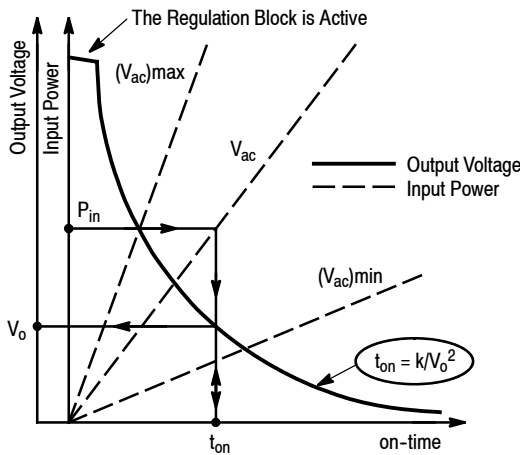


Figure 34. Follower Boost Characteristics

The behavior of the output voltage is depicted in Figures 34 and 35. In particular, Figure 35 illustrates how the output voltage converges to a stable equilibrium level. First, at a given ac line voltage, the on-time is dictated by the power demand. Then, the follower boost characteristic makes correspond one output voltage level to this on-time. Combining these two laws, it appears that the power level forces the output voltage.

One can notice that the system is fully stable:

- If an output voltage increase makes it move away from its equilibrium value, the on-time will immediately diminish according to the follower boost law. This will result in a delivered power decrease. Consequently, the supplied power being too low, the output voltage will decrease back,
- In the same way, if the output voltage decreases, more power will be transferred and then the output voltage will increase back.

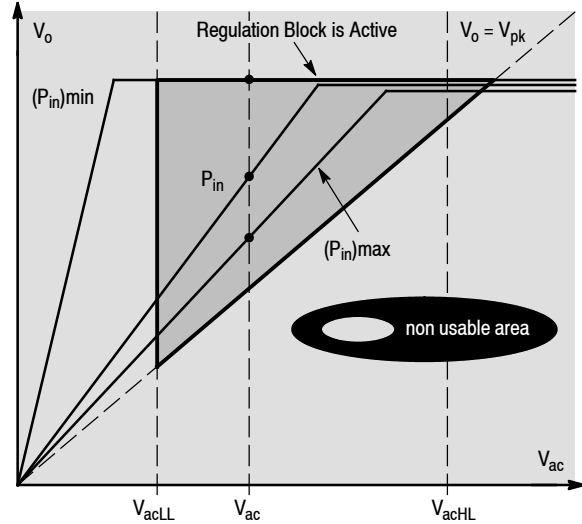


Figure 35. Follower Boost Output Voltage

Mode Selection

The operation mode is simply selected by adjusting the oscillator capacitor value. As shown in Figure 35, the output voltage first has an increasing linear characteristic versus the ac line magnitude and then is clamped down to the regulation value. In the traditional mode, the linear area must be rejected. This is achieved by dimensioning the oscillator capacitor so that the boost can deliver the maximum power while the output voltage equals its regulation level and this, whatever the given input voltage. Practically, that means that whatever the power and input voltage conditions are, the follower boost would generate output voltages values higher than the regulation level, if there was no regulation block.

In other words, if  $(V_o)_{regL}$  is the low output regulation level:

$$(V_o)_{regL} \leq \frac{R_o}{2} \times \sqrt{\frac{C_T + C_{int}}{K_{osc} \times L_p \times (P_{in})_{max}}} \times V_{pk}$$

Consequently,

$$C_T \geq -C_{int} + \frac{4 \times K_{osc} \times L_p \times (P_{in})_{max} \times (V_o)_{regL}^2}{R_o^2 \times V_{pk}^2}$$

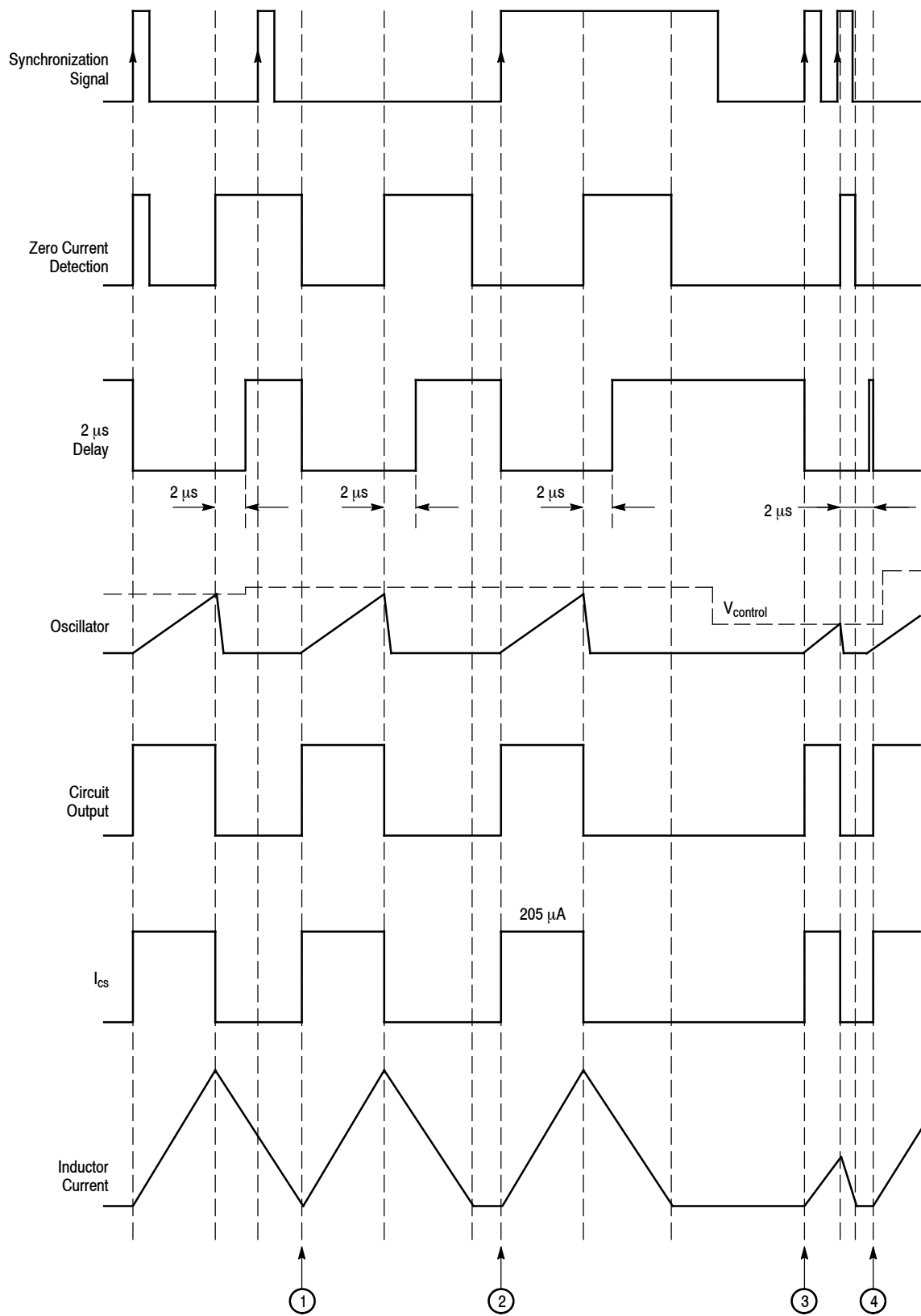
Using  $I_{regL}$  (regulation block current reference), this equation can be simplified as follows:

$$C_T \geq -C_{int} + \frac{4 \times K_{osc} \times L_p \times (P_{in})_{max} \times I_{regL}^2}{V_{pk}^2}$$

In the Follower Boost case, the oscillator capacitor must be chosen so that the wished characteristics are obtained.

Consequently, the simple choice of the oscillator capacitor enables the mode selection.

# MC33260



case no. 1: the turn on is delayed by the Zero Current Detection  
 cases no. 2 and no. 3: the turn on is delayed by the synchronization signal  
 case no. 4: the turn on is delayed by the minimum off-time (2 μs)

**Figure 36. Typical Waveforms**



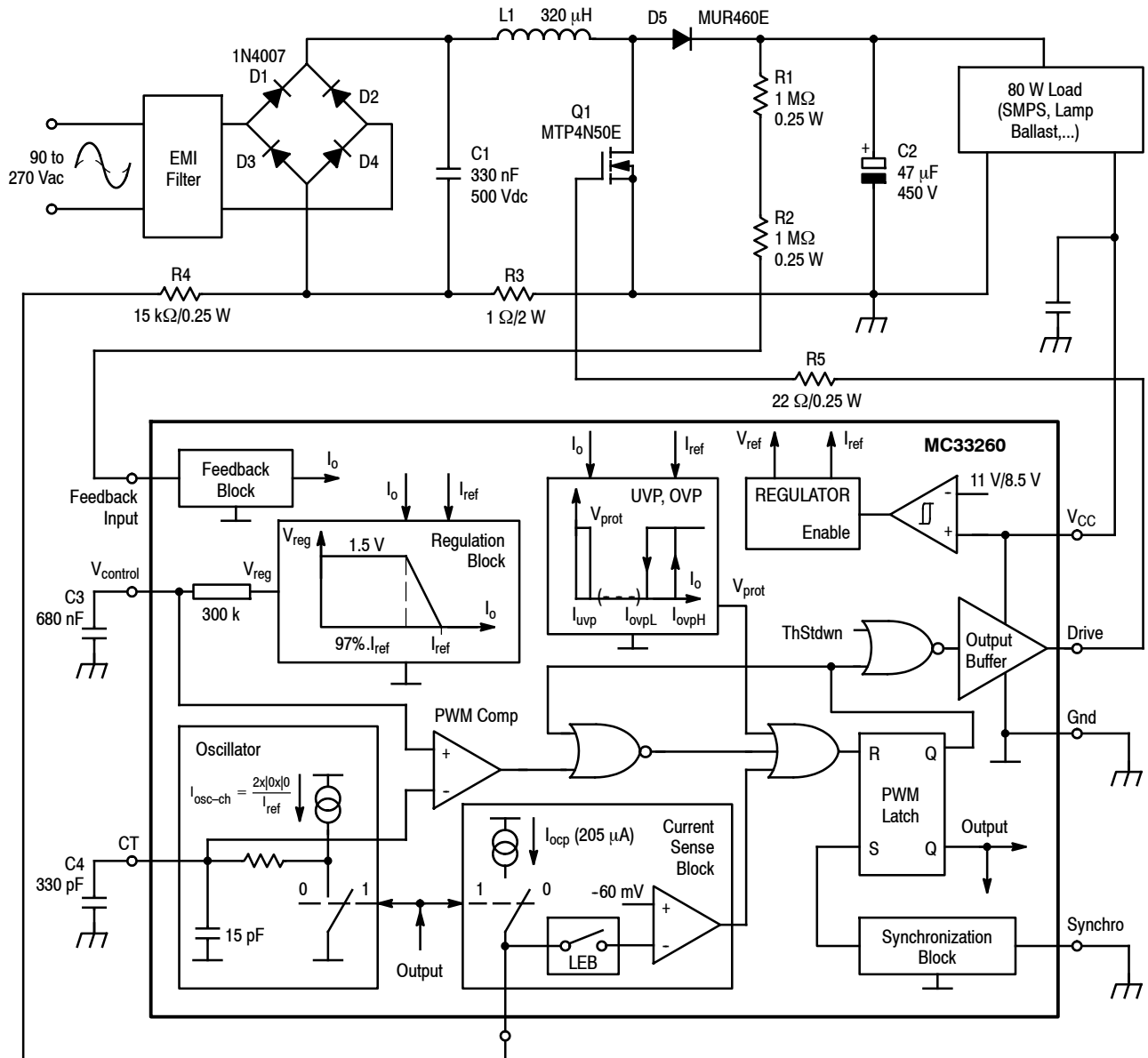
MAIN DESIGN EQUATIONS (Note 3)

rms Input Current ( $I_{ac}$ ) $I_{ac} = \frac{P_o}{\eta \times V_{ac}}$	$\eta$ (preconverter efficiency) is generally in the range of 90 - 95%.
Maximum Inductor Peak Current ( $(I_{pk})_{max}$ ): $(I_{pk})_{max} = \frac{2 \times \sqrt{2} \times (P_o)_{max}}{\eta \times V_{acLL}}$	$(I_{pk})_{max}$ is the maximum inductor current.
Output Voltage Peak to Peak 100Hz (120Hz) Ripple ( $(\Delta V_o)_{pk-pk}$ ): $(\Delta V_o)_{pk-pk} = \frac{P_o}{2\pi \times f_{ac} \times C_o \times V_o}$	$f_{ac}$ is the ac line frequency (50 or 60Hz).
Inductor Value ( $L_p$ ): $L_p = \frac{2 \times t \times \left( \frac{V_o}{\sqrt{2}} - V_{acLL} \right) \times V_{acLL}^2}{V_o \times V_{acLL} \times (I_{pk})_{max}}$	$t$ is the maximum switching period. ( $t = 40 \mu s$ ) for universal mains operation and ( $t = 20 \mu s$ ) for narrow range are generally used.
Maximum Power MOSFET Conduction Losses ( $(P_{on})_{max}$ ): $(P_{on})_{max} \approx \frac{1}{3} \times (R_{ds})_{on} \times (I_{pk})_{max}^2 \times \left[ 1 - \frac{1.2 \times V_{acLL}}{V_o} \right]$	$(R_{ds})_{on}$ is the MOSFET drain source on-time resistor. In Follower Boost, the ratio ( $V_{acLL}/V_o$ ) is higher. The on-time MOSFET losses are then reduced.
Maximum Average Diode Current ( $I_d$ ): $(I_d)_{max} = \frac{(P_o)_{max}}{(V_o)_{min}}$	The Average Diode Current depends on the power and on the output voltage.
Current Sense Resistor Losses ( $pR_{cs}$ ): $pR_{cs} = \frac{1}{6} \times (R_{ds})_{on} \times (I_{pk})_{max}^2$	This formula indicates the required dissipation capability for $R_{cs}$ (current sense resistor).
Over Current Protection Resistor ( $R_{OCP}$ ): $R_{OCP} \approx \frac{R_{cs} \times (I_{pk})_{max}}{0.205} \quad (k\Omega)$	The overcurrent threshold is adjusted by $R_{OCP}$ at a given $R_{cs}$ . $R_{cs}$ can be a preconverter inrush resistor.
Oscillator External Capacitor Value ( $C_T$ ): - Traditional Operation $C_T \geq -C_{int} + \frac{2 \times K_{osc} \times L_p \times (P_{in})_{max} \times I_{regL}^2}{V_{ac}^2}$ - Follower Boost: $V_o = \frac{R_o}{2} \times \sqrt{\frac{C_T + C_{int}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$	The Follower Boost characteristic is adjusted by the $C_T$ choice. The Traditional Mode is also selected by $C_T$ . $C_{int}$ is the oscillator pin internal capacitor.
Feedback Resistor ( $R_o$ ): $R_o = \frac{(V_o)_{reg} - V_{FB}}{I_{regH}} \approx \frac{V_o}{200} \quad (M\Omega)$	The output voltage regulation level is adjusted by $R_o$ .

3. The preconverter design requires the following characteristics specification:

- $(V_o)_{reg}$ : desired output voltage regulation level
- $(\Delta V_o)_{pk-pk}$ : admissible output peak to peak ripple voltage
- $P_o$ : desired output power
- $V_{ac}$ : ac rms operating line voltage
- $V_{acLL}$ : minimum ac rms operating line voltage
- $V_{FB}$ : Feedback Pin voltage

# MC33260



L1: Coilcraft N2881 - A (primary: 62 turns of # 22 AWG - Secondary: 5 turns of # 22 AWG Core: Coilcraft PT2510, EE 25 Gap: 0.072" total for a primary inductance (Lp) of 320  $\mu$ H)

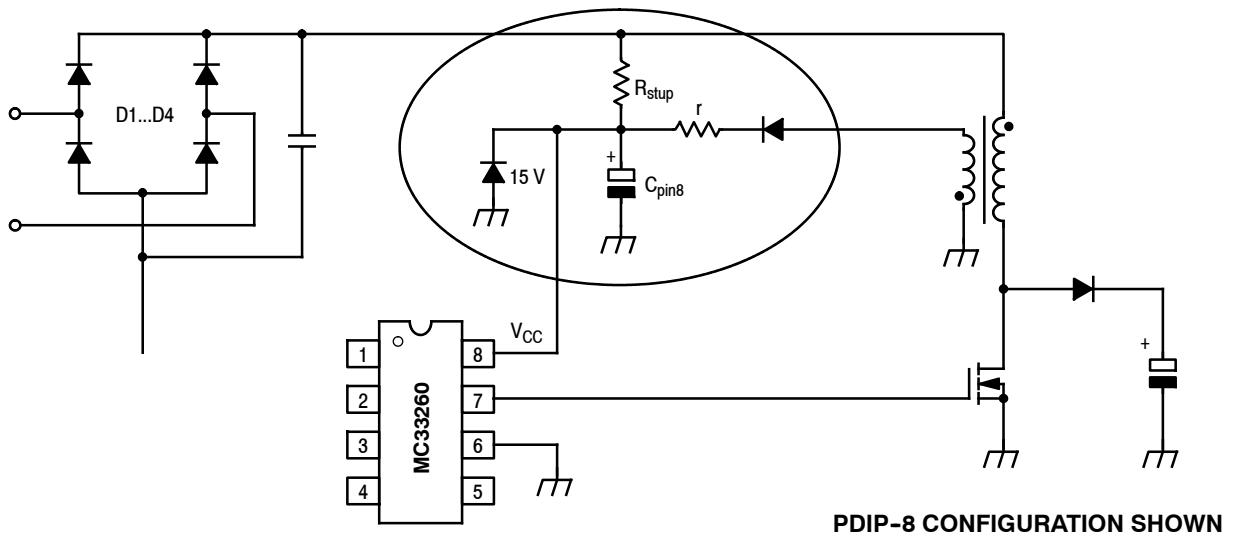
**Figure 37. 80 W Wide Mains Power Factor Corrector**

### POWER FACTOR CONTROLLER TEST DATA\*

AC Line Input										DC Output				
V <sub>rms</sub> (V)	P <sub>in</sub> (W)	PF (-)	I <sub>fund</sub> (mA)	Current Harmonic Distortion (% I <sub>fund</sub> )						V <sub>o</sub> (V)	$\Delta$ V <sub>o</sub> (V)	I <sub>o</sub> (mA)	P <sub>o</sub> (W)	$\eta$ (%)
				THD	H2	H3	H5	H7	H9					
90	88.2	0.991	990	8.1	0.07	5.9	4.3	1.5	1.7	181	31.2	440	79.6	90.2
110	86.3	0.996	782	7.0	0.05	2.7	5.7	1.1	0.8	222	26.4	360	79.9	92.6
135	85.2	0.995	642	8.2	0.03	1.5	6.8	1.1	1.5	265	20.8	300	79.5	93.3
180	87.0	0.994	480	9.5	0.16	4.0	6.5	3.1	4.0	360	16.0	225	81.0	93.1
220	84.7	0.982	385	15	0.5	8.4	7.8	5.3	1.9	379	14.0	210	79.6	94.4
240	85.3	0.975	359	16.5	0.7	9.0	7.8	7.4	3.8	384	14.0	210	80.6	94.5
260	84.0	0.967	330	18.8	0.7	11.0	7.0	9.0	4.0	392	13.2	205	80.4	95.7

\*Measurements performed using Voltech PM1200 ac power analysis.

## MC33260



**Figure 38. Circuit Supply Voltage**

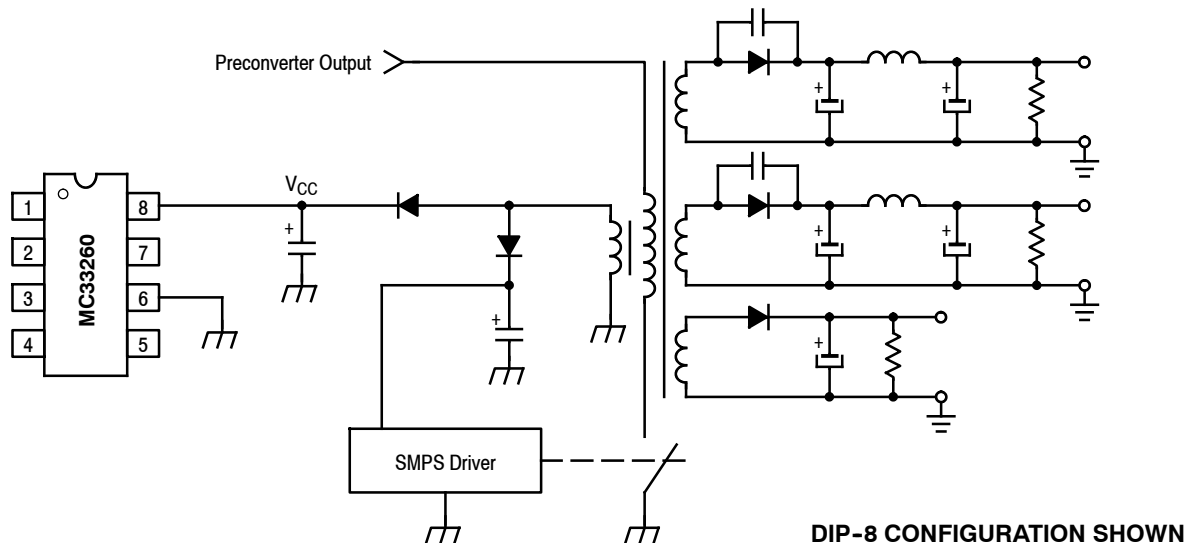
### MC33260 V<sub>CC</sub> SUPPLY VOLTAGE

In some applications, the arrangement shown in Figure 38 must be implemented to supply the circuit. A startup resistor is connected between the rectified voltage (or one-half wave) to charge the MC33260 V<sub>CC</sub> up to its startup threshold (11 V typically). The MC33260 turns on and the V<sub>CC</sub> capacitor (C<sub>pin8</sub>) starts to be charged by the PFC transformer auxiliary winding. A resistor, r (in the range of 22 Ω) and a 15 V Zener should be added to protect the circuit from excessive voltages.

When the PFC preconverter is loaded by an SMPS, the MC33260 should preferably be supplied by the SMPS itself. In this configuration, the SMPS starts first and the PFC gets active when the MC33260 V<sub>CC</sub> supplied by the power supply, exceeds the device startup level. With this configuration, the PFC preconverter doesn't require any auxiliary winding and finally a simple coil can be used.

### PCB LAYOUT

The connections of the oscillator and V<sub>control</sub> capacitors should be as short as possible.



**Figure 39. Preconverter Loaded by a Flyback SMPS: MC33260 V<sub>CC</sub> Supply**

# MC33260

## ORDERING INFORMATION

Device	Package	Shipping†
MC33260PG	PDIP-8 (Pb-Free)	50 Units / Rail
MC33260DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33260DR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

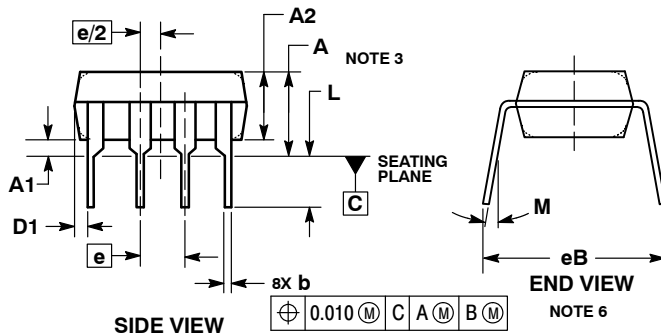
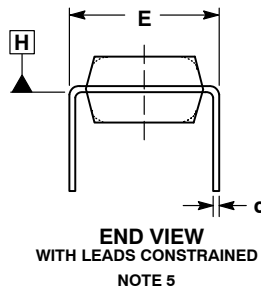
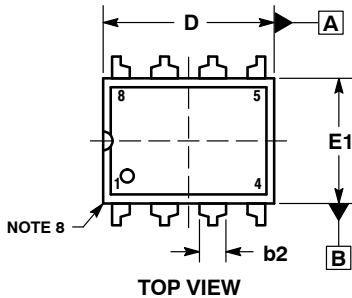
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SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015

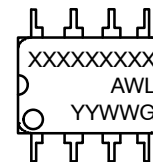


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:  
PIN 1. AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

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DESCRIPTION:	PDIP-8	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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