ISL8112

High Light-Load Efficiency, Dual-Output, Main Power Supply Controllers

FN6396
Rev 1.00
August 10, 2010

ISL8112 is a dual-output Synchronous Buck controller with 2A integrated driver. It features high light load efficiency which is especially preferred in systems concerned with high efficiency in wide load range, like the battery powered system. ISL8112 includes two constant on-time PWM controllers. Either of the two outputs can operate in output fixed mode or adjustable mode. In fixed mode, one output can be 5V or 3.3V and the other can output 1.5V or 1.05V. In output adjustable mode, one output can be 0.7V to 5.5V, and the other output can range from 0V to 2.5V (sensing output voltage directly) or up to 5V (using resistor divider voltage for voltage sensing). This device also features a linear regulator providing 3.3V/5V, or adjustable from 0.7V to 4.5V via LDOREF. The linear regulator provides up to 100mA output current with automatic linear-regulator bootstrapping to the BYP input. When in switch over, the LDO output can source up to 200mA. ISL8112 includes on-board power-up sequencing, the power-good (PGOOD_) outputs, digital soft-start, and internal soft-stop output discharge that prevents negative voltages on shutdown.

ISL8112 is implemented with constant on-time PWM control scheme which need no sense resistors and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic pulse-skipping mode maintains the switching frequency above 25kHz, eliminating undesired audible noises in low frequency operation at light load. Other features include pulse skipping which maximizes efficiency in light-load applications, and fixed-frequency PWM mode which reduces RF interference in sensitive applications.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8112IRZ*	ISL8112 IRZ	-40 to +100	32 Ld QFN (Pb-free)	L32.5x5B

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

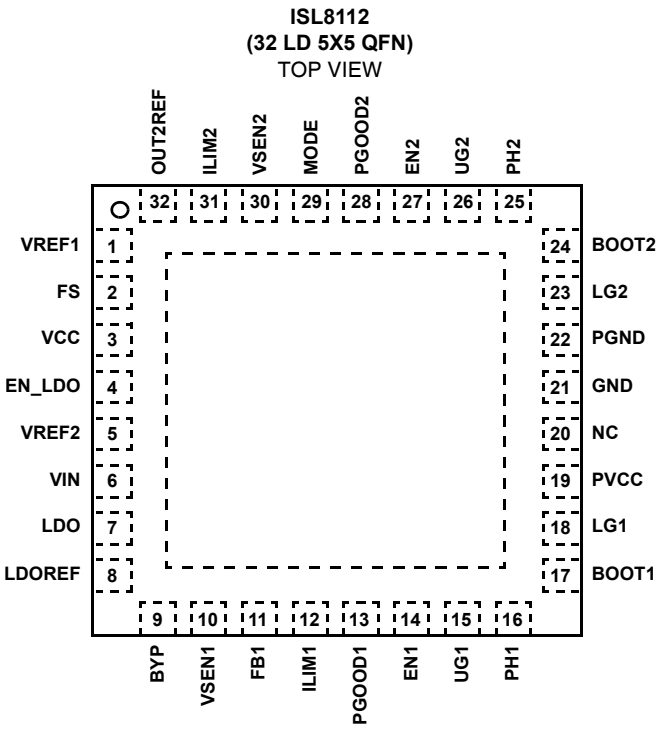
Features

- Wide Input Voltage Range 5.5V to 25V
- Constant ON-TIME Control with 100ns Load-Step Response
- Dual Fixed Outputs of 1.05V (3.3V) and 1.5V (5.0V), or Adjustable Outputs of 0.7V to 5.5V (SMPS1) and 0V to 2.5V/5V (SMPS2), ±1.5% Accuracy
- Adjustable Switching Frequency: 400/500kHz, 300/400kHz, 200/300kHz
- Very High Light Load Efficiency (Skip Mode)
- 5mW Quiescent Power Dissipation
- ±1.5% (LDO): 100mA, 200mA (Switch Over)
- 3.3V Reference Voltage ±2.0%: 5mA
- 2.0V Reference Voltage ±1.0%: 50µA
- Temperature Compensated $r_{DS(ON)}$ Current Sensing
- Programmable Current Limit with Foldback Capability
- Selectable PWM, Skip or Ultrasonic Mode
- Independent PGOOD1 and PGOOD2 Comparators
- Soft-Start with Pre-Biased Output and Soft-Stop
- 1.7ms Digital Soft-Start and Independent Shutdown
- Independent ENABLE
- Thermal Shutdown
- Extremely Low Components Count
- Pb-Free Available (RoHS Compliant)

Applications

- Power Supply for Telecom/Datacom and POL
- System Requiring High Efficiency in Wide Load Range
- Compact Design with Minimum Components Count
- PDAs and Mobile Communication Devices
- 3- and 4-Cell Li+ Battery-Powered Devices
- DDR1, DDR2, and DDR3 Applications

Pinout


ISL8112
(32 LD 5X5 QFN)
TOP VIEW
OUT2REF
ILIM2
VSEN2
MODE
PGOOD2
EN2
UG2
PH2
32
31
30
29
28
27
26
25
VREF1
1
FS
2
VCC
3
EN_LDO
4
VREF2
5
VIN
6
LDO
7
LDOREF
8
24
BOOT2
23
LG2
22
PGND
21
GND
20
NC
19
PVCC
18
LG1
17
BOOT1
9
10
11
12
13
14
15
16
BYP
VSEN1
FB1
ILIM1
PGOOD1
EN1
UG1
PH1

Absolute Voltage Ratings

VIN, EN_LDO to GND . . . . . -0.3V to +27V
BOOT_ to GND . . . . . -0.3V to +33V
BOOT_ to PH_ . . . . . -0.3V to +6V
VCC, EN_, MODE, FS,
PVCC, PGOOD_ to GND . . . . . -0.3V to +6V
LDO, FB1, OUT2REF, LDOREF to GND . . . . -0.3V to (VCC+0.3V)
VSEN_, VREF2, VREF1 to GND . . . . . -0.3V to (VCC+0.3V
UG_ to PH_ . . . . . -0.3V to (PVCC + 0.3V)
ILIM_ to GND . . . . . -0.3V to (VCC + 0.3V)
LG_, BYP to GND . . . . . -0.3V to (PVCC + 0.3V)
PGND to GND . . . . . -0.3V to + 0.3V
LDO, VREF1, VREF2 Short Circuit to GND . . . . . Continuous
VCC Short Circuit to GND 1s
LDO Current (Internal Regulator) Continuous 100mA
LDO Current (Switched Over to VSEN1) Continuous . . . . . +200mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN (Notes 1, 2)	32	3.0

Operating Temperature Range . . . . . -40°C to +100°C
Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Circuit of Figure 17, and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, VIN = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
MAIN SMPS CONTROLLERS					
V_{IN} Input Voltage Range	LDO in regulation	5.5		25	V
	V_{IN} = LDO, VSEN1 < 4.43V	4.5		5.5	V
3.3V Output Voltage in Fixed Mode	V_{IN} = 5.5V to 25V, OUT2REF > (VCC - 1V), MODE = 5V	3.285	3.330	3.375	V
1.05V Output Voltage in Fixed Mode	V_{IN} = 5.5V to 25V, 3.0 < OUT2REF < (VCC - 1.1V), MODE = 5V	1.038	1.05	1.062	V
1.5V Output Voltage in Fixed Mode	V_{IN}= 5.5V to 25V, FB1 = VCC, MODE = 5V	1.482	1.500	1.518	V
5V Output Voltage in Fixed Mode	V_{IN}= 5.5V to 25V, FB1 = GND, MODE = 5V	4.975	5.050	5.125	V
FB1 in Output Adjustable Mode	V_{IN} = 5.5V to 25V	0.693	0.700	0.707	V
OUT2REF in Output Adjustable Mode	V_{IN} = 5.5V to 25V	0.7		2.50	V
SMPS1 Output Voltage Adjust Range	SMPS1	0.70		5.50	V
SMPS2 Output Voltage Adjust Range	SMPS2	0.50		2.50	V
SMPS2 Output Voltage Accuracy (Referred for OUT2REF)	OUT2REF = 0.7V to 2.5V, MODE = VCC	-1.0		1.0	%
DC Load Regulation	Either SMPS, MODE = VCC, 0A to 5A		-0.1		%
	Either SMPS, MODE = VREF1, 0A to 5A		-1.7		%
	Either SMPS, MODE = GND, 0A to 5A		-1.5		%
Line Regulation	Either SMPS, 6V < V_{IN} < 24V		0.005		%/V
Current-Limit Current Source	Temperature = +25°C	4.75	5	5.25	µA
ILIM_ Adjustment Range		0.2		2	V
Current-Limit Threshold (Positive, Default)	ILIM_ = VCC, GND - PH_ (No temperature compensation)	93	100	107	mV

Electrical Specifications Circuit of Figure 17, and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, VIN = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	CONDITIONS		MIN (Note 3)	TYP	MAX (Note 3)	UNITS
Current-Limit Threshold (Positive, Adjustable)	GND - PH_	VILIM_ = 0.5V	40	50	60	mV
		VILIM_ = 1V	93	100	107	mV
		VILIM_ = 2V	185	200	215	mV
Zero-Current Threshold	MODE = GND, VREF1, or OPEN, GND - PH_			3		mV
Current-Limit Threshold (Negative, Default)	MODE = VCC, GND - PH_			-120		mV
Soft-Start Ramp Time	Zero to full limit			1.7		ms
Operating Frequency	(VFS = GND), MODE = VCC	SMPS 1		400		kHz
		SMPS 2		500		kHz
	(VFS = VREF1 or OPEN), MODE = VCC	SMPS 1		400		kHz
		SMPS 2		300		kHz
	(VFS = VCC), MODE = VCC	SMPS 1		200		kHz
		SMPS 2		300		kHz
On-Time Pulse Width	VFS = GND (400kHz/500kHz)	VSEN1 = 5.00V	0.895	1.052	1.209	µs
		VSEN2 = 3.33V	0.475	0.555	0.635	µs
	VFS = VREF1 or OPEN (400kHz/300kHz)	VSEN1 = 5.05V	0.895	1.052	1.209	µs
		VSEN2 = 3.33V	0.833	0.925	1.017	µs
	VFS = VCC (200kHz/300kHz)	VSEN1 = 5.05V	1.895	2.105	2.315	µs
		VSEN2 = 3.33V	0.833	0.925	1.017	µs
Minimum Off-Time			200	300	400	ns
Maximum Duty Cycle	VFS = GND	VSEN1 = 5.05V		88		%
		VSEN2 = 3.33V		85		%
	VFS = VREF1 or OPEN	VSEN1 = 5.05V		88		%
		VSEN2 = 3.33V		91		%
	VFS = VCC	VSEN1 = 5.05V		94		%
		VSEN2 = 3.33V		91		%
Ultrasonic SKIP Operating Frequency	MODE = VREF1 or OPEN		25	37		kHz
INTERNAL REGULATOR AND REFERENCE						
LDO Output Voltage	BYP = GND, 5.5V < V_{IN} < 25V, LDOREF < 0.3V, 0 < ILDO < 100mA		4.925	5.000	5.075	V
LDO Output Voltage	BYP = GND, 5.5V < V_{IN} < 25V, LDOREF > (VCC-1V), 0 < ILDO < 100mA		3.250	3.300	3.350	V
LDO Output in Adjustable Mode	V_{IN} = 5.5V to 25V, V_{LDO} = 2 x V_{LDOREF}		0.7		4.5	V
LDO Output Accuracy in Adjustable Mode	V_{IN} = 5.5V to 25V, V_{LDOREF} = 0.35V to 0.5V				±2	%
	V_{IN} = 5.5V to 25V, V_{LDOREF} = 0.5V to 2.25V				±1.5	%
LDOREF Input Range	V_{LDO} = 2 x V_{LDOREF}		0.35		2.25	V
LDO Output Current	BYP = GND, V_{IN} = 5.5V to 25V (Note 4)				100	mA
LDO Output Current During Switch Over	BYP = 5V, V_{IN} = 5.5V to 25V, LDOREF < 0.3V				200	mA
LDO Output Current During Switch Over to 3.3V	BYP = 3.3V, V_{IN} = 5.5V to 25V, LDOREF > (VCC-1V)				100	mA
LDO Short-Circuit Current	LDO = GND, BYP = GND			200	400	mA
Undervoltage-Lockout Fault Threshold	Rising edge of PVCC Falling edge of PVCC		 3.9	4.35 4.05	4.5	V

Electrical Specifications Circuit of Figure 17, and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, VIN = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
LDO 5V Bootstrap Switch Threshold to BYP	Rising edge at BYP regulation point LDOREF = GND	4.53	4.68	4.83	V
LDO 3.3V Bootstrap Switch Threshold to BYP	Rising edge at BYP regulation point LDOREF = VCC	3.0	3.1	3.2	V
LDO 5V Bootstrap Switch Equivalent Resistance	LDO to BYP, BYP = 5V, LDOREF > (VCC-1V) (Note 4)		0.7	1.5	Ω
LDO 3.3V Bootstrap Switch Equivalent Resistance	LDO to BYP, BYP = 3.3V, LDOREF < 0.3V (Note 4)		1.5	3.0	Ω
VREF2 Output Voltage	No external load, VCC > 4.5V	3.235	3.300	3.365	V
	No external load, VCC < 4.0V	3.220	3.300	3.380	V
VREF2 Load Regulation	0 < ILOAD < 5mA		10		mV
VREF2 Current Limit	VREF2 = GND		10	17	mA
VREF1 Output Voltage	No external load	1.980	2.000	2.020	V
VREF1 Load Regulation	0 < ILOAD < 50µA		10		mV
VREF1 Sink Current	VREF1 in regulation	10			µA
V_{IN} Operating Supply Current	Both SMPSs on, FB1 = MODE = GND, OUT2REF = VCC VSEN1 = BYP = 5.3V, VSEN2 = 3.5V		25	50	µA
V_{IN} Standby Supply Current	V_{IN} = 5.5V to 25V, both SMPSs off, EN_LDO = VCC		180	250	µA
V_{IN} Shutdown Supply Current	V_{IN} = 4.5V to 25V, EN1=EN2=EN_LDO=0V		20	30	µA
Quiescent Power Consumption	Both SMPSs on, FB1 = MODE = GND, OUT2REF = VCC, VSEN1 = BYP = 5.3V, VSEN2 = 3.5V		5	7	mW
FAULT DETECTION					
Overvoltage Trip Threshold	FB1 with respect to nominal regulation point	+8	+11	+14	%
	OUT2REF with respect to nominal regulation point	+12	+16	+20	%
Overvoltage Fault Propagation Delay	FB1 or OUT2REF delay with 50mV overdrive		10		µs
PGOOD_ Threshold	FB1 or OUT2REF with respect to nominal output, falling edge, typical hysteresis = 1%	-12	-9	-6	%
PGOOD_ Propagation Delay	Falling edge, 50mV overdrive		10		µs
PGOOD_ Output Low Voltage	ISINK = 4mA			0.2	V
PGOOD_ Leakage Current	High state, forced to 5.5V			1	µA
Thermal-Shutdown Threshold			+150		°C
Output Undervoltage Shutdown Threshold	FB1 or OUT2REF with respect to nominal output voltage	65	70	75	%
Output Undervoltage Shutdown Blanking Time	From EN_ signal	10	20	30	ms
INPUTS AND OUTPUTS					
FB1 Input Voltage	Low level			0.3	V
	High level	VCC-1.0			V
OUT2REF Input Voltage	VSEN2 Dynamic Range, VSEN2= $V_{OUT2REF}$	0.5		2.50	V
	Fixed VSEN2 = 1.05V	3.0		VCC-1.1	V
	Fixed VSEN2 = 3.3V	VCC-1.0			V

Electrical Specifications Circuit of Figure 17, and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, VIN = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
LDOREF Input Voltage	Fixed LDO = 5V			0.30	V
	VSEN2 Dynamic Range, V_{LDO} = 2 x V_{LDOREF}	0.35		2.25	V
	Fixed LDO = 3.3V	VCC-1.0			V
MODE Input Voltage	Low level (SKIP)			0.8	V
	Float level (ULTRASONIC SKIP)	1.7		2.3	V
	High level (PWM)	2.4			V
FS Input Voltage	Low level			0.8	V
	Float level	1.7		2.3	V
	High level	2.4			V
EN1, EN2 Input Voltage	Clear fault level/SMPS off level			0.8	V
	Delay start level	1.7		2.3	V
	SMPS on level	2.4			V
EN_LDO Input Voltage	Rising edge	1.2	1.6	2.0	V
	Falling edge	0.94	1.00	1.06	V
Input Leakage Current	VFS = 0 or 5V	-1		+1	µA
	VEN_ = VEN_LDO = 0V or 5V	-0.1		+0.1	µA
	VMODE = 0V or 5V	-1		+1	µA
	VFB1 = 0V or 5V	-0.2		+0.2	µA
	VREFIN = 0V or 2.5V	-0.2		+0.2	µA
	VLDOREF = 0V or 2.75V	-0.2		+0.2	µA
INTERNAL BOOT DIODE					
V_D Forward Voltage	PVCC - V_{BOOT}, I_F = 10mA		0.65	0.8	V
$I_{BOOT\_LEAKAGE}$ Leakage Current	V_{BOOT} = 30V, PH = 25V, PVCC = 5V			500	nA
MOSFET DRIVERS					
UG_ Gate-Driver Sink/Source Current	UG1, UG2 forced to 2V		2		A
LG_ Gate-Driver Source Current	LG1 (source), LG2 (source), forced to 2V		1.7		A
LG_ Gate-Driver Sink Current	LG1 (sink), LG2 (sink), forced to 2V		3.3		A
UG_ Gate-Driver On-Resistance	BST_ - PH_ forced to 5V (Note 4)		1.5	4.0	Ω
LG_ Gate-Driver On-Resistance	LG_, high state (pull-up) (Note 4)		2.2	5.0	Ω
	LG_, low state (pull-down) (Note 4)		0.6	1.5	Ω
Dead Time	LG_ Rising	15	20	35	ns
	UG_ Rising	20	30	50	ns
VSEN1, VSEN2 Discharge On Resistance			25	40	Ω

NOTES:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
4. Limits established by characterization and are not production tested.

Pin Descriptions

PIN	NAME	FUNCTION
1	VREF1	2V Reference Output. Bypass to GND with a 0.1µF (min) capacitor. VREF1 can source up to 50µA for external loads. Loading VREF1 degrades FB and output accuracy according to the VREF1 load-regulation error.
2	FS	Frequency Select Input. Connect to GND for 400kHz/500kHz operation. Connect to VREF1 (or leave OPEN) for 400kHz/300kHz operation. Connect to VCC for 200kHz/300kHz operation (5V/3.3V SMPS switching frequencies, respectively).
3	VCC	Analog Supply Voltage for PWM Core. Bypass to GND with a 1µF ceramic capacitor.
4	EN_LDO	LDO Enable Input. The LDO is enabled if EN_LDO is within logic high level and VIN is higher than POR threshold. The LDO is disabled if EN_LDO is less than the logic low level.
5	VREF2	3.3V Reference Output. VREF2 can source up to 5mA for external loads. Bypass to GND with a 0.01µF capacitor if loaded. Leave open if there is no load.
6	VIN	Power-Supply Input. VIN is used for the constant-on-time PWM on-time one-shot circuits. VIN is also used to power the linear regulators. The linear regulators are powered by SMPS1 if VSEN1 is set greater than 4.78V and BYP is tied to VSEN1. Connect VIN to the battery input and bypass with a 1µF capacitor.
7	LDO	Linear-Regulator Output. LDO can provide a total of 100mA external loads. The LDO regulate at 5V If LDOREF is connected to GND. When the LDO is set at 5V and BYP is within 5V switch over threshold, the internal regulator shuts down and the LDO output pin connects to BYP through a 0.7Ω switch. The LDO regulate at 3.3V if LDOREF is connected to VCC. When the LDO is set at 3.3V and BYP is within 3.3V switch over threshold, the internal regulator shuts down and the LDO output pin connects to BYP through a 1.5Ω switch. Bypass LDO output with a minimum of 4.7µF ceramic.
8	LDOREF	LDO Reference Input. Connect LDOREF to GND for fixed 5V operation. Connect LDOREF to VCC for fixed 3.3V operation. LDOREF can be used to program LDO output voltage from 0.7V to 4.5V. LDO output is two times the voltage of LDOREF. There is no switch over in adjustable mode.
9	BYP	BYP is the switch over source voltage for the LDO when LDOREF connected to GND or VCC. Connect BYP to 5V if LDOREF is tied to GND. Connect BYP to 3.3V if LDOREF is tied to VCC. The BYP is also controlled by EN_LDO. When LDOREFIN is tied to GND, the BYP is not switched over to LDO until SMPS1 finished soft-starting.
10	VSEN1	SMPS1 Output Voltage-Sense Input. Connect to the SMPS1 output. VSEN1 is an input to the Constant on-time-PWM on-time one-shot circuit. It also serves as the SMPS1 feedback input in fixed-voltage mode.
11	FB1	SMPS1 Feedback Input. Connect FB1 to GND for fixed 5V operation. Connect FB1 to VCC for fixed 1.5V operation Connect FB1 to a resistive voltage-divider from VSEN1 to GND to adjust the output from 0.7V to 5.5V.
12	ILIM1	SMPS1 Current-Limit Adjustment. The GND-PH1 current-limit threshold is 1/10th the voltage seen at ILIM1 over a 0.2V to 2V range. There is an internal 5µA current source from VCC to ILIM1. Connect ILIM1 to VREF1 for a fixed 200mV threshold. The logic current limit threshold is default to 100mV value if ILIM1 is higher than VCC - 1V.
13	PGOOD1	SMPS1 Power-Good Open-Drain Output. PGOOD1 is low when the SMPS1 output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD1 is high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD1 is low in shutdown.
14	EN1	SMPS1 Enable Input. The SMPS1 is enabled if EN1 is greater than the logic high level and disabled if EN1 is less than the logic low level. If EN1 is connected to VREF1, the SMPS1 starts after the SMPS2 reaches regulation (delay start). Drive EN1 below 0.8V to clear fault level and reset the fault latches.
15	UG1	High-Side MOSFET Floating Gate-Driver Output for SMPS1. UG1 swings between PH1 and BOOT1.
16	PH1	Inductor Connection for SMPS1. PH1 is the internal lower supply rail for the UG1 high-side gate driver. PH1 is the current-sense input for the SMPS1.
17	BOOT1	Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor according to the typical application circuits (Figure 17 and Figure 18). See “MOSFET Gate Drivers (UG_, LG_)” on page 19.
18	LG1	SMPS1 Synchronous-Rectifier Gate-Drive Output. LG1 swings between GND and PVCC.
19	PVCC	PVCC is the supply voltage for the low-side MOSFET driver LG_. Connect a 5V power source to the PVCC pin (bypass with 1µF MLCC capacitor to PGND if necessary). There is internal 10Ω PFET connecting PVCC to VCC. Make sure that both VCC and PVCC are bypassed with 1µF MLCC capacitors.
20	NC	No connection pin. Externally connect it to ground.
21	GND	Analog Ground for both SMPS_ and LDO. Connect externally to the underside of the exposed pad.
22	PGND	Power Ground for SMPS_ controller. Connect PGND externally to the underside of the exposed pad.

Pin Descriptions (Continued)

PIN	NAME	FUNCTION
23	LG2	SMPS2 Synchronous-Rectifier Gate-Drive Output. LG2 swings between GND and PVCC.
24	BOOT2	Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor according to the typical application circuits (Figure 17 and Figure 18). See “MOSFET Gate Drivers (UG_, LG_)” on page 19.
25	PH2	Inductor Connection for SMPS2. PH2 is the internal lower supply rail for the UG2 high-side gate driver. PH2 is the current-sense input for the SMPS2.
26	UG2	High-Side MOSFET Floating Gate-Driver Output for SMPS2. UG1 swings between PH2 and BOOT2.
27	EN2	SMPS2 Enable Input. The SMPS2 is enabled if EN2 is greater than the logic high level and disabled if EN2 is less than the logic low level. If EN2 is connected to VREF1, the SMPS2 starts after the SMPS1 reaches regulation (delay start). Drive EN2 below 0.8V to clear fault level and reset the fault latches.
28	PGOOD2	SMP2 Power-Good Open-Drain Output. PGOOD2 is low when the SMPS2 output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD2 is high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD2 is low in shutdown.
29	MODE	Low-Noise Mode Control. Connect MODE to GND for normal Idle-Mode (pulse-skipping) operation or to VCC for PWM mode (fixed frequency). Connect to VREF1 or leave floating for ultrasonic skip mode operation.
30	VSEN2	SMPS2 Output Voltage-Sense Input. Connect to the SMPS2 output. VSEN2 is an input to the Constant on-time-PWM on-time one-shot circuit. It also serves as the SMPS2 feedback input in fixed-voltage mode.
31	ILIM2	SMPS2 Current-Limit Adjustment. The GND-PH1 current-limit threshold is 1/10th the voltage seen at ILIM2 over a 0.2V to 2V range. There is an internal 5µA current source from VCC to ILIM2. Connect ILIM2 to VREF1 for a fixed 200mV. The logic current limit threshold is default to 100mV value if ILIM2 is higher than VCC - 1V.
32	OUT2REF	Output voltage control for SMPS2. Connect OUT2REF to VCC for fixed 3.3V. Connect OUT2REF to VREF2 for fixed 1.05V. OUT2REF can be used to program SMPS2 output. VSEN2 equals OUT2REF from 0.5V to 2.50V. SMPS2 output voltage is 0V if OUT2REF < 0.5V.

Typical Performance Curves

Circuit of Figure 17 and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, V_{IN} = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C.

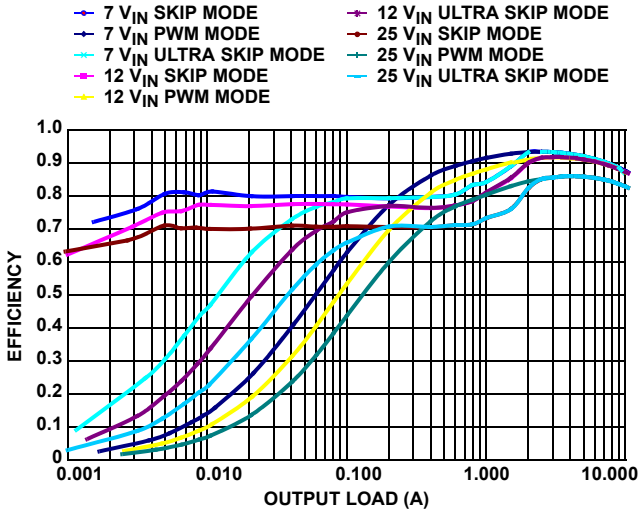


FIGURE 1. V_{OUT2} = 1.05V EFFICIENCY vs LOAD (300kHz)

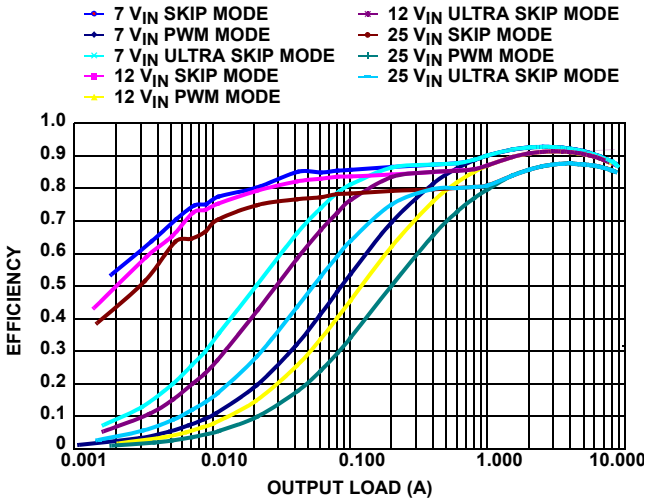


FIGURE 2. V_{OUT1} = 1.5V EFFICIENCY vs LOAD (200kHz)

Typical Performance Curves

Circuit of Figure 17 and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, V_{IN} = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

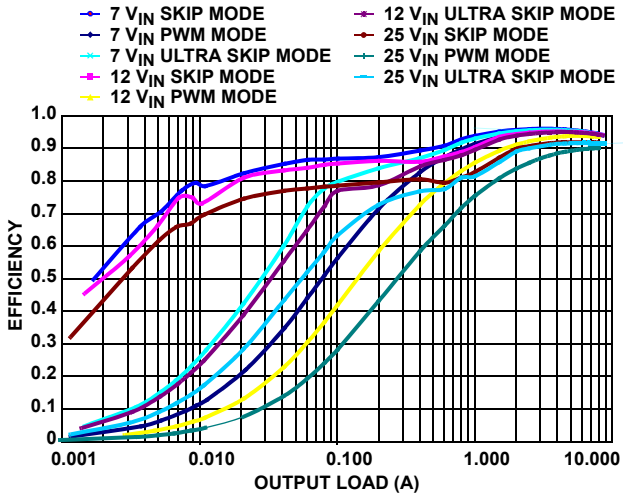


FIGURE 3. V_{OUT2} = 3.3V EFFICIENCY vs LOAD (500kHz)

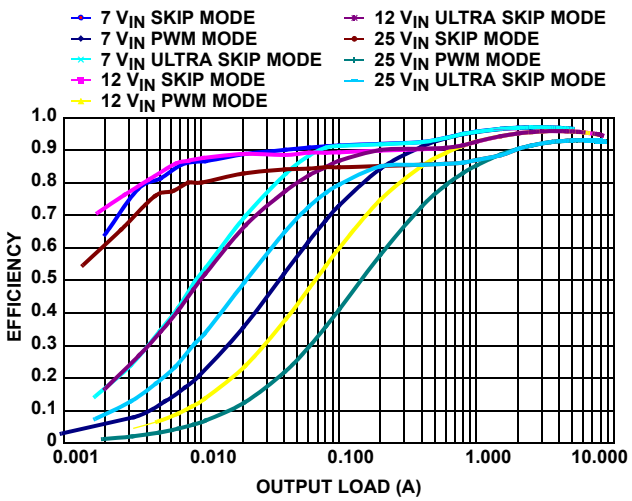


FIGURE 4. V_{OUT1} = 5V EFFICIENCY vs LOAD (400kHz)

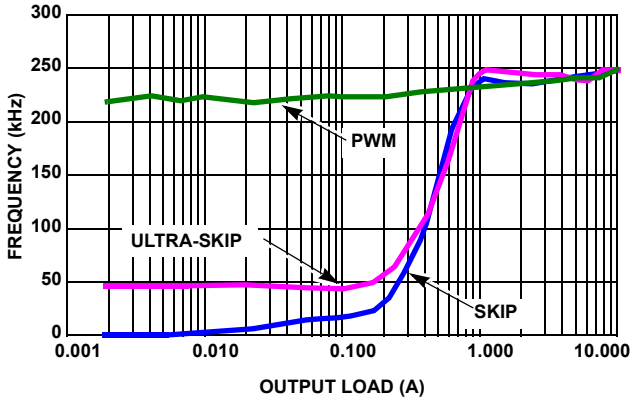


FIGURE 5. V_{OUT2} = 1.05V FREQUENCY vs LOAD

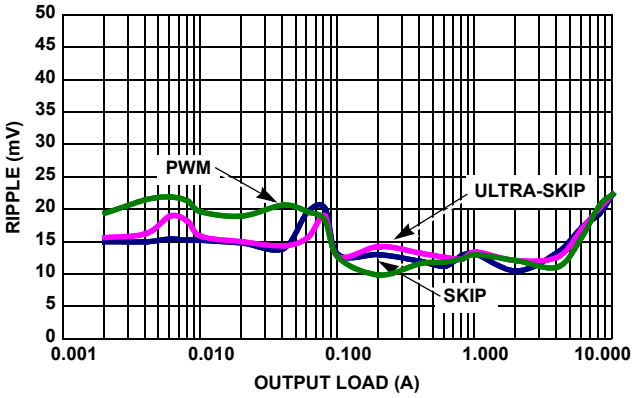


FIGURE 6. V_{OUT2} = 1.05V RIPPLE vs LOAD

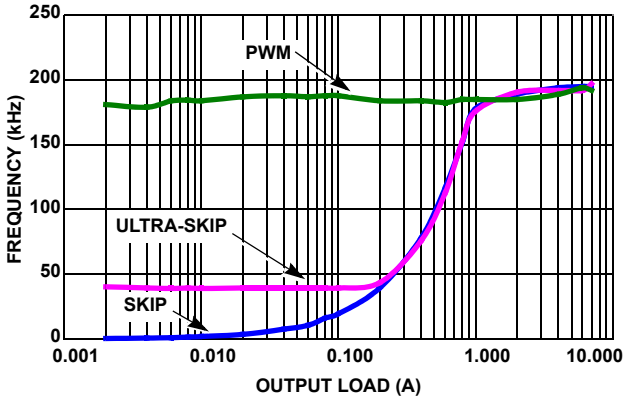


FIGURE 7. V_{OUT1} = 1.5V FREQUENCY vs LOAD

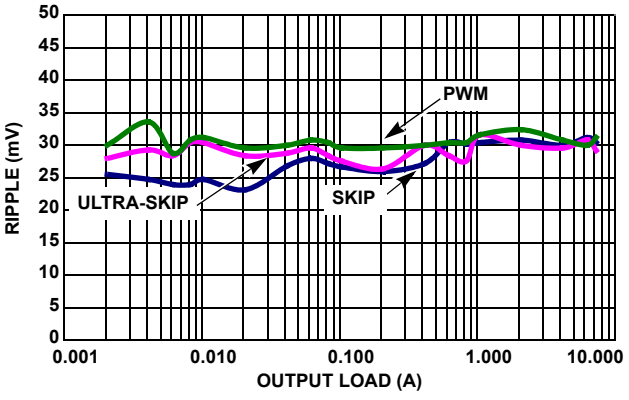


FIGURE 8. V_{OUT1} = 1.5V RIPPLE vs LOAD

Typical Performance Curves

Circuit of Figure 17 and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, V_{IN} = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

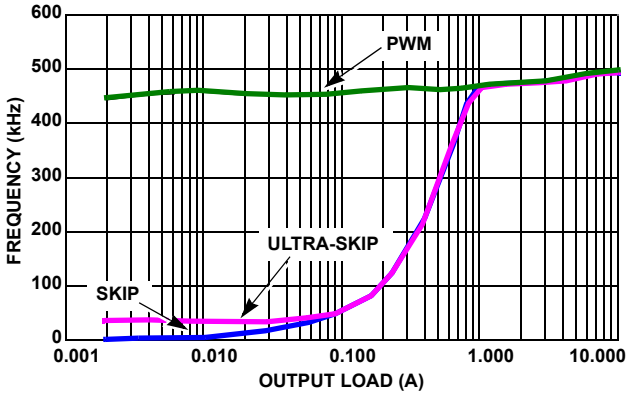


FIGURE 9. V_{OUT2} = 3.3V FREQUENCY vs LOAD

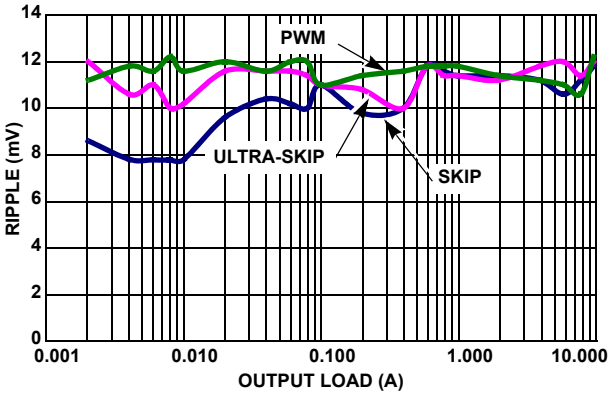


FIGURE 10. V_{OUT2} = 3.3V RIPPLE vs LOAD

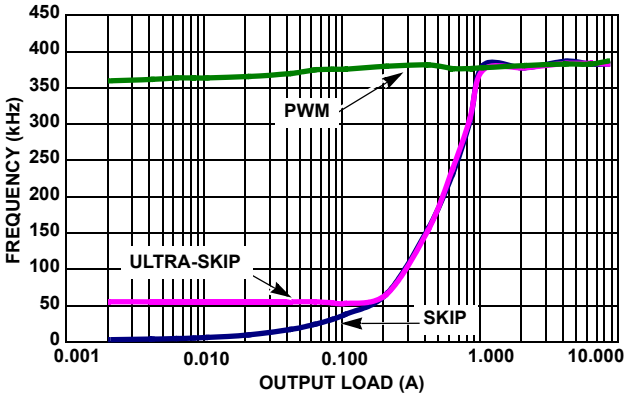


FIGURE 11. V_{OUT1} = 5V FREQUENCY vs LOAD

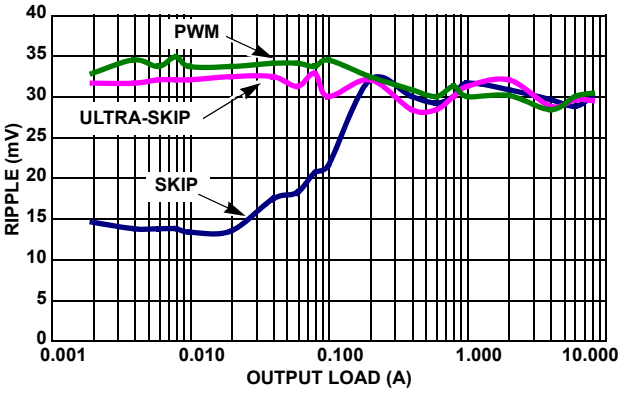


FIGURE 12. V_{OUT1} = 5V RIPPLE vs LOAD

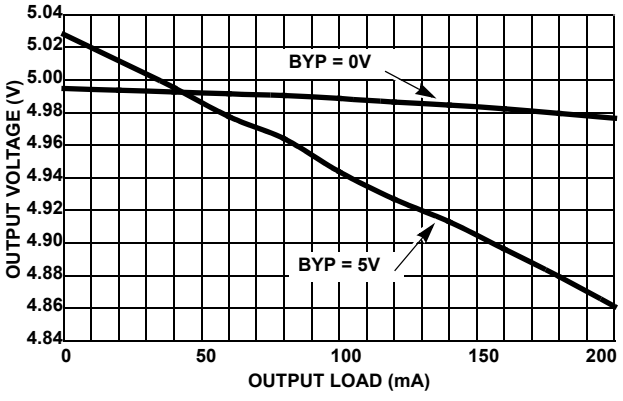


FIGURE 13. LDO OUTPUT 5V vs LOAD

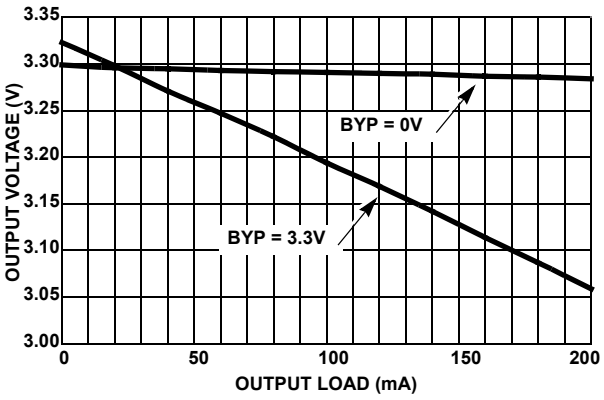


FIGURE 14. LDO OUTPUT 3.3V vs LOAD

Typical Performance Curves

Circuit of Figure 17 and Figure 18, no load on LDO, VSEN1, VSEN2, VREF2, and VREF1, V_{IN} = 12V, EN2 = EN1 = VCC, VBYP = 5V, PVCC = 5V, VEN_LDO = 5V, T_A = -40°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

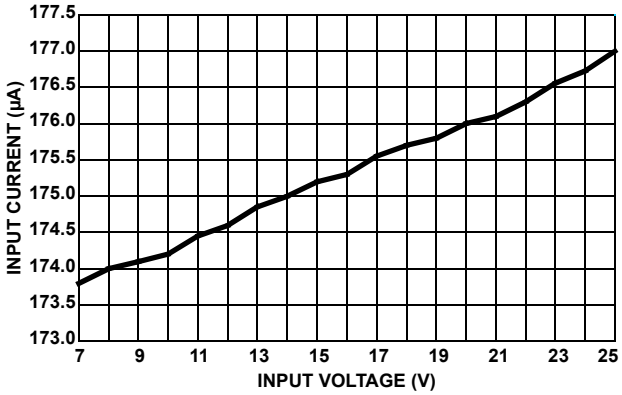


FIGURE 15. STANDBY INPUT CURRENT vs V_{IN} (EN = EN2 = 0, EN_LDO = VCC)

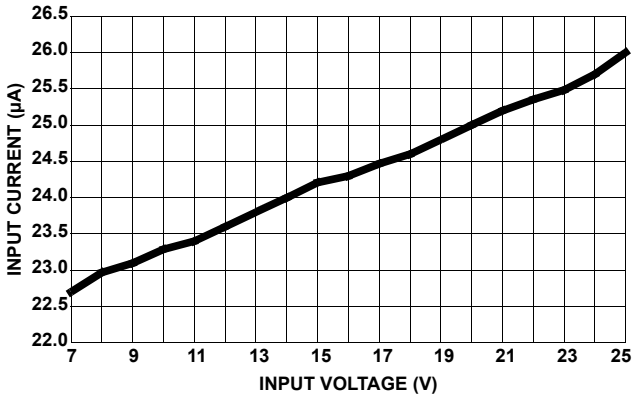


FIGURE 16. SHUTDOWN INPUT CURRENT vs V_{IN} (EN = EN2 = EN_LDO = 0)

Typical Application Circuits

The typical application circuits are shown in Figures 17, 18 and 19. In Figure 17, the power supply system generates 1.25V/5A and dynamic voltage/10A. Figure 18 shows system having1.5V/5A and 1.05V/5A output. The input supply range is 5.5V to 25V. Figure 19 shows system having1.2V/15A and 2.5V/5A output. The input supply range is 5.5V to 25V and 4.5V to 5.5V respectively.

Detailed Description

The ISL8112 dual-buck, BiCMOS, switch-mode power-supply controller generates logic supply voltages for notebook computers. The ISL8112 is designed primarily for battery-powered applications where high efficiency and low-quiescent supply current are critical. The ISL8112 provides a pin-selectable switching frequency, allowing operation for 200kHz/300kHz, 400kHz/300kHz, or 400kHz/500kHz on the SMPSs.

Light-load efficiency is enhanced by automatic Idle-Mode operation, a variable-frequency pulse-skipping mode that reduces transition and gate-charge losses. Each step-down, power-switching circuit consists of two n-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the n-channel high-side MOSFET must exceed the battery voltage, and is provided by a flying-capacitor boost circuit that uses a 100nF capacitor connected to BOOT_.

Both SMPS1 and SMPS2 PWM controllers consist of a triple-Mode feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers and logic. In addition, SMPS2 can also use OUT2REF to track its output from 0.5V to 2.50V. The ISL8112 contains fault-protection circuits that monitor the main PWM outputs for undervoltage and overvoltage conditions. A power-on sequence block controls the power-up timing of the main PWMs and monitors the outputs for undervoltage faults. The ISL8112 includes an adjustable low drop-out linear regulator. The bias generator blocks include the linear regulator, 3.3V precision reference, 2V precision reference and automatic bootstrap switch over circuit.

The synchronous-switch gate drivers are directly powered from PVCC, while the high-side switch gate drivers are indirectly powered from PVCC through an external capacitor and an internal Schottky diode boost circuit.

An automatic bootstrap circuit turns off the LDO linear regulator and powers the device from BYP if LDOREF is set to GND or VCC. See Table 1.

TABLE 1. LDO OUTPUT VOLTAGE TABLE

LDO VOLTAGE	CONDITIONS	COMMENT
VOLTAGE at BYP	LDOREF < 0.3V, BYP > 4.63V	Internal LDO is disabled.
VOLTAGE at BYP	LDOREF > VCC - 1V, BYP > 3V	Internal LDO is disabled.
5V	LDOREF < 0.3V, BYP < 4.63V	Internal LDO is active.
3.3V	LDOREF > VCC - 1V, BYP < 3V	Internal LDO is active.
2 x LDOREF	0.35V <LDOREF < 2.25V	Internal LDO is active.

FREE-RUNNING, CONSTANT ON-TIME PWM CONTROLLER WITH INPUT FEED-FORWARD

The constant on-time PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode type with voltage feed forward. The constant on-time PWM control architecture relies on the output ripple voltage to provide the PWM ramp signal; thus the output filter capacitor's ESR acts

as a current-feedback resistor. The high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (300ns typ). The on-time one-shot triggers when the following conditions are met: the error comparator's output is high, the synchronous rectifier current is below the current-limit threshold, and the minimum off time one-shot has timed out.

ON-TIME ONE-SHOT (FS)

Each PWM core includes a one-shot that sets the high-side switch on-time for each controller. Each fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V_{IN} input and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefit of a constant switching frequency is that the frequency can be selected to avoid noise-sensitive frequency regions:

$$t_{ON} = \frac{K(V_{OUT} + I_{LOAD} \cdot r_{DSON(LOWERQ)})}{V_{IN}} \quad \text{(EQ. 1)}$$

See Table 2 for approximate K- factors. Switching frequency increases as a function of load current due to the increasing drop across the synchronous rectifier, which causes a faster inductor-current discharge ramp. On-times translate only roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in the external high-side power MOSFET. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode (MODE = VCC) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes PH_ to go high earlier than normal, extending the on-time by a period equal to the UG-rising dead time.

For loads above the critical conduction point, the actual switching frequency is:

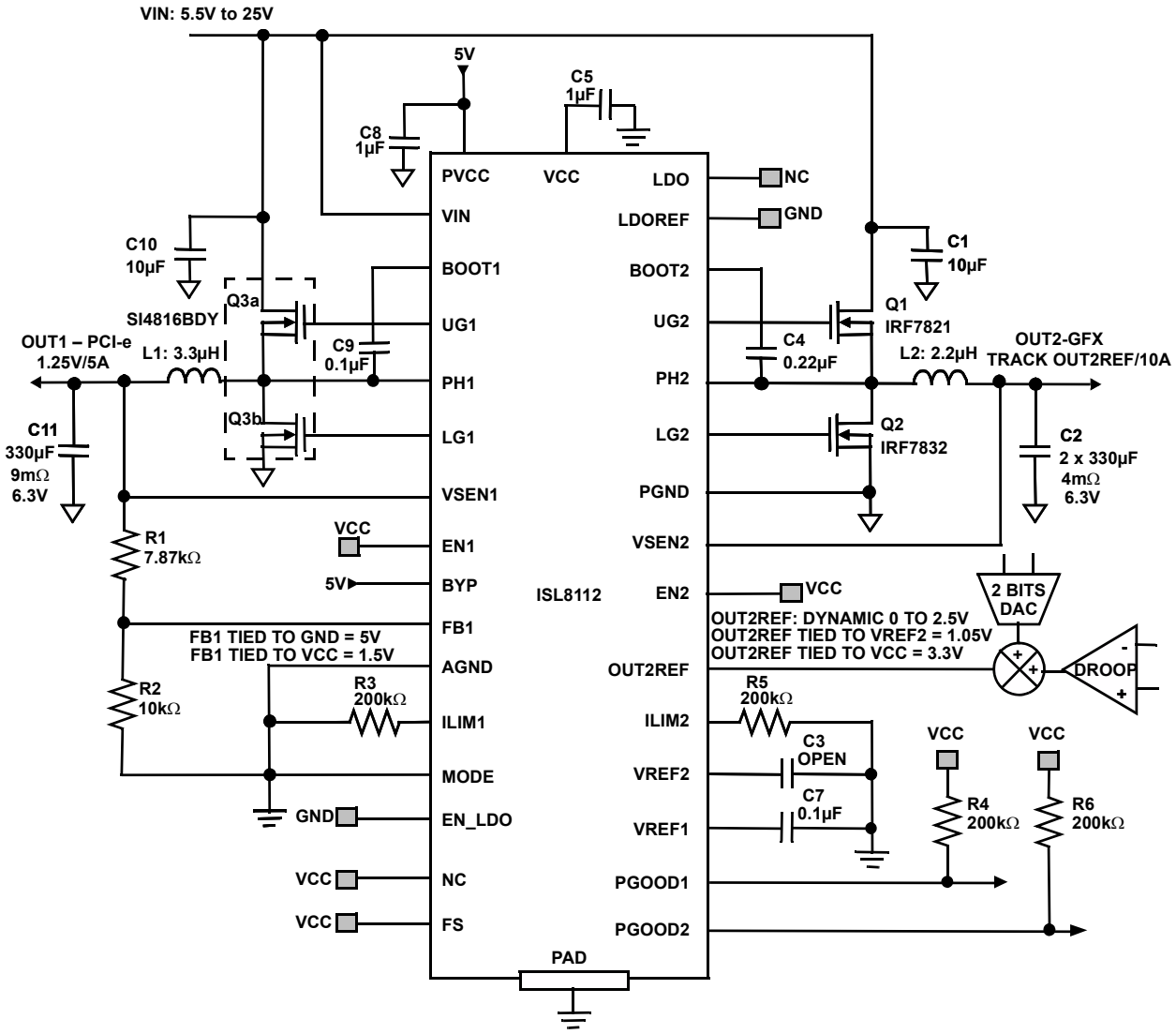
$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})} \quad \text{(EQ. 2)}$$

where:

- V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances
- V_{DROP2} is the sum of the parasitic voltage drops in the charging path, including high-side switch, inductor, and PC board resistances
- t_{ON} is the on-time calculated by the ISL8112.

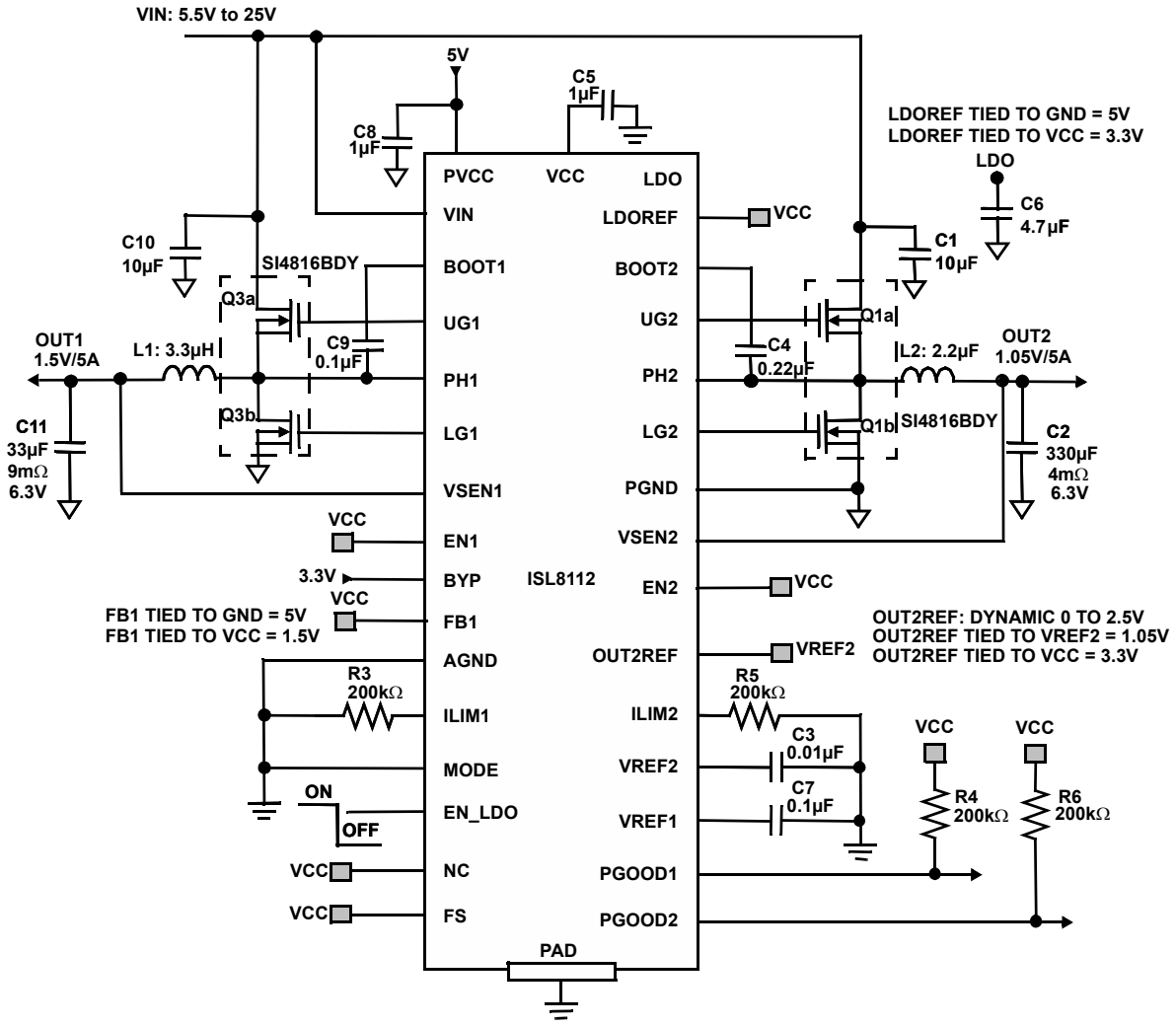
TABLE 2. APPROXIMATE K-FACTOR ERRORS

SMPS	SWITCHING FREQUENCY (kHz)	K-FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)
(FS = GND, VREF1, or OPEN), VSEN1	400	2.5	±10
(FS = GND), VSEN2	500	2.0	±10
(FS = VCC), VSEN1	200	5.0	±10
(FS = VCC, VREF1, or OPEN), VSEN2	300	3.3	±10



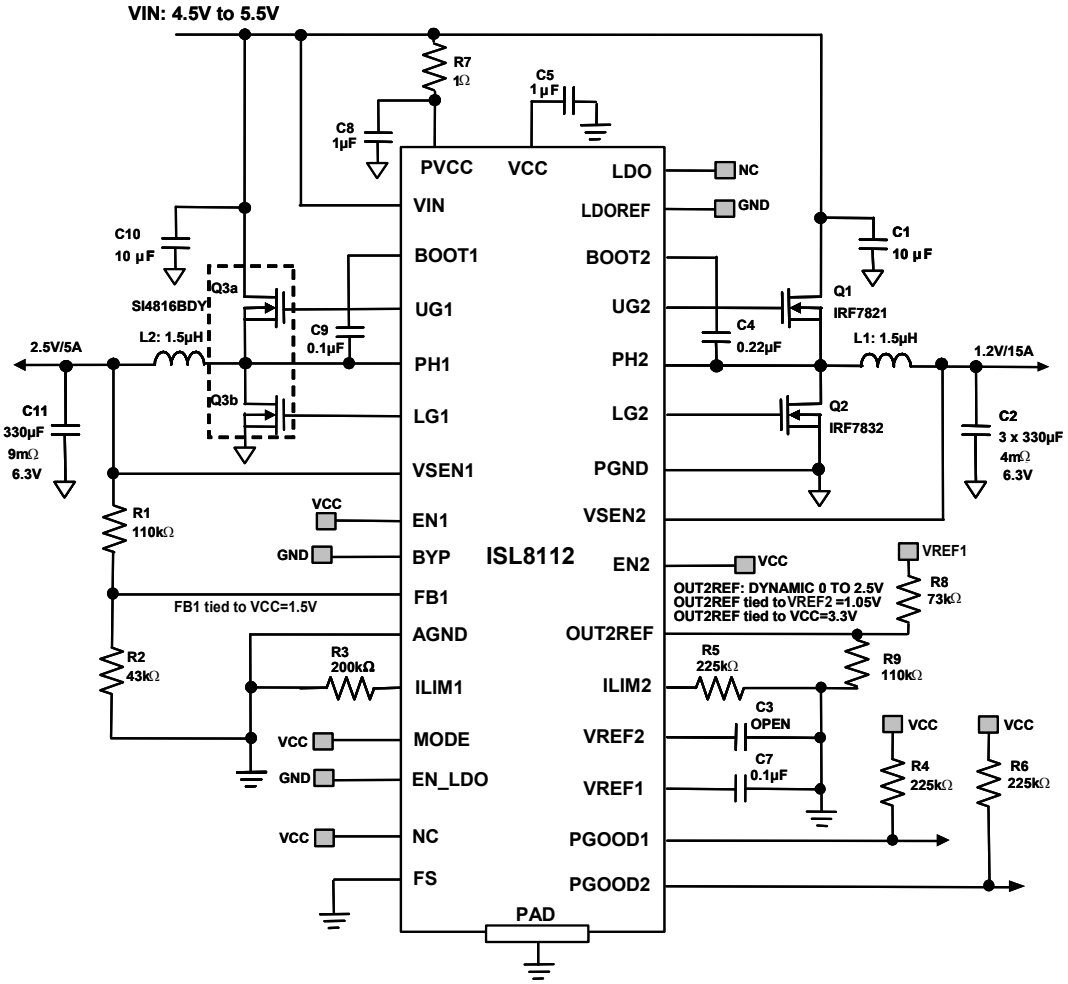
FREQUENCY-DEPENDENT COMPONENTS	
1.25V/1.05V SMPS SWITCHING FREQUENCY	FS = VCC
	200kHz/300kHz
L1	3.3µH
L2	2.7µH
C2	2 x 330µF
C11	330µF

FIGURE 17. ISL8112 TYPICAL DYNAMIC GFX APPLICATION CIRCUIT



FREQUENCY-DEPENDENT COMPONENTS	
1.5V/1.05V SMPS SWITCHING FREQUENCY	FS = VCC
	200kHz/300kHz
L1	3.3µH
L2	2.7µH
C2	330µF
C11	330µF

FIGURE 18. ISL8112 TYPICAL SYSTEM REGULATOR APPLICATION CIRCUIT



FREQUENCY-DEPENDENT COMPONENTS	
1.2V/2.5V SMPS SWITCHING FREQUENCY	FS = GND
	400kHz/500kHz
L1	1.5µH
L2	1.5µH
C2	3X330µF
C11	330µF

FIGURE 19. ISL8112 TYPICAL SYSTEM REGULATOR APPLICATION CIRCUIT

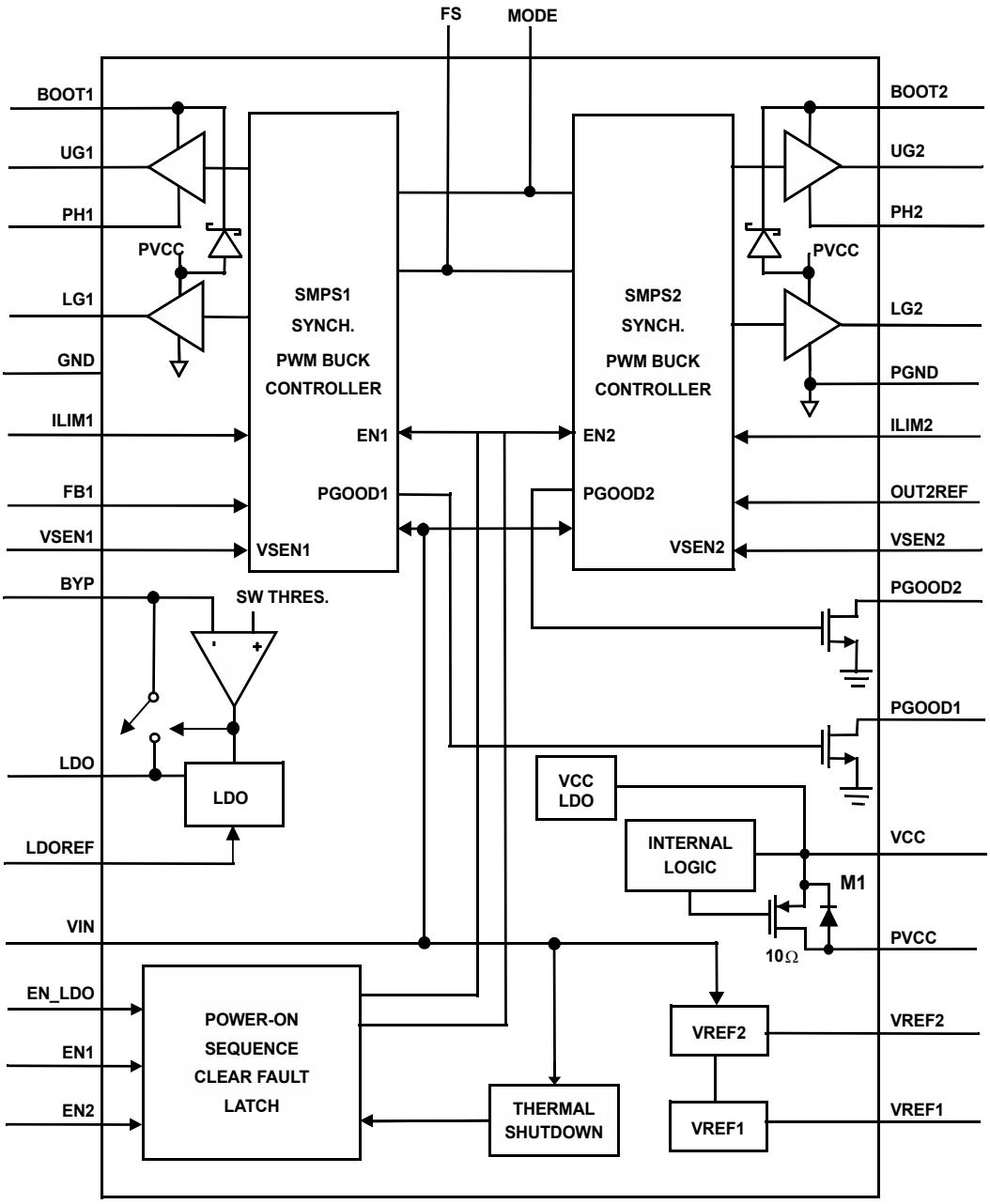


FIGURE 20. DETAIL FUNCTIONAL DIAGRAM ISL8112

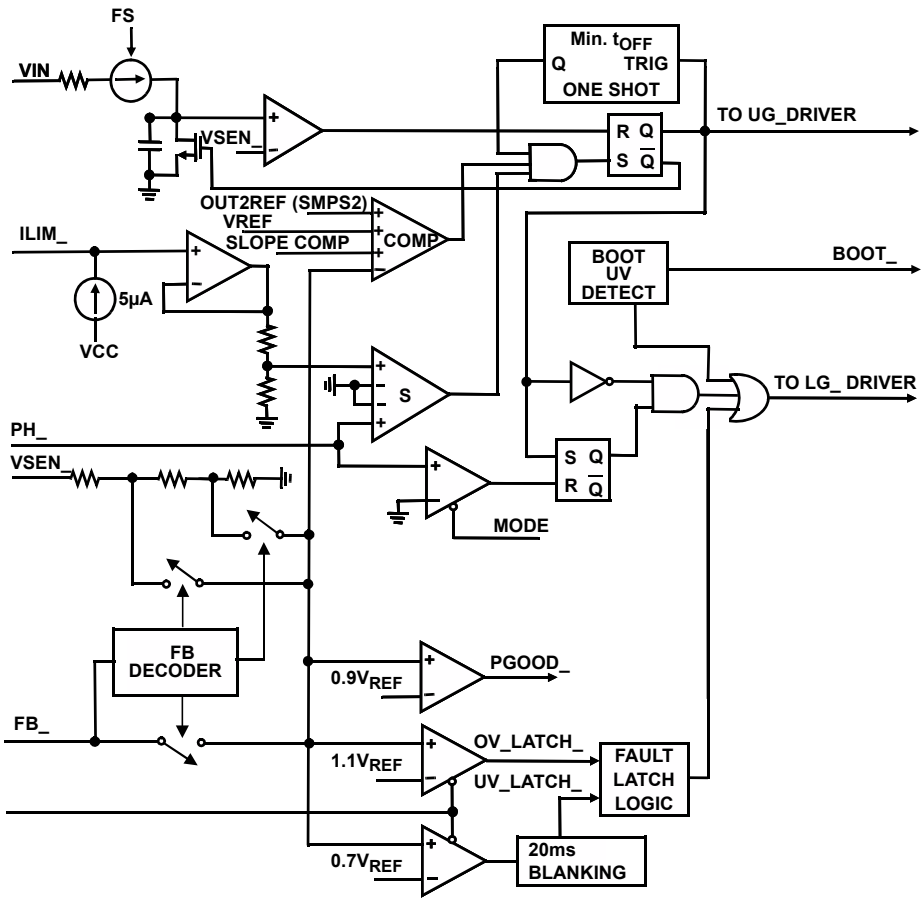


FIGURE 21. PWM CONTROLLER (ONE SIDE ONLY)

Automatic Pulse-Skipping Switch Over (Idle Mode)

In Idle Mode (MODE = GND), an inherent automatic switch over to PFM takes place at light loads. This switch over is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point):

$$I_{LOAD(SKIP)} = \frac{K \cdot V_{OUT}}{2 \cdot L}\frac{V_{IN} - V_{OUT}}{V_{IN}} \quad \text{(EQ. 3)}$$

where K is the on-time scale factor (see “On-Time One-Shot (FS)” on page 12). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to half the peak-to-peak ripple current, which is a function of the inductor value (Figure 22). For example, in the ISL8112 typical application circuit with VOUT1 = 5V, V_{IN} = 12V, L = 7.6µH, and K = 5µs, switch over to pulse-skipping operation occurs at I_{LOAD} = 0.96A or about on-fifth full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

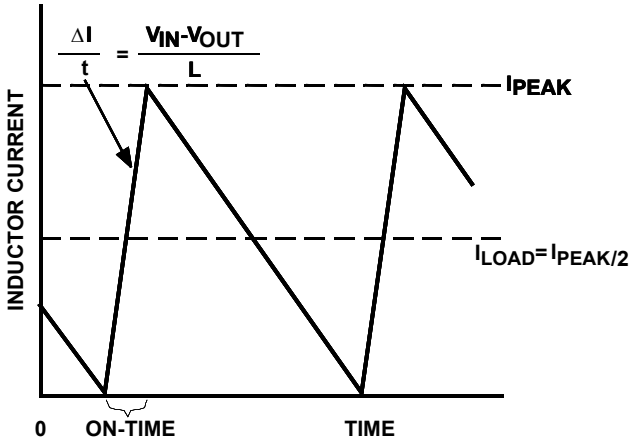


FIGURE 22. ULTRASONIC CURRENT WAVEFORMS

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger

physical size and degraded load-transient response (especially at low input-voltage levels).

DC output accuracy specifications refer to the trip level of the error comparator. When the inductor is in continuous conduction, the output voltage has a DC regulation higher than the trip level by 50% of the ripple. In discontinuous conduction (MODE = GND, light load), the output voltage has a DC regulation higher than the trip level by approximately 1.0% due to slope compensation.

Forced-PWM Mode

The low-noise, forced-PWM (MODE = VCC) mode disables the zero-crossing comparator, which controls the low-side switch on-time. Disabling the zero-crossing detector causes the low-side, gate-drive waveform to become the complement of the high-side, gate-drive waveform. The inductor current reverses at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 50mA, depending on switching frequency and the external MOSFETs.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor.

Enhanced Ultrasonic Mode (25kHz (min) Pulse Skipping)

Leaving MODE unconnected or connecting MODE to VREF1 activates a unique pulse-skipping mode with a minimum switching frequency of 25kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point (ILOAD(SKIP)).

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 20µs. Once triggered, the ultrasonic controller pulls LG high, turning on the low-side MOSFET to induce a negative inductor current. After FB drops below the regulation point, the controller turns off the low-side MOSFET (LG pulled low) and triggers a constant on-time (UG driven high). When the on-time has expired, the controller re-enables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold. Starting with a LG pulse greatly reduces the peak output voltage when compared to starting with a UG pulse, as long as VFB < VREF, LG is off and UG is on, similar to pure SKIP mode.

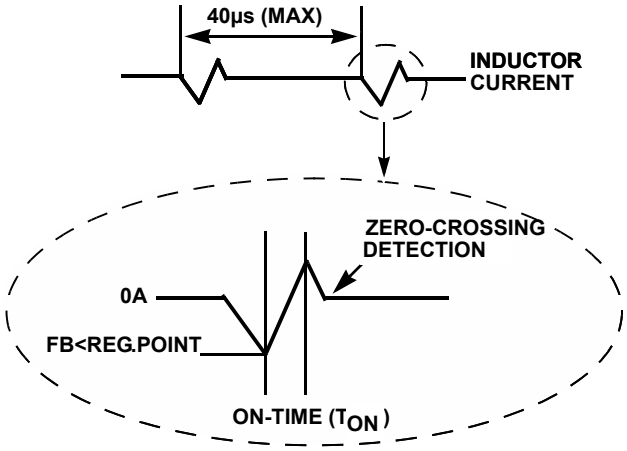


FIGURE 23. ULTRASONIC CURRENT WAVEFORMS

Reference and Linear Regulators (VREF2, VREF1, and LDO)

The 3.3V reference (VREF2) is accurate to ±1.5% over temperature, making VREF2 useful as a precision system reference. VREF2 can supply up to 5mA for external loads. Bypass VREF2 to GND with a 0.01µF capacitor. Leave open if there is no load.

The 2V reference (VREF1) is accurate to ±1% over temperature, also making VREF1 useful as a precision system reference. Bypass VREF1 to GND with a 0.1µF (min) capacitor. VREF1 can supply up to 50µA for external loads.

An internal regulator produces a fixed 5V (LDOREF < 0.2V) or 3.3V (LDOREF > VCC - 1V). In an adjustable mode, the LDO output can be set from 0.7V to 4.5V. The LDO output voltage is equal to two times the LDOREF voltage. The LDO regulator can supply up to 100mA for external loads. Bypass LDO with a minimum 4.7µF ceramic capacitor. When the LDOREF < 0.2V and BYP voltage is 5V, the LDO bootstrap-switch over to an internal 0.7Ω p-channel MOSFET switch connects BYP to LDO pin while simultaneously shutting down the internal linear regulator. These actions bootstrap the device, powering the loads from the BYP input voltages, rather than through internal linear regulators from the battery. Similarly, when the BYP = 3.3V and LDOREF = VCC, the LDO bootstrap-switch over to an internal 1.5Ω P-Channel MOSFET switch connects BYP to LDO pin while simultaneously shutting down the internal linear regulator. No switch over action in adjustable mode.

Current-Limit Circuit (ILIM_) with $r_{DS(ON)}$ Temperature Compensation

The current-limit circuit employs a "valley" current-sensing algorithm. The ISL8112 uses the on-resistance of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PH_ is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit

threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-limit threshold, inductor value and input and output voltage.

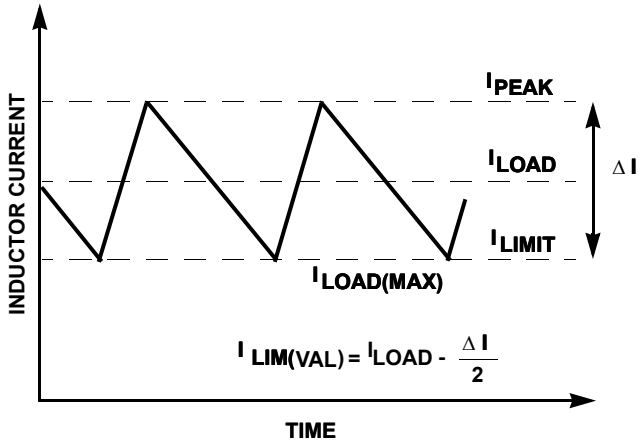


FIGURE 24. "VALLEY" CURRENT LIMIT THRESHOLD POINT

For lower power dissipation, the ISL8112 uses the on-resistance of the synchronous rectifier as the current-sense element. Use the worst-case maximum value for $r_{DS(ON)}$ from the MOSFET data sheet. Add some margin for the rise in $r_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise. The ISL8112 controller has a built-in 5µA current source as shown in Figure 25. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. The current limit varies with the on-resistance of the synchronous rectifier. When combined with the undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

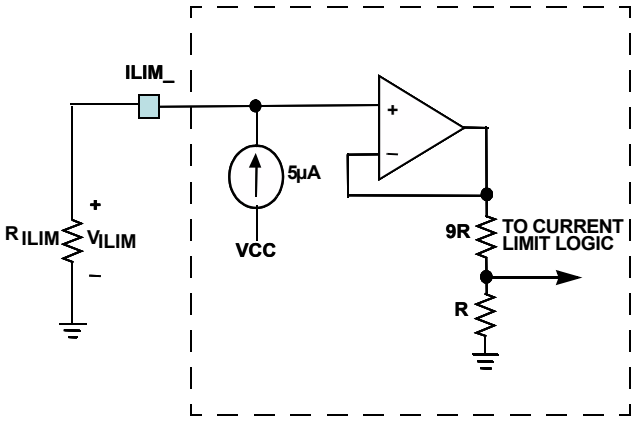


FIGURE 25. CURRENT LIMIT BLOCK DIAGRAM

A negative current limit prevents excessive reverse inductor currents when VOUT sinks current. The negative current-limit threshold is set to approximately 120% of the positive current limit and therefore tracks the positive current limit when ILIM_ is adjusted. The current-limit threshold is adjusted with an external resistor for ISL8112 at ILIM_. The current-limit threshold adjustment range is from 20mV to 200mV. In the adjustable mode, the current-limit threshold voltage is 1/10th the voltage at ILIM_. The voltage at ILIM pin is the product of 5µA * R_{ILIM}. The threshold defaults to 100mV when ILIM_ is connected to VCC. The logic threshold for switch-over to the 100mV default value is approximately VCC - 1V.

The PC board layout guidelines should be carefully observed to ensure that noise and DC errors do not corrupt the current-sense signals at PH_.

MOSFET Gate Drivers (UG_, LG_)

The UG_ and LG_ gate drivers sink 2.0A and 3.3A respectively of gate drive, ensuring robust gate drive for high-current applications. The UG_ floating high-side MOSFET drivers are powered by diode-capacitor charge pumps at BOOT_. The LG_ synchronous-rectifier drivers are powered by PVCC.

The internal pull-down transistors that drive LG_ low have a 0.6Ω typical on-resistance. These low on-resistance pull-down transistors prevent LG_ from being pulled up during the fast rise time of the inductor nodes due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFETs. However, for high-current applications, some combinations of high- and low-side MOSFETs may cause excessive gate-drain coupling, which leads to poor efficiency and EMI-producing shoot-through currents. Adding a 4.7Ω resistor in series with BOOT_ increases the turn-on time of the high-side MOSFETs at the expense of efficiency, without degrading the turn-off time (Figure 26).

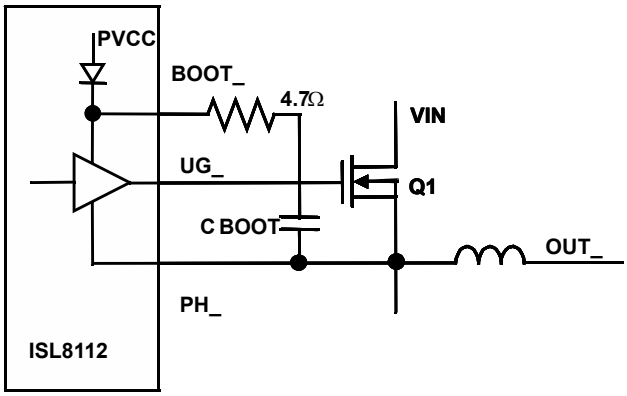


FIGURE 26. REDUCING THE SWITCHING-NODE RISE TIME

Adaptive dead-time circuits monitor the LG_ and UG_ drivers and prevent either FET from turning on until the other is fully off. This algorithm allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be low-resistance, low-inductance paths from the gate drivers to the MOSFET gates for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry interprets the MOSFET gate as "off" when there is actually charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 mils to 100 mils wide if the MOSFET is 1” from the device).

Boost-Supply Capacitor Selection (Buck)

The boost capacitor should be 0.1µF to 4.7µF, depending on the input and output voltages, external components, and PC board layout. The boost capacitance should be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET conduction time, which happens at maximum operating duty cycle (this occurs at minimum input voltage). The minimum gate to source voltage ($V_{GS(MIN)}$) is determined by:

$$V_{GS(MIN)} = PVCC \cdot \frac{C_{BOOT}}{C_{BOOT} + C_{GS}} \quad \text{(EQ. 4)}$$

where:

- PVCC is 5V
- C_{GS} is the gate capacitance of the high-side MOSFET

POR, UVLO, and Internal Digital Soft-Start

Power-on reset (POR) occurs when VIN rises above approximately 3V. UVLO occurs when PVCC drops below approximately 4V. The VIN POR reset the LDO control. The UVLO resets the undervoltage, overvoltage, and thermal-shutdown fault latches. PVCC undervoltage lockout (UVLO) circuitry inhibits switching when PVCC is below 4V. LG_ is low during UVLO. The output voltages begin to ramp up once PVCC exceeds its 4V UVLO and VREF1 is in regulation. The internal digital soft-start timer begins to ramp up the maximum-allowed current limit during start-up. The 1.7ms ramp occurs in five steps of positive current limit and the step size is 20%, 40%, 60%, 80% and 100%.

Power-Good Output (PGOOD_)

The PGOOD_ comparator continuously monitors both output voltages for undervoltage conditions. PGOOD_ is actively held low in shutdown, standby, and soft-start. PGOOD1 releases and digital soft-start terminates when VSEN1 reach the error-comparator threshold. PGOOD1 goes low if VOUT1 output turns off or is 10% below its nominal regulation point. PGOOD1 is a true open-drain output. Likewise, PGOOD2 is used to monitor VSEN2.

Fault Protection

The ISL8112 provides overvoltage/undervoltage fault protection in the buck controllers. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions.

- Out-of-bound Condition

  When the output voltage is 5% above the set voltage, the out-of-bound condition activates. LG turns on until output reaches within regulation. Once the output is within regulation, the controller will operate as normal. It is the "first line of defense" before OVP.

- Overvoltage Protection

  When VSEN1 is 11% (16% for VSEN2) above the set voltage, the overvoltage fault protection activates. This latches on the synchronous rectifier MOSFET with 100% duty cycle, rapidly discharging the output capacitor until the negative current limit is achieved. Once negative current limit is met, UG is turned on for a minimum on-time, followed by another LG pulse until negative current limit. This effectively regulates the discharge current at the negative current limit in an effort to prevent excessively large negative currents that cause potentially damaging negative voltages on the load. Once an overvoltage fault condition is set, it can only be reset by toggling SHDN#, EN_, or cycling PVCC(UVLO).

- Undervoltage Protection

  When the output voltage drops below 70% of its regulation voltage for at least 100µs, the controller sets the fault latch and begins the discharge mode (see the Shutdown and Output Discharge section). UVP is ignored for at least 20ms (typical), after start-up or after a rising edge on EN_. Toggle EN_ or cycle PVCC (UVLO) to clear the undervoltage fault latch and restart the controller. UVP only applies to the buck outputs.

- Thermal Protection

  The ISL8112 has thermal shutdown to protect the devices from overheating. Thermal shutdown occurs when the die temperature exceeds +150°C. All internal circuitry shuts down during thermal shutdown. The ISL8112 may trigger thermal shutdown if LDO_ is not bootstrapped from VSEN_ while applying a high input voltage on VIN and drawing the maximum current (including short circuit) from LDO_. Even if LDO_ is bootstrapped from VSEN_, overloading the LDO_ causes large power dissipation on the bootstrap switches, which may result in thermal shutdown. Cycling EN_, EN_LDO, or PVCC(UVLO) ends the thermal-shutdown state.

Discharge Mode (Soft-Stop)

When a transition to standby or shutdown mode occurs, or the output is discharged to GND through an internal 25Ω switch, the reference remains active to provide an accurate threshold and to provide overvoltage protection.

When the output undervoltage fault latch is set, both channels are discharged to GND through the internal 25Ω switches.

Shutdown Mode

The ISL8112 SMPS1, SMPS2 and LDO have independent enabling control. Drive EN1, EN2 and EN_LDO below the precise input falling-edge trip level to place the ISL8112 in its low-power shutdown state. The ISL8112 consumes only 20µA of quiescent current while in shutdown. When shutdown mode activates, the 3.3V VREF2 remain on. Both SMPS outputs are discharged to 0V through a 25Ω switch.

Power-Up Sequencing and On/Off Controls (EN_)

EN1 and EN2 control SMPS power-up sequencing. EN1 or EN2 rising above 2.4V enables the respective outputs. EN1 or EN2 falling below 1.6V disables the respective outputs.

Connecting EN1 or EN2 to VREF1 will force its outputs off while the other output is below regulation. The sequenced SMPS will start once the other SMPS reaches regulation. The second SMPS remains on until the first SMPS turns off, the device shuts down, a fault occurs or PVCC goes into undervoltage lockout. Both supplies begin their power-down sequence immediately when the first supply turns off. Driving EN_ below 0.8V clears the overvoltage, undervoltage and thermal fault latches.

TABLE 3. OPERATING-MODE TRUTH TABLE

MODE	CONDITION	COMMENT
Power-Up	PVCC < UVLO threshold.	Transitions to discharge mode after a PVCC UVLO and after VREF1 becomes valid. LDO, VREF2, and VREF1 remain active.
Run	EN_LDO = high, EN1 or EN2 enabled.	Normal operation
Overvoltage Protection	Either output > 111% (VSEN1) or 116% (VSEN2) of nominal level.	LG_ is forced high. LDO, VREF2 and VREF1 active. Exited by a PVCC UVLO, VCC POR, or by toggling EN1 or EN2.
Undervoltage Protection	Either output < 70% of nominal after 20ms time-out expires and output is enabled.	Both the internal 25Ω switches turn on. LDO, VREF2 and VREF1 are active. Exited by a PVCC UVLO, or by toggling EN1 or EN2.
Discharge	Either SMPS output is still high in either standby mode or shutdown mode	Discharge switch (25Ω) connects VSEN_ to GND. One output may still run while the other is in discharge mode. Activates when PVCC is in UVLO, or transition to UVLO, standby, or shutdown has begun. LDO, VREF2 and VREF1 active.
Standby	EN1, EN2 < startup threshold, EN_LDO= High	LDO, VREF2 and VREF1 active.
Shutdown	EN1, EN2, EN_LDO = low	Discharge switch (25Ω) connects VSEN_ to PGND. All circuitry off except VREF2.
Thermal Shutdown	TJ > +150°C	All circuitry off. Exited by PVCC UVLO or cycling EN_. VREF2 remain active.

TABLE 4. SHUTDOWN AND STANDBY CONTROL LOGIS

VEN_LDO	VEN1 (V)	VEN2 (V)	LDO	SMPS1	SMPS2
Low	Low	Low	Off	Off	Off
“>2.5” → High	Low	Low	On	Off	Off
“>2.5” → High	High	High	On	On	On
“>2.5” → High	High	Low	On	On	Off
“>2.5” → High	Low	High	On	Off	On
“>2.5” → High	High	VREF1	On	On	On (after SMPS1 is up)
“>2.5” → High	VREF1	High	On	On (after SMPS2 is up)	On

Adjustable-Output Feedback (Dual-Mode FB)

Connect FB1 to GND to enable the fixed 5V or tie FB1 to VCC to set the fixed 1.5V output. Connect a resistive voltage-divider at FB1 between output and GND to adjust the respective output voltage between 0.7V and 5.5V (Figure 27). Choose R2 to be approximately 10k and solve for R1 using Equation 5.

$$R1 = R2 \cdot \left(\frac{V_{OUT1}}{V_{FB1}} - 1 \right) \quad \text{(EQ. 5)}$$

where V_{FB1} = 0.7V nominal.

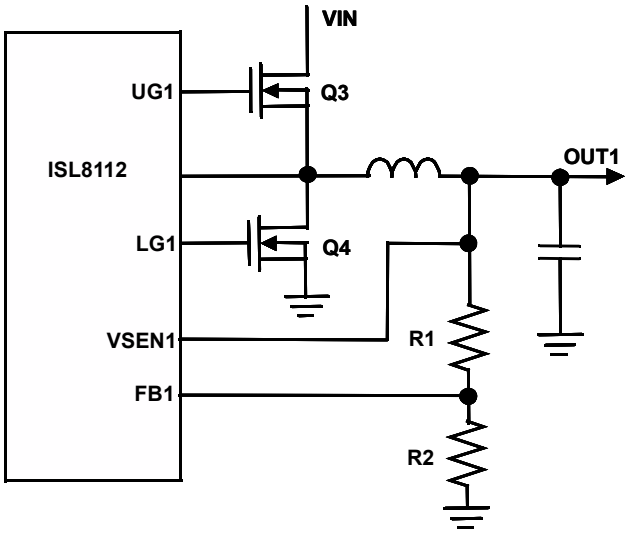


FIGURE 27. SETTING V_{OUT1} WITH A RESISTOR DIVIDER

Likewise, connect OUT2REF to VCC to enable the fixed 3.3V or tie OUT2REF to VREF2 to set the fixed 1.05V output. Set OUT2REF from 0 to 2.50V for SMPS2 tracking mode (Figure 28).

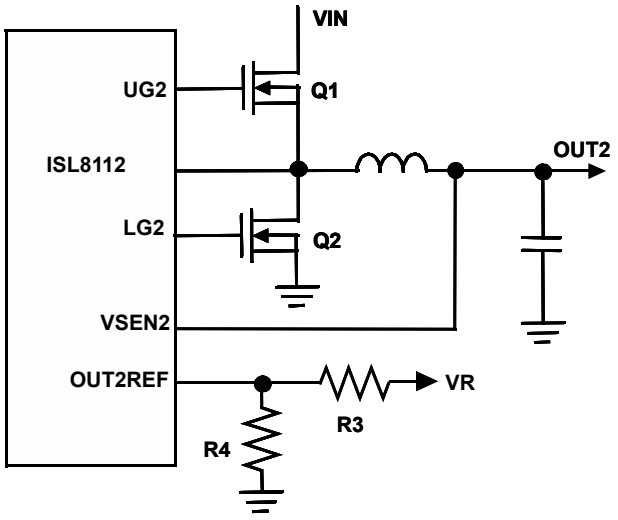


FIGURE 28. SETTING V_{OUT2} WITH A VOLTAGE DIVIDER FOR TRACKING

$$R3 = R4 \cdot \left(\frac{VR}{V_{OUT2}} - 1 \right) \quad \text{(EQ. 6)}$$

where:

- VR = 2V nominal (if tied to VREF1)

or

- VR = 3.3V nominal (if tied to VREF2)

Design Procedure

Establish the input voltage range and maximum load current before choosing an inductor and its associated ripple-current ratio (LIR). The following four factors dictate the rest of the design:

1. Input Voltage Range. The maximum value (V_{IN}(MAX)) must accommodate the maximum AC adapter voltage. The minimum value (V_{IN}(MIN)) must account for the lowest input voltage after drops due to connectors, fuses and battery selector switches. Lower input voltages result in better efficiency.
2. Maximum Load Current. The peak load current (ILOAD(MAX)) determines the instantaneous component stress and filtering requirements and thus drives output capacitor selection, inductor saturation rating and the design of the current-limit circuit. The continuous load current (ILOAD) determines the thermal stress and drives the selection of input capacitors, MOSFETs and other critical heat-contributing components.
3. Switching Frequency. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage and MOSFET switching losses.
4. Inductor Ripple Current Ratio (LIR). LIR is the ratio of the peak-peak ripple current to the average inductor current. Size and efficiency trade-offs must be considered when setting the inductor ripple current ratio. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

   The ISL8112 pulse-skipping algorithm (MODE = GND) initiates skip mode at the critical conduction point, so the inductor's operating point also determines the load current at which PWM/PFM switch over occurs. The optimum point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT\_}(V_{IN} + V_{OUT\_})}{V_{IN} \cdot f \cdot LIR \cdot I_{LOAD(MAX)}} \quad \text{(EQ. 7)}$$

Example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT2} = 5V, f = 200kHz, 35% ripple current or LIR = 0.35:

$$L = \frac{5V(12V-5V)}{12V \cdot 200kHz \cdot 0.35 \cdot 5A} = 8.3\mu H \quad \text{(EQ. 8)}$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. The core must be large enough not to saturate at the peak inductor current (IPEAK):

$$IPEAK = I_{LOAD(MAX)} + [(LIR/2) \cdot I_{LOAD(MAX)}] \quad \text{(EQ. 9)}$$

The inductor ripple current also impacts transient response performance, especially at low V_{IN} - VSEN_ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (VSAG) is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$VSAG = \frac{(\Delta I_{LOAD(MAX)})^2 \cdot L\left(K\left(\frac{V_{OUT}}{V_{IN}}\right) + t_{OFF(MIN)}\right)}{2 \cdot C_{OUT} \cdot V_{OUT}\left[K\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right) - t_{OFF(MIN)}\right]} \quad \text{(EQ. 10)}$$

where minimum off-time = 0.35µs (max) and K is from Table 2.

Determining the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at ILOAD(MAX) minus half of the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - [(LIR/2) \cdot I_{LOAD(MAX)}] \quad \text{(EQ. 11)}$$

where: $I_{LIMIT(LOW)}$ = minimum current-limit threshold voltage divided by the $r_{DS(ON)}$ of Q2/Q4.

Use the worst-case maximum value for $r_{DS(ON)}$ from the MOSFET Q2/Q4 data sheet and add some margin for the rise in $r_{DS(ON)}$ with temperature. A good general rule is to allow 0.2% additional resistance for each °C of temperature rise. Examining the 5A circuit example with a maximum $r_{DS(ON)}$ = 5mΩ at room temperature. At +125°C reveals the following:

$$I_{LIMIT(LOW)} = (25mV)/((5m\Omega \times 1.2) > 5A - (0.35/2)5A) \quad \text{(EQ. 12)}$$

$$4.17A > 4.12A \quad \text{(EQ. 13)}$$

4.17A is greater than the valley current of 4.12A, so the circuit can easily deliver the full-rated 5A using the 30mV nominal current-limit threshold voltage.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault latch. In applications where the output is subject to large load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{SER} \leq \frac{V_{DIP}}{I_{LOAD(MAX)}} \quad \text{(EQ. 14)}$$

where V_{DIP} is the maximum-tolerable transient voltage drop. In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{P-P}}{L_{IR} \cdot I_{LOAD(MAX)}} \quad \text{(EQ. 15)}$$

where V_{P-P} is the peak-to-peak output voltage ripple. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalum, OS-CON, and other electrolytic-type capacitors).

When using low-capacity filter capacitors such as polymer types, capacitor size is usually determined by the capacity required to prevent VSAG and VSOAR from tripping the undervoltage and overvoltage fault latches during load transients in ultrasonic mode.

For low input-to-output voltage differentials (V_{IN}/ V_{OUT} < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode. The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{I_{PEAK}^2 \cdot L}{2 \cdot C_{OUT} \cdot V_{OUT\_}} \quad \text{(EQ. 16)}$$

where I_{PEAK} is the peak inductor current.

Input Capacitor Selection

The input capacitors must meet the input-ripple-current (IRMS) requirement imposed by the switching current. The ISL8112 dual switching regulator operates at different frequencies. This interleaves the current pulses drawn by the two switches and reduces the overlap time where they add together. The input RMS current is much smaller in comparison than with both SMPSs operating in phase. The input RMS current varies with load and the input voltage.

The maximum input capacitor RMS current for a single SMPS is given by:

$$I_{RMS} \approx I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT\_})}}{V_{IN}}\right) \quad \text{(EQ. 17)}$$

When $V_{IN} = 2 \cdot V_{OUT\_}(D = 50\%)$, IRMS has maximum current of $I_{LOAD}/2$.

The ESR of the input-capacitor is important for determining capacitor power dissipation. All the power (I_{RMS}^2 x ESR) heats up the capacitor and reduces efficiency. Nontantalum chemistries (ceramic or OS-CON) are preferred due to their low ESR and resilience to power-up surge currents. Choose input capacitors that exhibit less than +10°C temperature rise at the RMS input current for optimal circuit longevity. Place the drains of the high-side switches close to each other to share common input bypass capacitors.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

Choose a high-side MOSFET (Q1/Q3) that has conduction losses equal to the switching losses at the typical battery voltage for maximum efficiency. Ensure that the conduction losses at the minimum input voltage do not exceed the package thermal limits or violate the overall thermal budget. Ensure that conduction losses plus switching losses at the maximum input voltage do not exceed the package ratings or violate the overall thermal budget.

Choose a synchronous rectifier (Q2/Q4) with the lowest possible $r_{DS(ON)}$. Ensure the gate is not pulled up by the high-side switch turning on due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses are not an issue for the synchronous rectifier in the buck topology since it is a zero-voltage switched device when using the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to the MOSFET's $r_{DS(ON)}$ occurs at the minimum battery voltage:

$$PD(Q_H \text{ Resistance}) = \left(\frac{V_{OUT\_}}{V_{IN(MIN)}}\right)(I_{LOAD})^2 \cdot r_{DS(ON)} \quad \text{(EQ. 18)}$$

Generally, a small high-side MOSFET reduces switching losses at high input voltage. However, the $r_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum situation occurs when the switching (AC) losses equal the conduction ($r_{DS(ON)}$) losses.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum battery voltage is applied, due to the squared term in the CV^2f switching-loss equation. Reconsider the high-side MOSFET chosen for adequate $r_{DS(ON)}$ at low battery voltages if it becomes extraordinarily hot when subjected to $V_{IN(MAX)}$.

Calculating the power dissipation in NH (Q1/Q3) due to switching losses is difficult since it must allow for quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for bench evaluation, preferably including verification using a thermocouple mounted on NH (Q1/Q3):

$$PD(Q_H \text{ Switching}) = (V_{IN(MAX)})^2\left(\frac{C_{RSS} \cdot f_{SW} \cdot I_{LOAD}}{I_{GATE}}\right) \quad \text{(EQ. 19)}$$

where C_{RSS} is the reverse transfer capacitance of Q_H (Q1/Q3) and I_{GATE} is the peak gate-drive source/sink current.

For the synchronous rectifier, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q_L) = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)I_{LOAD}^2 \cdot r_{DS(ON)} \quad \text{(EQ. 20)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + ((LIR)/2) \cdot I_{LOAD(MAX)} \quad \text{(EQ. 21)}$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and resistance variation.

Rectifier Selection

Current circulates from ground to the junction of both MOSFETs and the inductor when the high-side switch is off. As a consequence, the polarity of the switching node is negative with respect to ground. This voltage is approximately -0.7V (a diode drop) at both transition edges while both switches are off (dead time). The drop is $I_L \cdot r_{DS(ON)}$ when the low-side switch conducts.

The rectifier is a clamp across the synchronous rectifier that catches the negative inductor swing during the dead time between turning the high-side MOSFET off and the synchronous rectifier on. The MOSFETs incorporate a high-speed silicon body diode as an adequate clamp diode if efficiency is not of primary importance. Place a Schottky diode in parallel with the body diode to reduce the forward voltage drop and prevent the Q2/Q4 MOSFET body diodes from turning on during the dead time. Typically, the external diode improves the efficiency by 1% to 2%. Use a Schottky diode with a DC current rating equal to one-third of the load current. For example, use an MBR0530 (500mA-rated) type for loads up to 1.5A, a 1N5817 type for loads up to 3A, or a 1N5821 type for loads up to 10A. The rectifier's rated reverse breakdown

voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Applications Information

Dropout Performance

The output voltage-adjust range for continuous-conduction operation is restricted by the nonadjustable 350ns (max) minimum off-time one-shot. Use the slower 5V SMPS for the higher of the two output voltages for best dropout performance in adjustable feedback mode. The duty-factor limit must be calculated using worst-case values for on-times and off-times, when working with low input voltages. Manufacturing tolerances and internal propagation delays introduce an error to the FS K-factor. Also, keep in mind that transient-response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see Equation 10 on page 23).

The absolute point of dropout occurs when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ indicates the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current is less able to increase during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this can be adjusted up or down to allow trade-offs between V_{SAG}, output capacitance and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{(V_{OUT\_} + V_{DROP})}{1 - \left(\frac{t_{OFF(MIN)} \cdot h}{K}\right)} + V_{DROP2} - V_{DROP1} \quad \text{(EQ. 22)}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see “On-Time One-Shot (FS)” on page 12), $t_{OFF(MIN)}$ is from the “Electrical Specifications” table on page 4 and K is taken from Table 2. The absolute minimum input voltage is calculated with h = 1.

Operating frequency must be reduced or h must be increased and output capacitance added to obtain an acceptable V_{SAG} if calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage. Calculate V_{SAG} to be sure of adequate transient response if operation near dropout is anticipated.

Dropout Design Example:

ISL8112: With V_{OUT2} = 5V, fsw = 400kHz, K = 2.25µs, $t_{OFF(MIN)}$ = 350ns, $V_{DROP1} = V_{DROP2}$ = 100mV, and h = 1.5, the minimum V_{IN} is:

$$V_{IN(MIN)} = \frac{(5V + 0.1V)}{1 - \left(\frac{0.35\mu s \cdot 1.5}{2.25\mu s}\right)} + 0.1V - 0.1V = 6.65V \quad \text{(EQ. 23)}$$

Calculating with h = 1 yields:

$$V_{IN(MIN)} = \frac{(5V + 0.1V)}{1 - \left(\frac{0.35\mu s \cdot 1}{2.25\mu s}\right)} + 0.1V - 0.1V = 6.04V \quad \text{(EQ. 24)}$$

Therefore, V_{IN} must be greater than 6.65V. A practical input voltage with reasonable output capacitance would be 7.5V.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve minimal switching losses and clean, stable operation. This is especially true when multiple converters are on the same PC board where one circuit can affect the other. Refer to the ISL8112 Evaluation Kit data sheet for a specific layout example.

Mount all of the power components on the top side of the board with their ground terminals flush against one another, if possible. Follow these guidelines for good PC board layout:

- Isolate the power components on the top side from the sensitive analog components on the bottom side with a ground shield. Use a separate PGND plane under the VSEN1 and VSEN2 sides (called PGND1 and PGND2). Avoid the introduction of AC currents into the PGND1 and PGND2 ground planes. Run the power plane ground currents on the top side only, if possible.
- Use a star ground connection on the power plane to minimize the crosstalk between VSEN1 and VSEN2.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- PH_ (ISL8112) and GND connections to the synchronous rectifiers for current limiting must be made using Kelvin-sense connections to guarantee the current-limit accuracy with 8-pin SO MOSFETs. This is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting PH_ traces inside (underneath) the MOSFETs.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the synchronous rectifier or between the inductor and the output filter capacitor.
- Ensure that the VSEN_ connection to COUT_ is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the VSEN_ connector node and the output filter capacitor (see the Stability Considerations section).
- Route high-speed switching nodes (BOOT_, UG_, PH_, and LG_) away from sensitive analog areas (VREF1, ILIM_, and

FB_). Use PGND1 and PGND2 as an EMI shield to keep radiated switching noise away from the IC's feedback divider and analog bypass capacitors.

- Make all pin-strap control input connections (MODE, ILIM_, etc.) to GND or VCC of the device.

Layout Procedure

Place the power components first with ground terminals adjacent (Q2/Q4 source, CIN_, COUT_). If possible, make all these connections on the top layer with wide, copper-filled areas.

Mount the controller IC adjacent to the synchronous rectifier MOSFETs close to the hottest spot, preferably on the back side in order to keep UG_, GND, and the LG_ gate drive lines short and wide. The LG_ gate trace must be short and wide, measuring 50 mils to 100 mils wide if the MOSFET is 1” from the controller device.

Group the gate-drive components (BOOT_ capacitor, VIN bypass capacitor) together near the controller device.

Make the DC/DC controller ground connections as follows:

1. Near the device, create a small analog ground plane.
2. Connect the small analog ground plane to GND and use the plane for the ground connection for the VREF1 and VCC bypass capacitors, FB dividers and ILIM resistors (if any).
3. Create another small ground island for PGND and use the plane for the VIN bypass capacitor, placed very close to the device.
4. Connect the GND and PGND planes together at the metal tab under device.

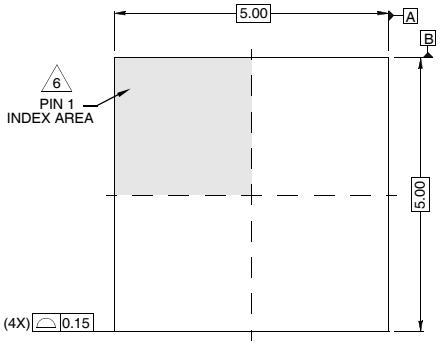
On the board's top side (power planes), make a star ground to minimize crosstalk between the two sides. The top-side star ground is a star connection of the input capacitors and synchronous rectifiers. Keep the resistance low between the star ground and the source of the synchronous rectifiers for accurate current limit. Connect the top-side star ground (used for MOSFET, input, and output capacitors) to the small island with a single short, wide connection (preferably just a via). Create PGND islands on the layer just below the top-side layer (refer to the ISL8112 EV kit for an example) to act as an EMI shield if multiple layers are available (highly recommended). Connect each of these individually to the star ground via, which connects the top side to the PGND plane. Add one more solid ground plane under the device to act as an additional shield, and also connect the solid ground plane to the star ground via.

Connect the output power planes (VCORE and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias.

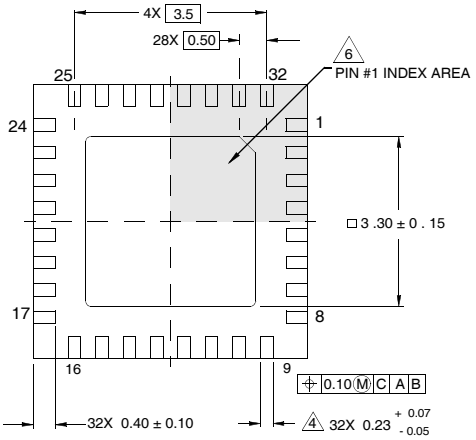
Package Outline Drawing

L32.5x5B

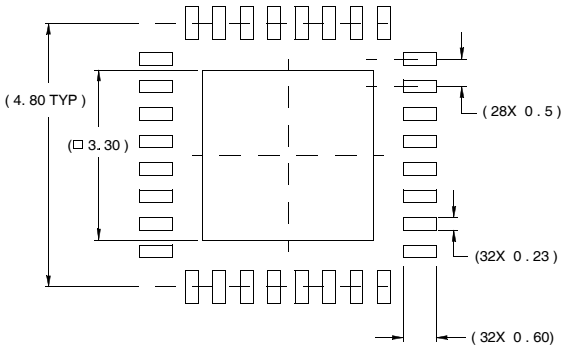
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 5/10



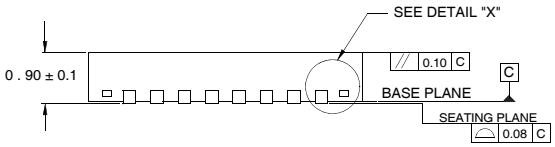
TOP VIEW



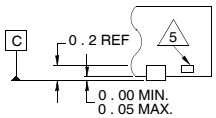
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.