

Dual Self-Protected Low-Side Driver with Temperature and Current Limit



NCV8402D, NCV8402AD

NCV8402D/AD is a dual protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

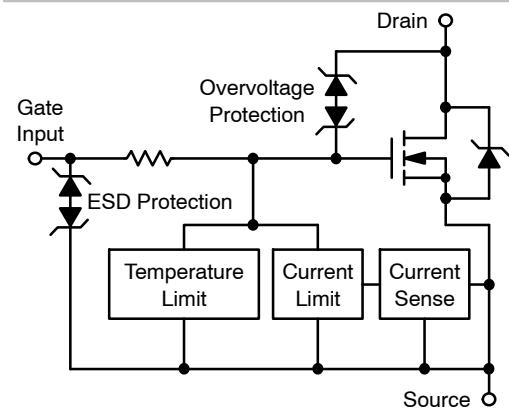
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

ON Semiconductor®

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$V_{(BR)DSS}$ (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX
42 V	165 mΩ @ 10 V	2.0 A*

*Max current limit value is dependent on input condition.

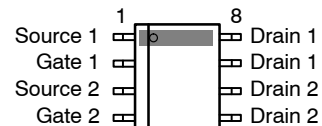


MARKING DIAGRAM



xxxxxx = V8402D or 8402AD
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NCV8402DDR2G	SOIC-8	2500/Tape & Reel
NCV8402ADDR2G	(Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V _{DSS}	42	V
Drain-to-Gate Voltage Internally Clamped (R _G = 1.0 MΩ)	V _{DGR}	42	V
Gate-to-Source Voltage	V _{GS}	± 14	V
Continuous Drain Current	I _D	Internally Limited	
Total Power Dissipation	P _D	0.8 1.62	W
		@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	
Maximum Continuous Drain, both channels on	I _D	1.87 2.65	A
		@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	
Thermal Resistance	Junction-to-Ambient Steady State (Note 1) R _{θJA} Junction-to-Ambient Steady State (Note 2) R _{θJA}	157 77	°C/W
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 32 V, V _G = 5.0 V, I _{PK} = 1.0 A, L = 300 mH, R _{G(ext)} = 25 Ω)	E _{AS}	150	mJ
Load Dump Voltage (V _{GS} = 0 and 10 V, R _I = 2.0 Ω, R _L = 9.0 Ω, t _d = 400 ms)	V _{LD}	55	V
Operating Junction and Storage Temperature	T _J , T _{stg}	-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted onto min pad FR4 PCB, (Cu area = 40 sq. mm, 1 oz.).
2. Surface-mounted onto 1" sq. FR4 board (Cu area = 625 sq. mm, 2 oz.).

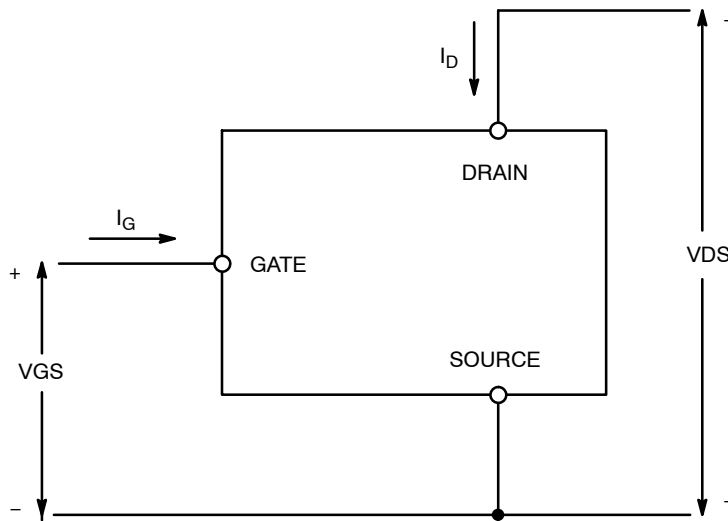


Figure 1. Voltage and Current Convention

NCV8402D, NCV8402AD

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3)	V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C	V _{(BR)DSS}	42	46	55	V
	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5)		40	45	55	
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C	I _{DSS}		0.25	4.0	μA
	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5)			1.1	20	
Gate Input Current	V _{DS} = 0 V, V _{GS} = 5.0 V	I _{GSSF}		50	100	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 150 μA	V _{GS(th)}	1.3	1.8	2.2	V
Gate Threshold Temperature Coefficient		V _{GS(th)} /T _J		4.0	6.0	-mV/°C
Static Drain-to-Source On-Resistance	V _{GS} = 10 V, I _D = 1.7 A, T _J = 25°C	R _{DS(on)}		165	200	mΩ
	V _{GS} = 10 V, I _D = 1.7 A, T _J = 150°C (Note 5)			305	400	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 25°C			195	230	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 150°C (Note 5)			360	460	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C			190	230	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 5)			350	460	
Source-Drain Forward On Voltage	V _{GS} = 0 V, I _S = 7.0 A	V _{SD}		1.0		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Time (10% V _{IN} to 90% I _D)	V _{GS} = 10 V, V _{DD} = 12 V, I _D = 2.5 A, R _L = 4.7 Ω	t _{on}		25	30	μs
Turn-Off Time (90% V _{IN} to 10% I _D)		t _{off}		120	200	μs
Turn-On Rise Time (10% I _D to 90% I _D)		t _{rise}		20	25	μs
Turn-Off Fall Time (90% I _D to 10% I _D)		t _{fall}		50	70	μs
Slew-Rate ON (70% V _{DS} to 50% V _{DD})		-dV _{DS} /dt _{ON}		0.8	1.2	V/μs
Slew-Rate OFF (50% V _{DS} to 70% V _{DD})		dV _{DS} /dt _{OFF}		0.3	0.5	

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)

Current Limit	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 25°C	I _{LIM}	3.7	4.3	5.0	A
	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Note 5)		2.3	3.0	3.7	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C		4.2	4.8	5.4	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Note 5)		2.7	3.6	4.5	
Temperature Limit (Turn-off)	V _{GS} = 5.0 V (Note 5)	T _{LIM(off)}	150	175	200	°C
Thermal Hysteresis	V _{GS} = 5.0 V	ΔT _{LIM(on)}		15		
Temperature Limit (Turn-off)	V _{GS} = 10 V (Note 5)	T _{LIM(off)}	150	165	185	
Thermal Hysteresis	V _{GS} = 10 V	ΔT _{LIM(on)}		15		

GATE INPUT CHARACTERISTICS (Note 5)

Device ON Gate Input Current	V _{GS} = 5 V, I _D = 1.0 A	I _{GON}		50		μA
	V _{GS} = 10 V, I _D = 1.0 A			400		
Current Limit Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GCL}		0.05		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.4		
Thermal Limit Fault Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GTL}		0.15		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.7		

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)		400			

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

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TYPICAL PERFORMANCE CURVES

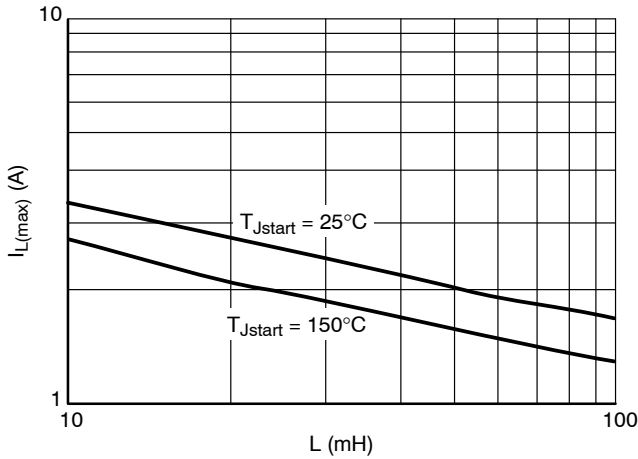


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

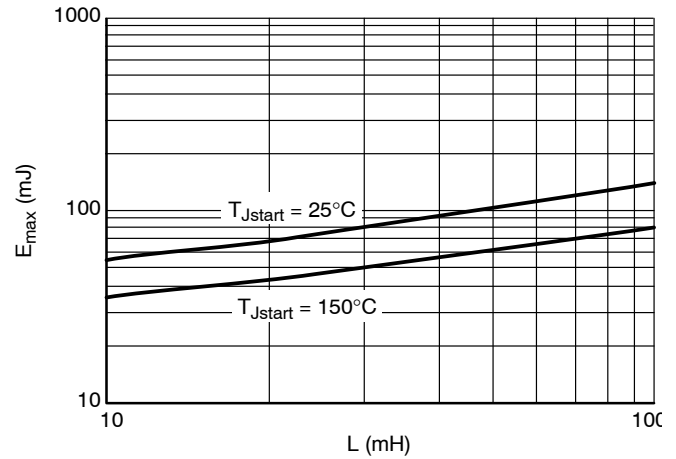


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

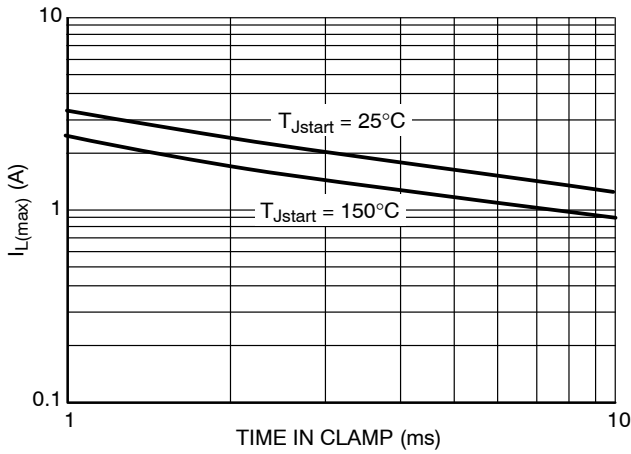


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

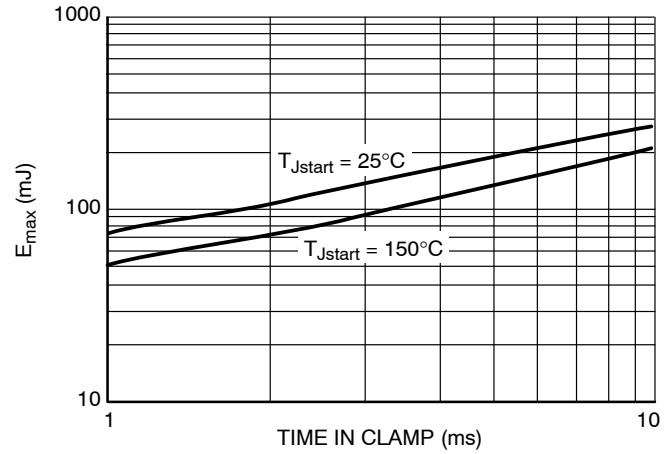


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

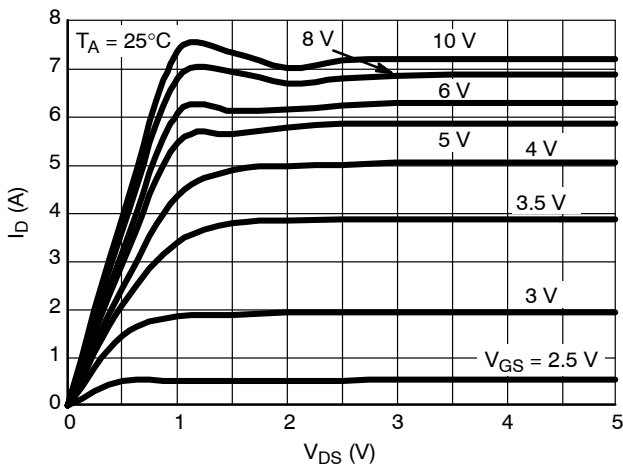


Figure 6. On-state Output Characteristics

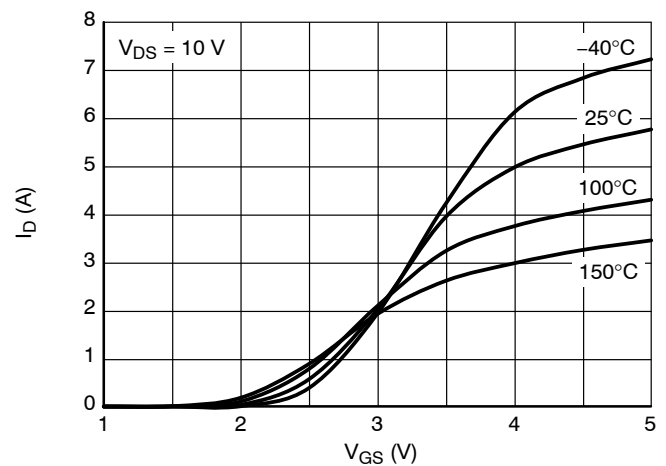


Figure 7. Transfer Characteristics

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TYPICAL PERFORMANCE CURVES

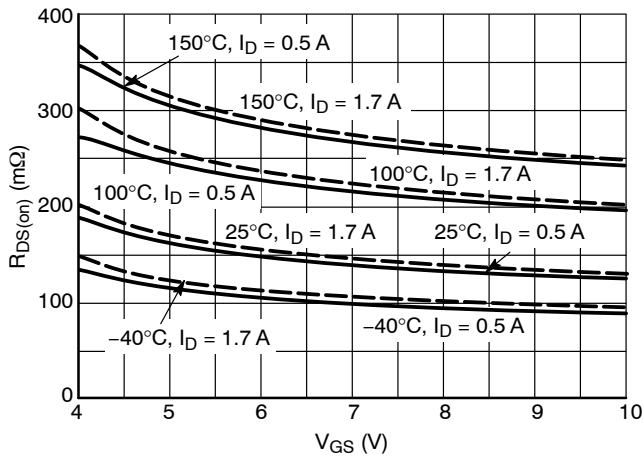


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

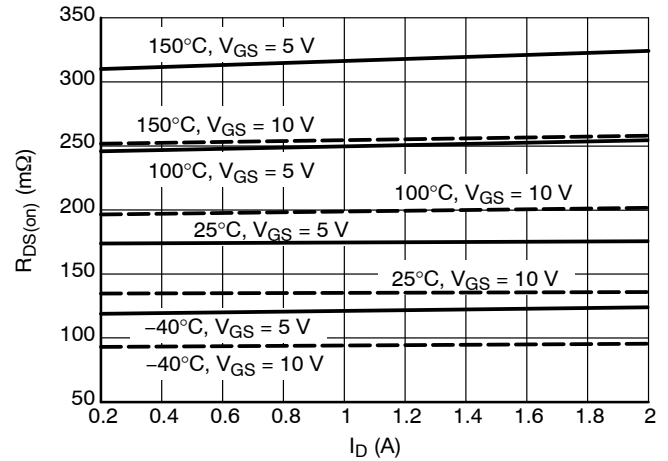


Figure 9. $R_{DS(on)}$ vs. Drain Current

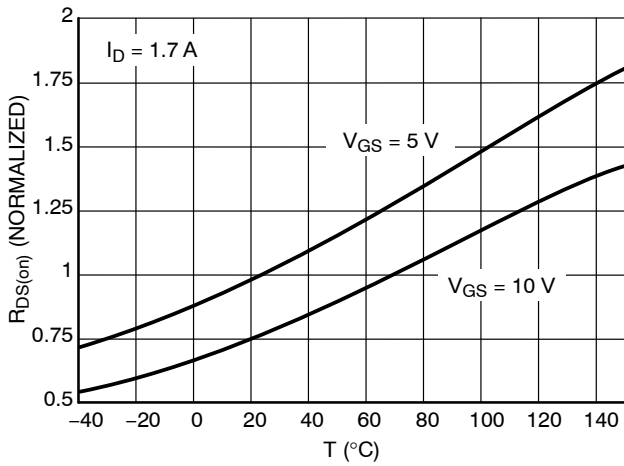


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

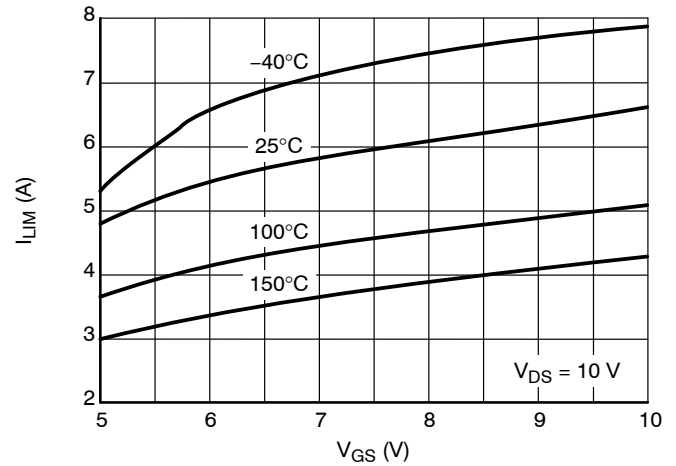


Figure 11. Current Limit vs. Gate-Source Voltage

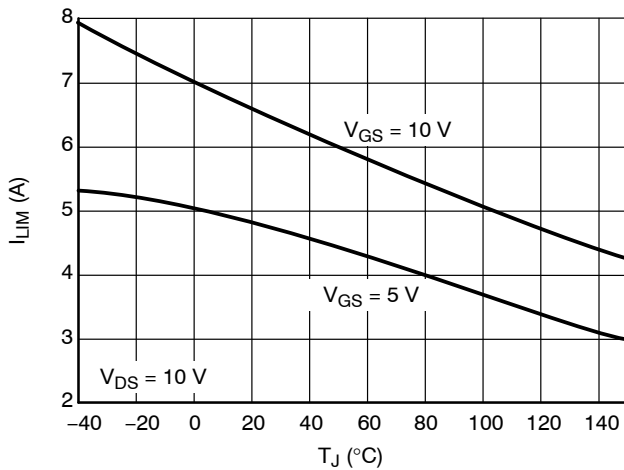


Figure 12. Current Limit vs. Junction Temperature

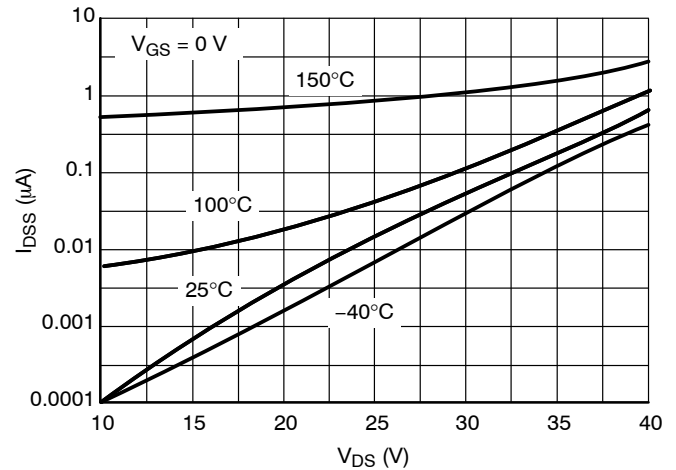


Figure 13. Drain-to-Source Leakage Current

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TYPICAL PERFORMANCE CURVES

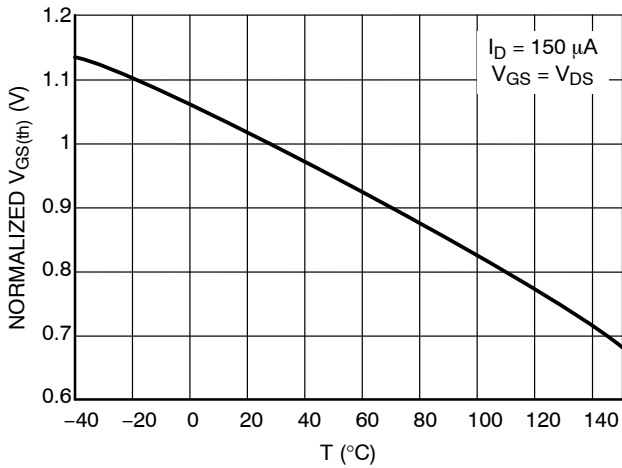


Figure 14. Normalized Threshold Voltage vs. Temperature

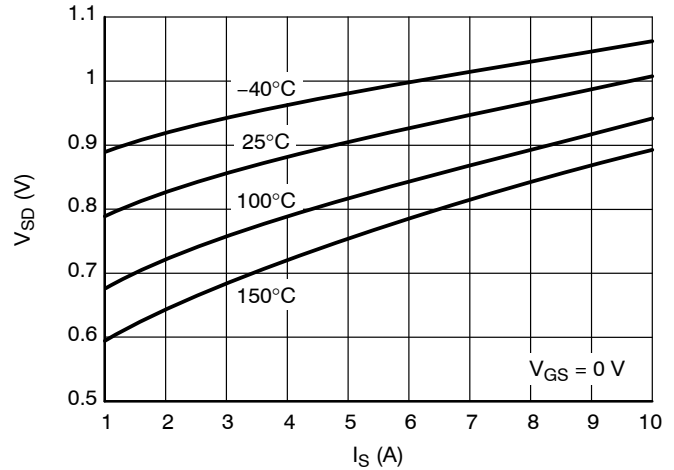


Figure 15. Source-Drain Diode Forward Characteristics

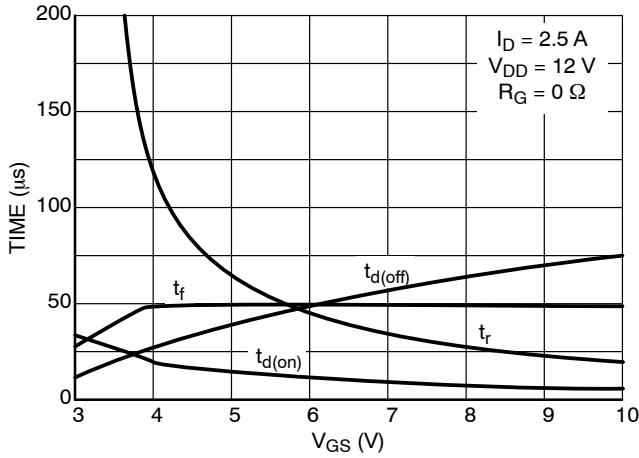


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

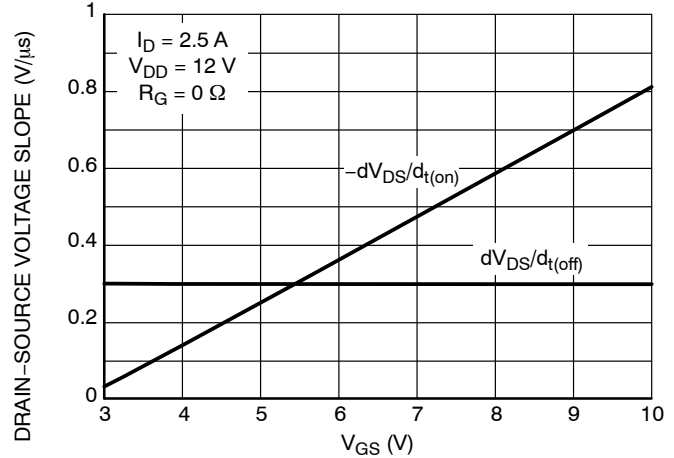


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

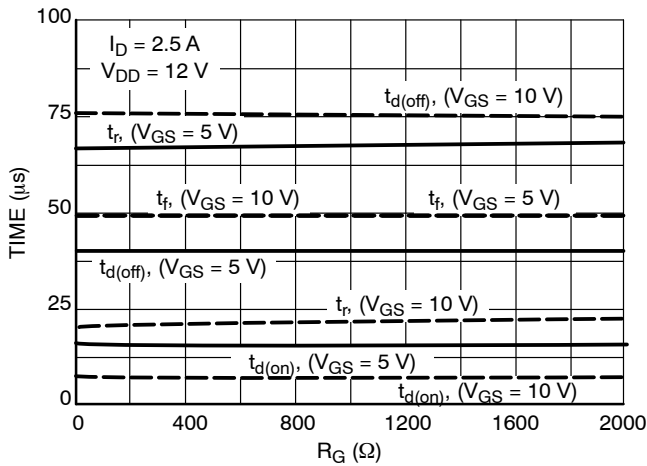


Figure 18. Resistive Load Switching Time vs. Gate Resistance

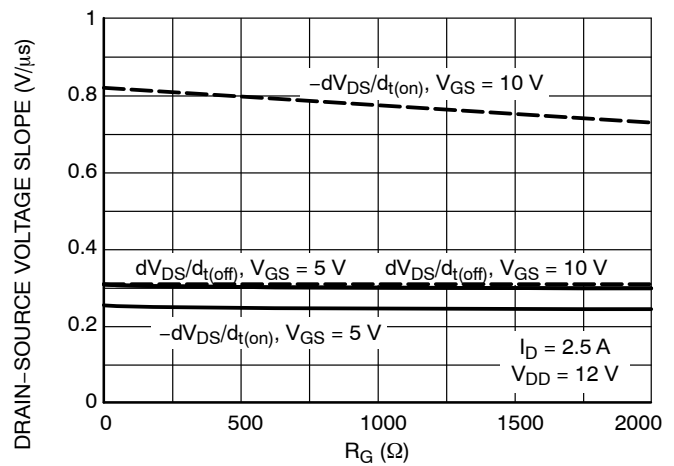


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

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TYPICAL PERFORMANCE CURVES

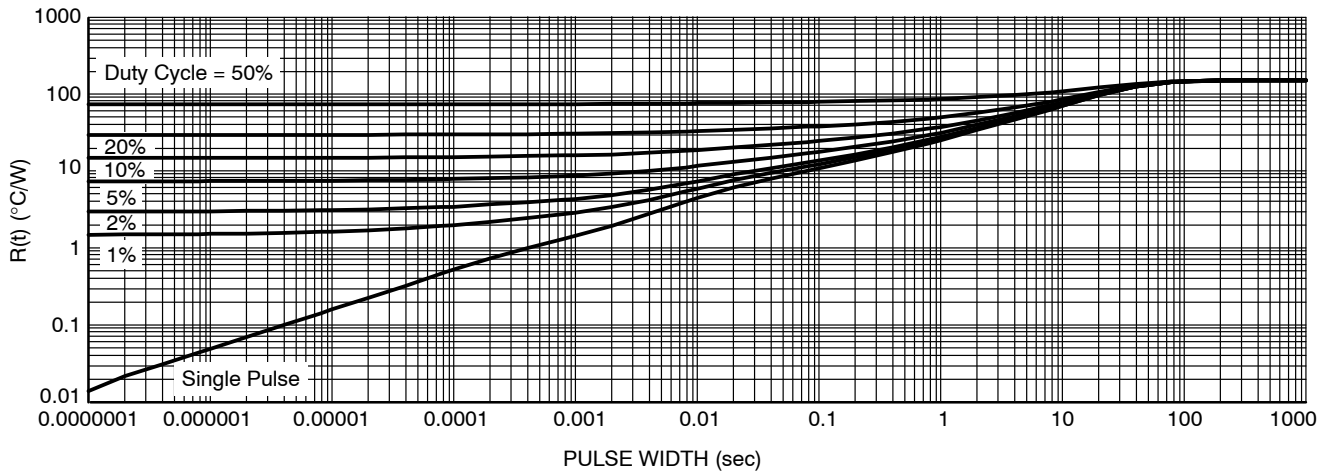


Figure 20. Transient Thermal Resistance

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TEST CIRCUITS AND WAVEFORMS

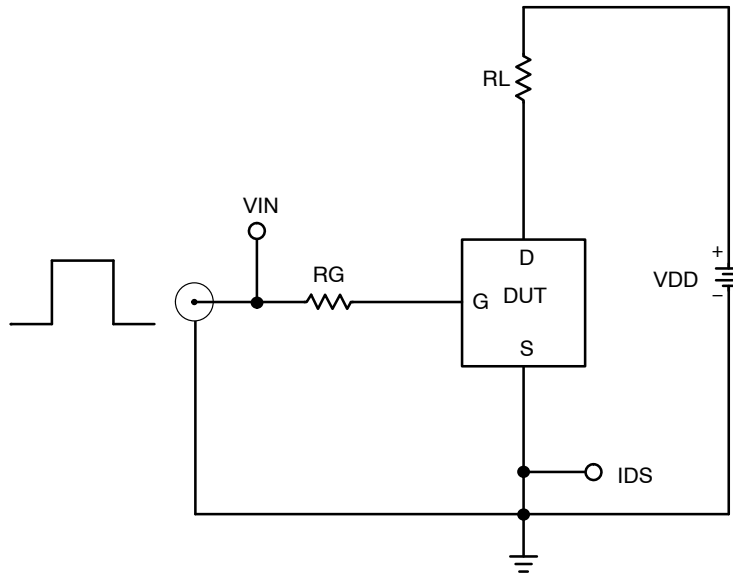


Figure 21. Resistive Load Switching Test Circuit

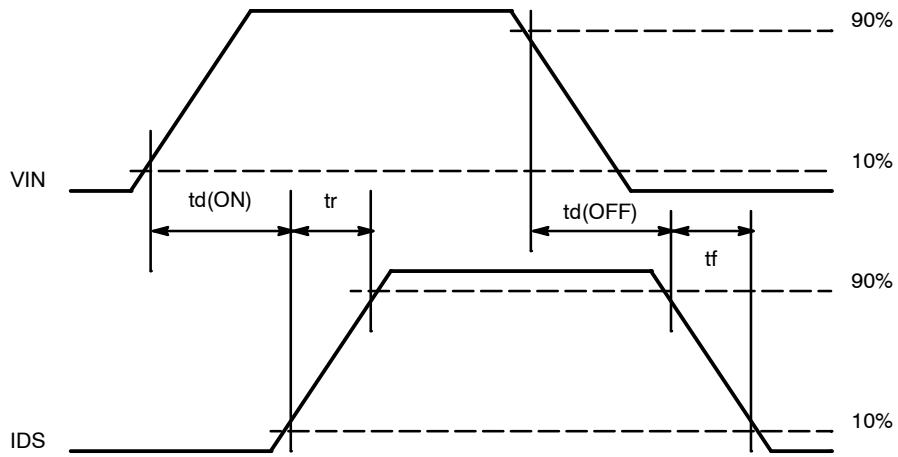


Figure 22. Resistive Load Switching Waveforms

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TEST CIRCUITS AND WAVEFORMS

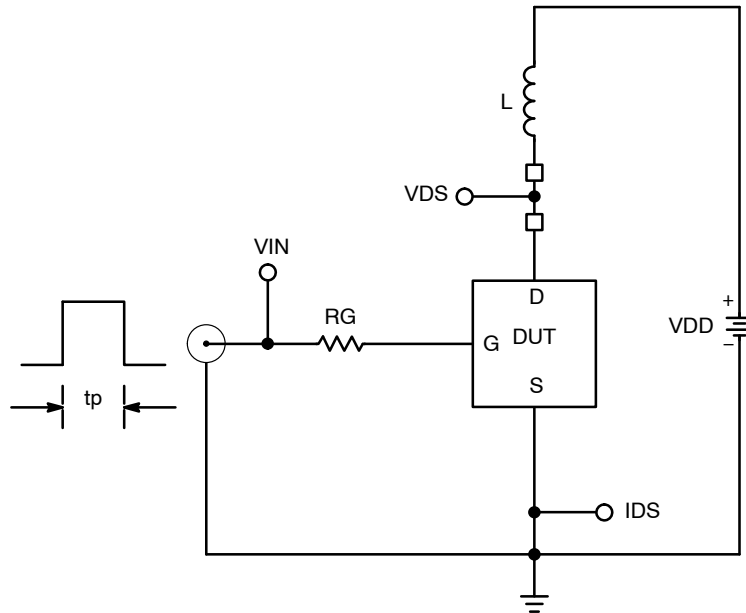


Figure 23. Inductive Load Switching Test Circuit



Figure 24. Inductive Load Switching Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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