### **General Description**

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator, and the MAX13047E is a dual-channel translator. Externally applied voltages, V<sub>CC</sub> and V<sub>L</sub>, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction (V<sub>L</sub>↔V<sub>CC</sub>) on any single data line. The MAX13046E/MAX13047E accept V<sub>L</sub> from +1.1V to the minimum of either +3.6V or (V<sub>CC</sub> + 0.3V), and V<sub>CC</sub> from +1.65V to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1µA thermal short-circuit protection, and  $\pm$ 15kV ESD protection on the V<sub>CC</sub> side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when push-pull driving is used.

The MAX13046E is available in a 6-pin  $\mu$ DFN package, and the MAX13047E is available in a 10-pin UTQFN. Both devices are specified over the extended -40°C to +85°C operating temperature range.

### **Applications**

- I<sup>2</sup>C and 1-Wire<sup>®</sup> Level Translation
- CMOS Logic-Level Translation
- Cell Phones
- Portable Devices

### **Ordering Information/Selector Guide**

PART	PIN-PACKAGE	NUMBER OF CHANNELS	TOP MARK	
MAX13046EELT+	6 μDFN (1mm x 1.5mm)	1	ос	
MAX13047EEVB+	10 UTQFN (1.4mm x 1.8mm)	2	AAC	

**Note:** All devices are specified over the extended -40°C to +85°C operating temperature range.

+Denotes a lead-free/RoHS-compliant package.

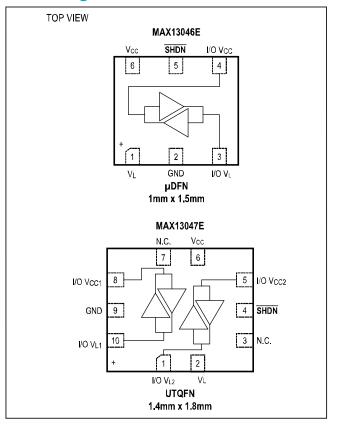
1-Wire is a registered trademark of Maxim Integrated Products, Inc.

# Single- and Dual-Bidirectional Low-Level Translator

#### **Features**

- Bidirectional Level Translation
- Operation Down to +1.1V on VL
- Ultra-Low Supply Current in Shutdown Mode 1µA (max)
- Guaranteed Push-Pull Driving Data Rate
  - 8Mbps (+1.2V  $\leq$  V<sub>L</sub>  $\leq$  +3.6V, V<sub>CC</sub>  $\leq$  +5.5V)
  - 16Mbps (+1.8V  $\leq$  V<sub>L</sub>  $\leq$  V<sub>CC</sub>  $\leq$  +3.3V)
- Extended ESD Protection on the I/O V<sub>CC</sub> Lines
  - ±15kV Human Body Model
  - ±15kV IEC61000-4-2 Air-Gap Discharge Method
  - ±8kV IEC61000-4-2 Contact Discharge
- Low Supply Current
- Short-Circuit Protection
- Space-Saving µDFN and UTQFN Packages

### **Pin Configurations**



Typical Application Circuits appear at end of data sheet.



## Single- and Dual-Bidirectional Low-Level Translator

### **Absolute Maximum Ratings**

(All voltages referenced to GND.)
V <sub>CC</sub> 0.3V to +6V
VI0.3V to +4V
$1/\overline{O}$ V <sub>CC</sub> 0.3V to (V <sub>CC</sub> + 0.3V)
I/O V <sub>1</sub> 0.3V to (V <sub>1</sub> + 0.3V)
SHDN0.3V to +6V
Short-Circuit Duration I/O V <sub>I</sub> , I/O V <sub>CC</sub> to GND Continuous
Power Dissipation ( $T_A = +70^{\circ}C$ )
6-Pin µDFN (derate 2.1mW/°C above +70°C)168mW
10-Pin UTQFN (derate 6.9mW/°C above +70°C)559mW

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$	) (Note 1)
6-Pin µDFN	477°C/W
10-Pin UTQFN	20.1°C/W
Junction-to-Ambient Thermal Resistance (θ <sub>JC</sub>	) (Note 1)
6-Pin μDFN	20.1°C/W
10-Pin UTQFN	143.1°C/W
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **Electrical Characteristics**

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.1V to minimum of either +3.6V or ((V<sub>CC</sub> + 0.3V)), I/O V<sub>L</sub> and I/O V<sub>CC</sub> are unconnected, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are V<sub>CC</sub> = +3.3V, V<sub>L</sub> = +1.8V at T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
POWER SUPPLY	•						
V Supply Bongo	V	V <sub>CC</sub> > 3.3V	1.1		3.6V	V	
V <sub>L</sub> Supply Range	VL	$V_{CC} \le 3.3V$	1.1	Vc	<sub>C</sub> + 0.3V	V	
V <sub>CC</sub> Supply Range	V <sub>CC</sub>		1.65		5.5	V	
Supply Current from V <sub>CC</sub>	IQVCC				10	μA	
Supply Current from VL	I <sub>QVL</sub>				15	μA	
V <sub>CC</sub> Shutdown-Mode Supply Current	I <sub>SD-VCC</sub>	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.03	1	μA	
V <sub>L</sub> Shutdown-Mode Supply Current	I <sub>SD-VL</sub>	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.03	1	μA	
I/O V <sub>L</sub> and I/O V <sub>CC</sub> Shutdown-Mode Leakage Current	I <sub>SD-LKG</sub>	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.02	0.5	μA	
SHDN Input Leakage		T <sub>A</sub> = +25°C		0.02	0.1	μA	
ESD PROTECTION							
		Human Body Model		±15V			
I/O V <sub>CC</sub> (Note 4)		IEC 61000-4-2 Air-Gap Discharge		±15V		kV	
		IEC 61000-4-2 Contact Discharge		±8V			
All Other Pins		Human Body Model		±2		kV	
LOGIC-LEVEL THRESHOLDS	-						
I/O V <sub>L</sub> Input-Voltage High	VIHL		V <sub>L</sub> - 0.2			V	
I/O V <sub>L</sub> Input-Voltage Low	V <sub>ILL</sub>				0.15	V	

# Single- and Dual-Bidirectional Low-Level Translator

### **Electrical Characteristics (continued)**

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.1V to minimum of either +3.6V or ((V<sub>CC</sub> + 0.3V)), I/O V<sub>L</sub> and I/O V<sub>CC</sub> are unconnected, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are V<sub>CC</sub> = +3.3V, V<sub>L</sub> = +1.8V at T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V <sub>CC</sub> Input-Voltage High	VIHC		V <sub>CC</sub> - 0.4			V
I/O V <sub>CC</sub> Input-Voltage Low	VILC				0.15	V
I/O V <sub>L</sub> Output-Voltage High	V <sub>OHL</sub>	$I/O V_L$ source current = 20µA, $V_{I/O VCC} > V_{CC} - 0.4V$	0.67 x V <sub>L</sub>			V
I/O V <sub>L</sub> Output-Voltage Low	V <sub>OLL</sub>	I/O V <sub>L</sub> sink current = 1mA, V <sub>I/O VCC</sub> < 0.15V			0.4	V
I/O V <sub>CC</sub> Output-Voltage High	V <sub>OHC</sub>	I/O V <sub>CC</sub> source current = 20 $\mu$ A, V <sub>I/O VL</sub> > V <sub>L</sub> - 0.2V	0.67 x V <sub>CC</sub>			V
I/O V <sub>CC</sub> Output-Voltage Low	V <sub>OLC</sub>	I/O V <sub>CC</sub> sink current = 1mA, V <sub>I/O VL</sub> < 0.15V			0.4	V
SHDN Input-Voltage High	V	V <sub>L</sub> > 1.2	V <sub>L</sub> - 0.2			- V
	VIH-SHDN	$1.1 \le V_L \le 1.2$	V <sub>L</sub> - 0.1			v
SHDN Input-Voltage Low	VIL-SHDN				0.15	V
I/O V <sub>L</sub> -to-I/O V <sub>CC</sub> Resistance				80	250	Ω
V <sub>CC</sub> Shutdown Threshold Low	V <sub>TH_L_VCC</sub>	$V_{CC}$ falling, $V_{L}$ = +3.3V	0.5	0.8	1.1	V
V <sub>CC</sub> Shutdown Threshold High	V <sub>TH_H_VCC</sub>	$V_{CC}$ rising, $V_{L}$ = +3.3V	0.3	0.6	0.9	V
V <sub>L</sub> Shutdown Threshold	V <sub>TH_VL</sub>		0.35	0.75	1.06	V
Pullup Resistance		$V_{CC} = V_{L} = +3.3V$	6	10	15.5	kΩ
RISE/FALL-TIME ACCELERATOR ST	AGE	-	I			
Accelerator Pulse Duration				20		ns
I/O V <sub>L</sub> Output-Accelerator Source Impedance		V <sub>L</sub> = 1.7V		13		Ω
I/O V <sub>CC</sub> Output-Accelerator Source Impedance		V <sub>CC</sub> = 2.2V		17		Ω
I/O V <sub>L</sub> Output-Accelerator Source Impedance		V <sub>L</sub> = 3.2V		6		Ω
I/O V <sub>CC</sub> Output-Accelerator Source Impedance		V <sub>CC</sub> = 3.6V		10		Ω

# Single- and Dual-Bidirectional Low-Level Translator

## Timing Characteristics For $+1.2V \le V_L \le Minimum Of Either +3.6V OR (V_{CC} + 0.3V)$

 $(V_{CC} \le \pm 5.5V, +1.2V \le V_L \le \text{minimum of either +3.6V or } ((V_{CC} + 0.3V)), R_S = 50\Omega, R_L = 1M\Omega, C_L = 15\text{pF}, T_A = -40^\circ\text{C to +85}^\circ\text{C}, \text{ unless otherwise noted. Typical values are } V_{CC} = +3.3V, V_L = +1.8V \text{ at } T_A = +25^\circ\text{C}.) \text{ (Notes 2, 3, 5)}$ 

PARAMETER	SYMBOL	CONDI	TIONS	MIN	TYP	MAX	UNITS
		Push-pull driving, Figure	Push-pull driving, Figure 1a			25	
I/O V <sub>CC</sub> Rise Time	<sup>t</sup> RVCC	Open-drain driving, Figur	re 1c		170	400	ns
		Push-pull driving, Figure	1a		6	37	
I/O V <sub>CC</sub> Fall Time	<sup>t</sup> FVCC	Open-drain driving, Figur	re 1c		20	50	ns
		Push-pull driving, Figure	1b		8	30	
I/O V <sub>L</sub> Rise Time	t <sub>RVL</sub>	Open-drain driving, Figure 1d			180	400	ns
	, F	Push-pull driving, Figure 1			3	56	
I/O V <sub>L</sub> Fall Time	t <sub>FVL</sub>	Open-drain driving, Figure 1d			30	60	) ns
	t <sub>PD-VL-VCC</sub>	-VCC Driving I/O VL	Push-pull driving		5	30	ns
Draw a wation Dalaw			Open-drain driving		210	1000	
Propagation Delay			Push-pull driving		4	30	
	<sup>t</sup> PD-VCC-VL	Driving I/O V <sub>CC</sub>	Open-drain driving		190	1000	
		Each translator equally	Push-pull driving			20	
Channel-to-Channel Skew	tskew	loaded	Open-drain driving			50	ns
Maximum Data Data		Push-pull driving	·	8			Mbps
Maximum Data Rate		Open-drain driving		500			kbps

### Timing Characteristics For $\pm 1.1V \le V_L \le \pm 1.2V$

 $(V_{CC} \le \pm 5.5V, +1.1V \le V_L \le +1.2V, R_S = 50\Omega, R_L = 1M\Omega, C_L = 15pF, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted. Typical values are } V_{CC} = +3.3V, V_L = +1.8V \text{ at } T_A = +25^{\circ}C.) \text{ (Notes 2, 3, 5)}$ 

PARAMETER	SYMBOL	COND	ITIONS	MIN	TYP	MAX	UNITS
	+	Push-pull driving, Figure	Push-pull driving, Figure 1a			200	
I/O V <sub>CC</sub> Rise Time	t <sub>RVCC</sub>	Open-drain driving, Figu	ire 1c		170	400	ns
		Push-pull driving, Figure	e 1a		6	37	
I/O V <sub>CC</sub> Fall Time	<sup>t</sup> FVCC	Open-drain driving, Figu	ire 1c		20	50	ns
	1	Push-pull driving, Figure	e 1b		8	30	
I/O V <sub>L</sub> Rise Time	t <sub>RVL</sub>	Open-drain driving, Figure 1d			180	400	loo ns
		Push-pull driving, Figure	e 1		3	30	
I/O V <sub>L</sub> Fall Time	t <sub>FVL</sub>	Open-drain driving, Figure 1d			30	60	ns
	t <sub>PD-VL-VCC</sub>	Driving I/O VL	Push-pull driving		5	200	ns
Draw a wation Dalaw			Open-drain driving		210	1000	
Propagation Delay		Driving I/O V <sub>CC</sub>	Push-pull driving		4	200	
	<sup>t</sup> PD-VCC-VL		Open-drain driving		190	1000	
Channel to Channel Skow	4	Each translator equally	Push-pull driving			20	
Channel-to-Channel Skew	<sup>t</sup> SKEW	loaded	Open-drain driving			50 ns	ns
Maximum Data Rate		Push-pull driving		1.2			Mbps
	<u> </u>	Open-drain driving		500			kbps

# Single- and Dual-Bidirectional Low-Level Translator

### Timing Characteristics For +1.8V $\leq$ V<sub>L</sub> $\leq$ V<sub>CC</sub> $\leq$ +3.3V

(+1.8V  $\leq$  V<sub>L</sub>  $\leq$  V<sub>CC</sub>  $\leq$  +3.3V, R<sub>S</sub> = 50 $\Omega$ , R<sub>L</sub> = 1M $\Omega$ , C<sub>L</sub> = 15pF, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are V<sub>CC</sub> = +3.3V, V<sub>L</sub> = +1.8V at T<sub>A</sub> = +25°C.) (Notes 2, 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V <sub>CC</sub> Rise Time	t <sub>RVCC</sub>	Push-pull driving, Figure 1a			15	ns
I/O V <sub>CC</sub> Fall Time	t <sub>FVCC</sub>	Push-pull driving, Figure 1a			15	ns
I/O V <sub>L</sub> Rise Time	t <sub>RVL</sub>	Push-pull driving, Figure 1b			15	ns
I/O V <sub>L</sub> Fall Time	t <sub>FVL</sub>	Push-pull driving, Figure 1b			15	ns
Propagation Dalay	t <sub>PD-VL-VCC</sub>	Push-pull driving, driving I/O $V_L$			15	
Propagation Delay	tPD-VCC-VL	Push-pull driving, driving I/O $V_{CC}$			15	ns
Channel-to-Channel Skew	<sup>t</sup> SKEW	Push-pull driving, each translator equally loaded			10	ns
Maximum Data Rate		Push-pull driving	16			Mbps

**Note 2:** All units are 100% production tested at  $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: For normal operation, ensure  $V_L < (V_{CC} + 0.3V)$ . During power-up,  $V_L > (V_{CC} + 0.3V)$  does not damage the device.

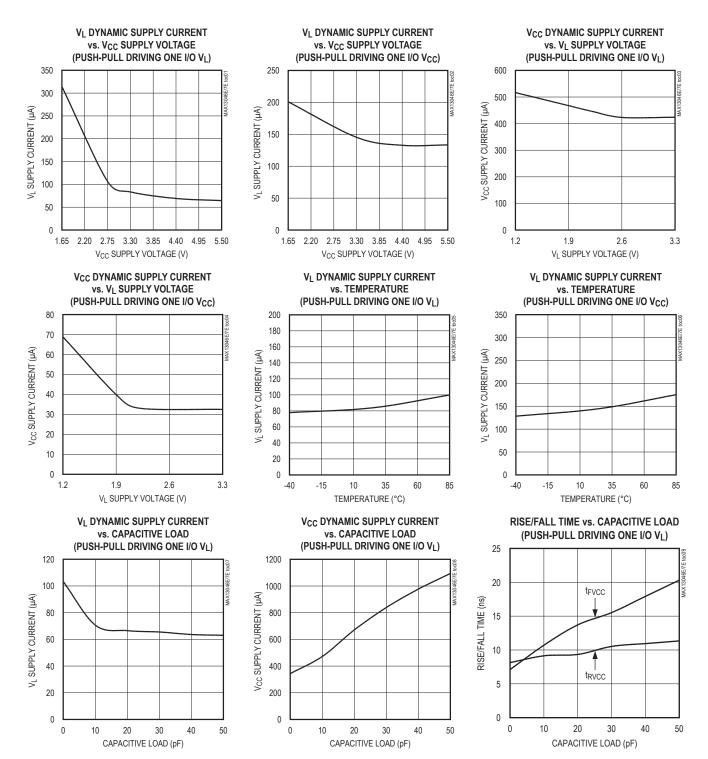
Note 4: ESD protection is guaranteed by design. To ensure maximum ESD protection, place a 1µF ceramic capacitor between V<sub>CC</sub> and GND. See *Typical Application Circuits*.

Note 5: Timing is measured using 10% of input to 90% of output.

# Single- and Dual-Bidirectional Low-Level Translator

### **Typical Operating Characteristics**

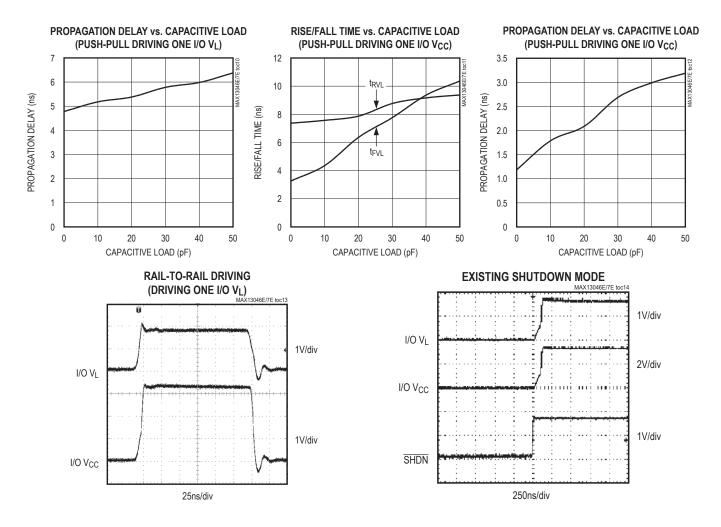
 $(V_{CC} = +3.3V, V_L = +1.8V, R_L = 1M\Omega, C_L = 15pF$ , push-pull driving data rate = 8Mbps,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Single- and Dual-Bidirectional Low-Level Translator

## **Typical Operating Characteristics (continued)**

 $(V_{CC} = +3.3V, V_L = +1.8V, R_L = 1M\Omega, C_L = 15pF$ , push-pull driving data rate = 8Mbps,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Single- and Dual-Bidirectional Low-Level Translator

### MAX13046E Pin Description

MAX13046E		FUNCTION
μDFN	NAME	
1	VL	$V_L$ Input Supply Voltage. Bypass $V_L$ with a 0.1 $\mu$ F ceramic capacitor located as close as possible to the input.
2	GND	Ground
3	I/O V <sub>L</sub>	Input/Output. Referenced to V <sub>L</sub> .
4	I/O V <sub>CC</sub>	Input/Output. Referenced to V <sub>CC</sub> .
5	SHDN	Shutdown Input. Drive SHDN high to enable the device. Drive SHDN low to put the device in shutdown mode.
6	V <sub>CC</sub>	$V_{CC}$ Input Supply Voltage. Bypass $V_{CC}$ with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass $V_{CC}$ with a 0.1µF ceramic capacitor.

### **MAX13047E Pin Description**

MAX13047E		FUNCTION
UTQFN	NAME	
1	I/O V <sub>L2</sub>	Input/Output 2. Referenced to VL.
2	VL	$V_L$ Input Supply Voltage. Bypass $V_L$ with a 0.1 $\mu$ F ceramic capacitor located as close as possible to the input.
3, 7	N.C.	Not Connected. Internally not connected.
4	SHDN	Enable Input. Drive SHDN high to enable the device. Drive SHDN low to put the device in shutdown mode.
5	I/O V <sub>CC2</sub>	Input/Output 2. Referenced to V <sub>CC</sub> .
6	V <sub>CC</sub>	$V_{CC}$ Input Supply Voltage. Bypass $V_{CC}$ with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass $V_{CC}$ with a 0.1µF ceramic capacitor.
8	I/O V <sub>CC1</sub>	Input/Output 1. Referenced to V <sub>CC</sub> .
9	GND	Ground
10	I/O V <sub>L1</sub>	Input/Output 1. Referenced to V <sub>L</sub> .

#### **Detailed Description**

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator and the MAX13047E is a dual-channel translator. Externally applied voltages, V<sub>CC</sub> and V<sub>L</sub>, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction (V<sub>L</sub>  $\leftrightarrow$  V<sub>CC</sub>) on any single data line. The MAX13046E/MAX13047E accept V<sub>L</sub> from +1.1V to the minimum of either +3.6V or (V<sub>CC</sub> + 0.3V) and V<sub>CC</sub> from +1.65V

to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1 $\mu$ A thermal short-circuit protection, and ±15kV ESD protection on the V<sub>CC</sub> side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when push-pull driving is used. See the *Functional Diagram*.

# Single- and Dual-Bidirectional Low-Level Translator

### VL V<sub>CC</sub> ONE-SHOT ONE-SHOT RISE-TIME RISE-TIME PU1 PU2 ACCELERATOR ACCELERATOR ><sub>10kΩ</sub> 10kΩ GATE BIAS $I/O V_L$ I/O V<sub>CC</sub> Ν SHDN GND

## **Functional Diagram**

#### **Level Translation**

For proper operation, ensure that +1.65V  $\leq$  V<sub>CC</sub>  $\leq$  +5.5V and +1.1V  $\leq$  V<sub>L</sub>  $\leq$  the minimum of either +3.6V or (V<sub>CC</sub> + 0.3V). During power-up sequencing, V<sub>L</sub>  $\geq$  (V<sub>CC</sub> + 0.3V) does not damage the device. The speed of the rise time accelerator circuitry limits the maximum data rate for the MAX13046E/MAX13047E to 16Mbps.

#### **Rise-Time Accelerators**

The MAX13046E/MAX13047E have an internal rise-time accelerator, allowing operation up to 16Mbps. The rise-time accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To guarantee operation of the rise time accelerators the maximum parasitic capacitance should be less than 200pF on the I/O lines.

#### **Shutdown Mode**

Drive  $\overline{SHDN}$  low to place the MAX13046E/MAX13047E in shutdown mode and drive  $\overline{SHDN}$  high for normal operation. Activating the shutdown mode disconnects the internal 10k $\Omega$  pullup resistors on the I/O V<sub>CC</sub> and I/O V<sub>L</sub> lines. This forces the I/O lines to a high-impedance state, and

decreases the supply current to less than 1µA. The highimpedance I/O lines in shutdown mode allow for use in a multidrop network. The MAX13046E/MAX13047E have a diode from each I/O to the corresponding supply rail and GND. Therefore, when in shutdown mode, do not allow the voltage at I/O V<sub>L</sub> to exceed (V<sub>L</sub> + 0.3V), or the voltage at I/O V<sub>CC</sub> to exceed (V<sub>CC</sub> + 0.3V).

#### **Operation with One Supply Disconnected**

Certain applications require sections of circuitry to be disconnected to save power. When V<sub>L</sub> is connected and V<sub>CC</sub> is disconnected or connected to ground, the device enters shutdown mode. In this mode, I/O V<sub>L</sub> can still be driven without damage to the device; however, data does not translate from I/O V<sub>L</sub> to I/O V<sub>CC</sub>. If V<sub>CC</sub> falls more than V<sub>TH\_L</sub>V<sub>CC</sub> below V<sub>L</sub>, the device disconnects the pullup resistors at I/O V<sub>L</sub> and I/O V<sub>CC</sub>. To achieve the lowest possible supply current from V<sub>L</sub> when V<sub>CC</sub> is disconnected, it is recommended that the voltage at the V<sub>CC</sub> supply input be approximately equal to GND.

When V<sub>CC</sub> is connected and V<sub>L</sub> is less than V<sub>TH\_VL</sub>, the device enters shutdown mode. In this mode, I/O  $V_{CC}$  can still be driven without damage to the device; however, data does not translate from I/O V<sub>CC</sub> to I/O V<sub>L</sub>.

# Single- and Dual-Bidirectional Low-Level Translator

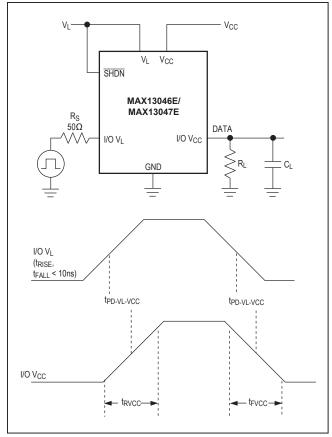


Figure 1a. Rail-to-Rail Driving I/O VL

When V<sub>CC</sub> is disconnected or connected to ground, I/O V<sub>CC</sub> must not be driven more than V<sub>CC</sub> + 0.3V. When V<sub>L</sub> is disconnected or connected to ground, I/O V<sub>L</sub> must not be driven more than V<sub>L</sub> + 0.3V.

#### **Short-Circuit Protection**

Thermal-overload detection protects the MAX13046E/ MAX13047E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature  $(T_J)$  exceeds +150°C, the device enters shutdown mode. When the device has cooled to below +140°C, normal operation resumes.

#### ±15kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The ESD structures withstand electrostatic discharge in all states: normal

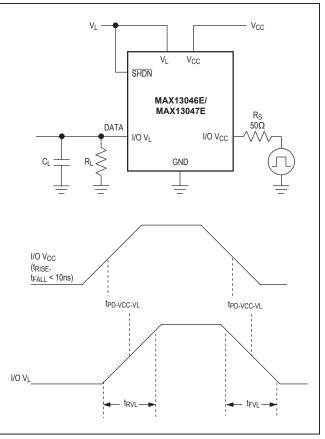


Figure 1b. Rail-to-Rail Driving I/O V<sub>CC</sub>

operation, shutdown mode, and powered down. The I/O  $V_{CC}$  lines of the MAX13046E/MAX13047E are characterized for protection to the following limit:

• ±15kV using the Human Body Model

#### **ESD Test Conditions**

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

#### Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a  $1.5k\Omega$  resistor.

# Single- and Dual-Bidirectional Low-Level Translator

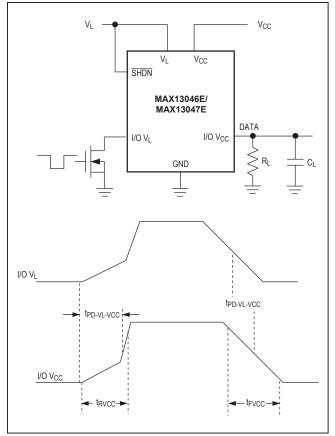


Figure 1c. Open-Drain Driving I/O VL

#### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX13046E/MAX13047E help to design equipment that meets Level 4 of IEC 61000-4-2 without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 can be lower than that measured using the Human Body Model. Figure 3a shows the IEC 61000-4-2 model, and Figure 3b shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD contact-discharge test. The Air-Gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

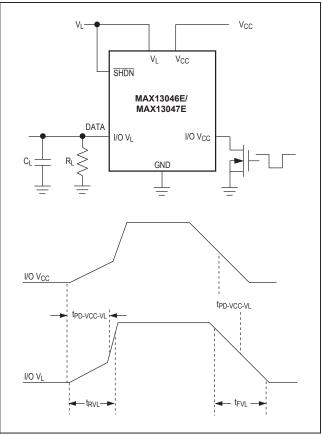


Figure 1d. Open-Drain Driving I/O V<sub>CC</sub>

### **Applications Information**

#### **Power-Supply Decoupling**

To reduce ripple and the chance of transmitting incorrect data, bypass V<sub>L</sub> and V<sub>CC</sub> to ground with a 0.1µF ceramic capacitor. To ensure full ±15kV ESD protection, bypass V<sub>CC</sub> to ground with a 1µF ceramic capacitor. Place all capacitors as close as possible to the power-supply inputs.

#### I<sup>2</sup>C Level Translation

The MAX13046E/MAX13047E level shifts the data present on the I/O lines between +1.1V and +5.5V, making them ideal for level translation between a low-voltage ASIC and an I<sup>2</sup>C device. A typical application involves interfacing a low-voltage microprocessor to a +3V or +5V D/A converter, such as the MAX517.

# Single- and Dual-Bidirectional Low-Level Translator

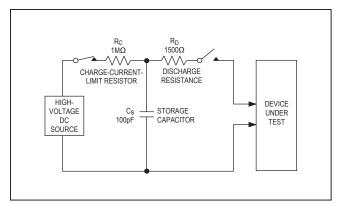


Figure 2a. Human Body ESD Test Model

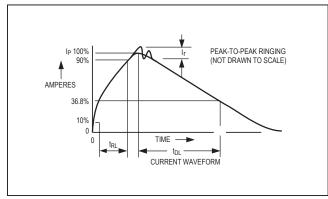


Figure 2b. Human Body Current Waveform

#### **1-Wire Interface Translation**

The MAX13046E/MAX13047E are ideal for level translation between a low-voltage ASIC and 1-Wire device. A typical application involves interfacing a low-voltage microprocessor to an external memory, such as the DS2502. The maximum data rate depends on the 1-Wire device. For the DS2502, the maximum data rate is 16.3kbps. A  $5k\Omega$  pullup resistor is recommended when interfacing with the DS2502.

#### Push-Pull vs. Open-Drain Driving

The MAX13046E/MAX13047E can be driven in a pushpull or open-drain configurations. For open-drain configuration, internal 10k $\Omega$  resistors pull up I/O V<sub>L</sub> and I/O V<sub>CC</sub> to their respective power supplies. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers.

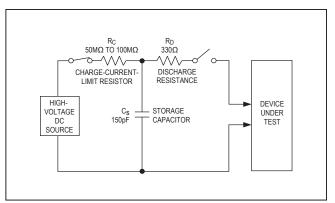


Figure 3a. IEC 61000-4-2 ESD Test Model

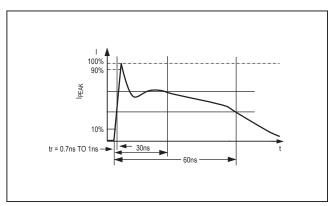


Figure 3b. IEC 61000-4-2 ESD Generator Current Waveform

### **PCB Layout**

The MAX13046E/MAX13047E require good PCB layout for proper operation and optimal rise/fall time performance. Ensure proper high-frequency PCB layout even when operating at low data rates.

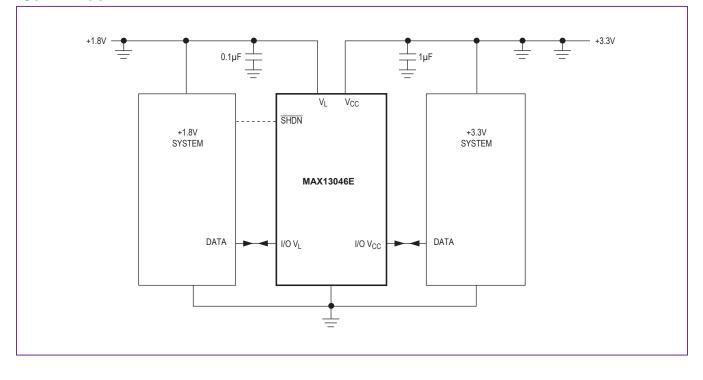
### **Driving High-Capacitive Load**

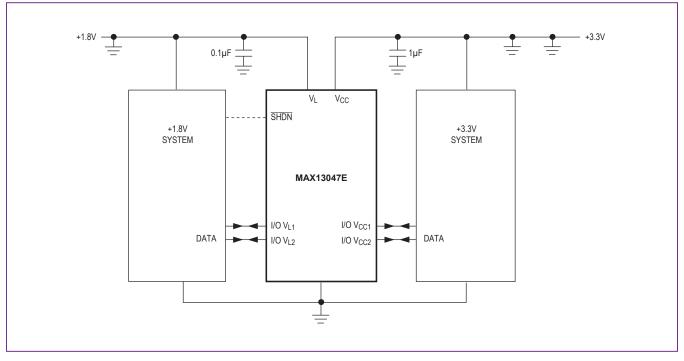
Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13046E/MAX13047E when driving the signal lines. The actual rise time is a function of the load capacitance, parasitic capacitance, the supply voltage, and the drive impedance of the MAX13046E/MAX13047E.

Operating the MAX13046E/MAX13047E at a low data rate does **NOT** increase capacitive load driving capability.

# Single- and Dual-Bidirectional Low-Level Translator

## **Typical Application Circuits**





# Single- and Dual-Bidirectional Low-Level Translator

## **Chip Information**

PROCESS: BICMOS

## **Package Information**

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO		
6 µDFN	L611-1	<u>21-0147</u>		
10 UTQFN	V101A1CN-1	<u>21-0028</u>		

# Single- and Dual-Bidirectional Low-Level Translator

## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	8/08	Removing future product asterisks from MAX13047, changing <i>Electrical Characteristics</i> Table, packaging changes, changing ESD information	1–4, 6, 10
2	10/19	Updated MAX13047E Pin Description table	8
3	7/21	Updated Pin Configurations.	1

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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