

#### FEATURES

##### High speed

- 41 MHz, -3 dB bandwidth
- 125 V/ $\mu$ s slew rate
- 80 ns settling time

Input bias current of 20 pA and noise current of 10 fA/ $\sqrt$ Hz

Input voltage noise of 12 nV/ $\sqrt$ Hz

Fully specified power supplies:  $\pm$ 5 V to  $\pm$ 15 V

Low distortion: -76 dB at 1 MHz

##### High output drive capability

- Drives unlimited capacitance load
- 50 mA min output current

No phase reversal when input is at rail

Available in 8-lead SOIC

#### APPLICATIONS

CCDs

Low distortion filters

Mixed gain stages

Audio amplifiers

Photo detector interfaces

ADC input buffers

DAC output buffers

#### GENERAL DESCRIPTION

The AD825 is a superbly optimized operational amplifier for high speed, low cost, and dc parameters, making it ideally suited for a broad range of signal conditioning and data acquisition applications. The ac performance, gain, bandwidth, slew rate, and drive capability are all very stable over temperature. The AD825 also maintains stable gain under varying load conditions.

The unique input stage has ultralow input bias current and input current noise. Signals that go to either rail on this high performance input do not cause phase reversals at the output. These features make the AD825 a good choice as a buffer for MUX outputs, creating minimal offset and gain errors.

The AD825 is fully specified for operation with dual  $\pm$ 5 V and  $\pm$ 15 V supplies. This power supply flexibility, and the low supply current of 6.5 mA with excellent ac characteristics under all supply conditions, makes the AD825 well-suited for many demanding applications.

#### CONNECTION DIAGRAMS

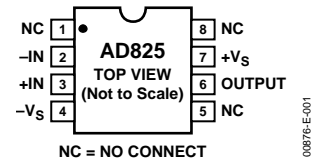


Figure 1. 8-Lead Plastic SOIC (R-8) Package

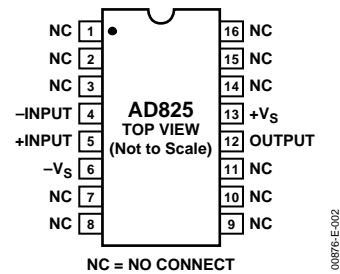


Figure 2. 16-Lead Plastic SOIC (RW-16) Package

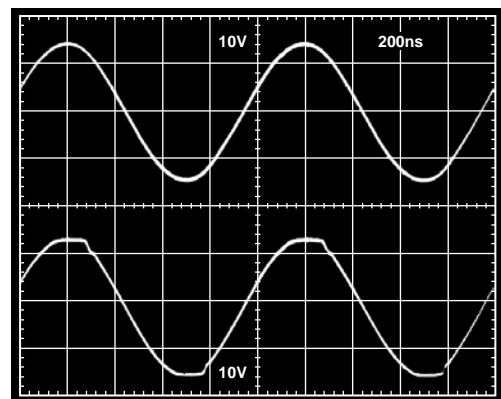


Figure 3. Performance with Rail-to-Rail Input Signals

Rev. G

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## REVISION HISTORY

### 4/14—Rev. F to Rev. G

Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 10/04—Data Sheet Changed from Rev. E to Rev. F

Changes to Figure 1.....	1
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### 3/04—Data Sheet Changed from Rev. D to Rev. E

Changes to Specifications .....	3
Addition of 16-Lead SOIC Pin Configuration .....	5
Changes to Figure 27.....	9
Updated Outline Dimensions .....	12
Updated Ordering Guide.....	12

### 2/01—Data Sheet Changed from Rev. C to Rev. D

Addition of 16-lead SOIC package (R-16)	
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Addition to Absolute Maximum Ratings .....	4
Addition to Ordering Guide (R-16).....	4
Addition of 16-lead SOIC package (R-16)	
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## SPECIFICATIONS

All limits are determined to be at least four standard deviations away from mean value. At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	Conditions	$V_S$	AD825A			Unit
			Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>						
Unity Gain Bandwidth		$\pm 15\text{ V}$	23	26		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	$\pm 15\text{ V}$	18	21		MHz
-3 dB Bandwidth	Gain = +1	$\pm 15\text{ V}$	44	46		MHz
Slew Rate	$R_{LOAD} = 1\text{ k}\Omega$ , $G = +1$	$\pm 15\text{ V}$	125	140		V/ $\mu\text{s}$
Settling Time to 0.1%	0 V to 10 V Step, $A_V = -1$	$\pm 15\text{ V}$		150	180	ns
to 0.1%	0 V to 10 V Step, $A_V = -1$	$\pm 15\text{ V}$		180	220	ns
Total Harmonic Distortion	$F_C = 1\text{ MHz}$ , $G = -1$	$\pm 15\text{ V}$		-77		dB
Differential Gain Error ( $R_{LOAD} = 150\ \Omega$ )	NTSC Gain = +2	$\pm 15\text{ V}$		1.3		%
Differential Phase Error ( $R_{LOAD} = 150\ \Omega$ )	NTSC Gain = +2	$\pm 15\text{ V}$		2.1		Degrees
<b>INPUT OFFSET VOLTAGE</b>						
	$T_{MIN}$ to $T_{MAX}$	$\pm 15\text{ V}$		1	2	mV
Offset Drift				10	5	mV $\mu\text{V}/^\circ\text{C}$
<b>INPUT BIAS CURRENT</b>						
	$T_{MIN}$	$\pm 15\text{ V}$	5	15	40	pA
	$T_{MAX}$				700	pA
<b>INPUT OFFSET CURRENT</b>						
	$T_{MIN}$	$\pm 15\text{ V}$	5	20	30	pA
	$T_{MAX}$				440	pA
<b>OPEN-LOOP GAIN</b>						
	$V_{OUT} = \pm 10\text{ V}$ $R_{LOAD} = 1\text{ k}\Omega$	$\pm 15\text{ V}$	70	76		dB
	$V_{OUT} = \pm 7.5\text{ V}$ $R_{LOAD} = 1\text{ k}\Omega$	$\pm 15\text{ V}$	70	76		dB
	$V_{OUT} = \pm 7.5\text{ V}$ $R_{LOAD} = 150\text{ k}\Omega$ (50 mA Output)	$\pm 15\text{ V}$	68	74		dB
<b>COMMON-MODE REJECTION</b>						
	$V_{CM} = \pm 10$	$\pm 15\text{ V}$	71	80		dB
<b>INPUT VOLTAGE NOISE</b>						
	$f = 10\text{ kHz}$	$\pm 15\text{ V}$		12		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT CURRENT NOISE</b>						
	$f = 10\text{ kHz}$	$\pm 15\text{ V}$		10		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT COMMON-MODE VOLTAGE RANGE</b>						
		$\pm 15\text{ V}$		$\pm 13.5$		V
<b>OUTPUT VOLTAGE SWING</b>						
	$R_{LOAD} = 1\text{ k}\Omega$	$\pm 15\text{ V}$	13	$\pm 13.3$		V
	$R_{LOAD} = 500\ \Omega$	$\pm 15\text{ V}$	12.9	$\pm 13.2$		V
Output Current		$\pm 15\text{ V}$	50			mA
Short-Circuit Current		$\pm 15\text{ V}$		100		mA
<b>INPUT RESISTANCE</b>						
				$5 \times 10^{11}$		$\Omega$
<b>INPUT CAPACITANCE</b>						
				6		pF
<b>OUTPUT RESISTANCE</b>						
	Open Loop			8		$\Omega$
<b>POWER SUPPLY</b>						
Quiescent Current		$\pm 15\text{ V}$		6.5	7.2	mA
	$T_{MIN}$ to $T_{MAX}$	$\pm 15\text{ V}$			7.5	mA

All limits are determined to be at least four standard deviations away from mean value. At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{ V}$  unless otherwise noted.

Table 2.

Parameter	Conditions	$V_S$	AD825A			Unit
			Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>						
Unity Gain Bandwidth		$\pm 5\text{ V}$	18	21		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	$\pm 5\text{ V}$	8	10		MHz
-3 dB Bandwidth	Gain = +1	$\pm 5\text{ V}$	34	37		MHz
Slew Rate	$R_{\text{LOAD}} = 1\text{ k}\Omega$ , $G = -1$	$\pm 5\text{ V}$	115	130		$\text{V}/\mu\text{s}$
Settling Time to 0.1% to 0.01%	-2.5 V to +2.5 V	$\pm 5\text{ V}$		75	90	ns
	-2.5 V to +2.5 V	$\pm 5\text{ V}$		90	110	ns
Total Harmonic Distortion	$F_c = 1\text{ MHz}$ , $G = -1$	$\pm 5\text{ V}$		-76		dB
Differential Gain Error ( $R_{\text{LOAD}} = 150\ \Omega$ )	NTSC Gain = +2	$\pm 5\text{ V}$		1.2		%
Differential Phase Error ( $R_{\text{LOAD}} = 150\ \Omega$ )	NTSC Gain = +2	$\pm 5\text{ V}$		1.4		Degrees
<b>INPUT OFFSET VOLTAGE</b>						
	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	$\pm 5\text{ V}$		1	2	mV
Offset Drift					5	mV
				10		$\mu\text{V}/^\circ\text{C}$
<b>INPUT BIAS CURRENT</b>						
	$T_{\text{MIN}}$	$\pm 5\text{ V}$		10	30	pA
	$T_{\text{MAX}}$		5		600	pA
<b>INPUT OFFSET CURRENT</b>						
	$T_{\text{MIN}}$	$\pm 5\text{ V}$		15	25	pA
Offset Current Drift	$T_{\text{MAX}}$		5		280	pA
						pA
<b>OPEN-LOOP GAIN</b>						
	$V_{\text{OUT}} = \pm 2.5$	$\pm 5\text{ V}$				dB
	$R_{\text{LOAD}} = 500\ \Omega$		64	66		dB
	$R_{\text{LOAD}} = 150\ \Omega$		64	66		dB
<b>COMMON-MODE REJECTION</b>						
	$V_{\text{CM}} = \pm 2\text{ V}$	$\pm 5\text{ V}$	69	80		dB
<b>INPUT VOLTAGE NOISE</b>						
	$f = 10\text{ kHz}$	$\pm 5\text{ V}$		12		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT CURRENT NOISE</b>						
	$f = 10\text{ kHz}$	$\pm 5\text{ V}$		10		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT COMMON-MODE VOLTAGE RANGE</b>						
		$\pm 5\text{ V}$		$\pm 3.5$		V
<b>OUTPUT VOLTAGE SWING</b>						
	$R_{\text{LOAD}} = 500\ \Omega$		+3.2	$\pm 3.4$		V
	$R_{\text{LOAD}} = 150\ \Omega$	$\pm 5\text{ V}$	+3.1	$\pm 3.2$		V
Output Current		$\pm 5\text{ V}$	50			mA
Short-Circuit Current				80		mA
<b>INPUT RESISTANCE</b>						
				$5 \times 10^{11}$		$\Omega$
<b>INPUT CAPACITANCE</b>						
				6		pF
<b>OUTPUT RESISTANCE</b>						
	Open Loop			8		$\Omega$
<b>POWER SUPPLY</b>						
Quiescent Current		$\pm 5\text{ V}$		6.2	6.8	mA
	$T_{\text{MIN}}$ to $T_{\text{MAX}}$	$\pm 5\text{ V}$			7.5	mA
<b>POWER SUPPLY REJECTION</b>						
	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$		76	88		dB

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18$ V
Internal Power Dissipation <sup>1</sup>	
Small Outline (R)	See Figure 6
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	See Figure 6
Storage Temperature Range (R-8, RW-16)	$-65^\circ\text{C}$ to $+125^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Lead Temperature Range (Soldering 10 sec)	$300^\circ\text{C}$

<sup>1</sup> Specification is for device in free air:  
 8-lead SOIC package:  $\theta_{JA} = 155^\circ\text{C}/\text{W}$   
 16-lead SOIC package:  $\theta_{JA} = 85^\circ\text{C}/\text{W}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONFIGURATIONS

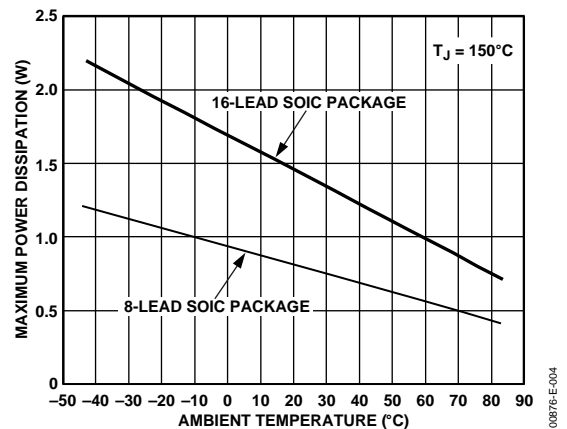
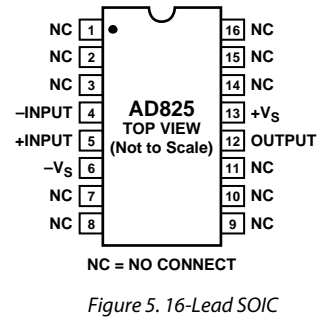
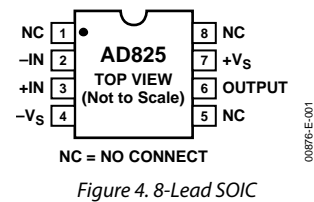


Figure 6. Maximum Power Dissipation vs. Temperature

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

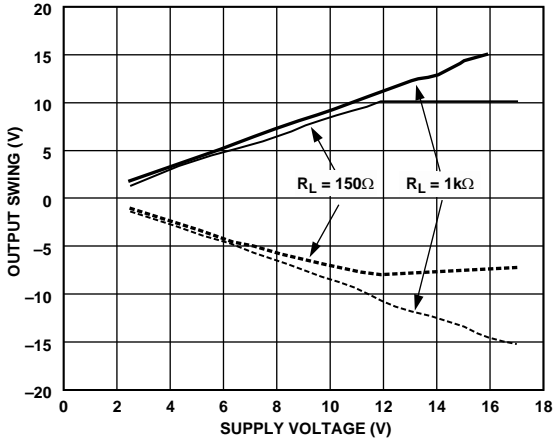


Figure 7. Output Voltage Swing vs. Supply Voltage

00876-E-005

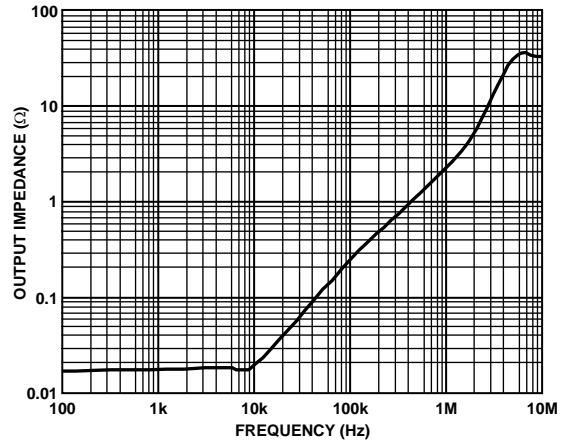


Figure 10. Closed-Loop Output Impedance vs. Frequency

00876-E-008

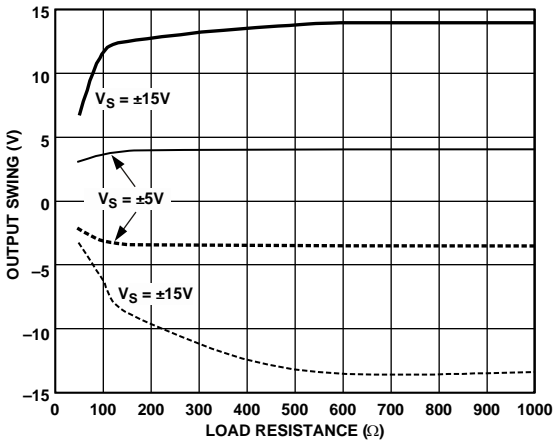


Figure 8. Output Voltage Swing vs. Load Resistance

00876-E-006

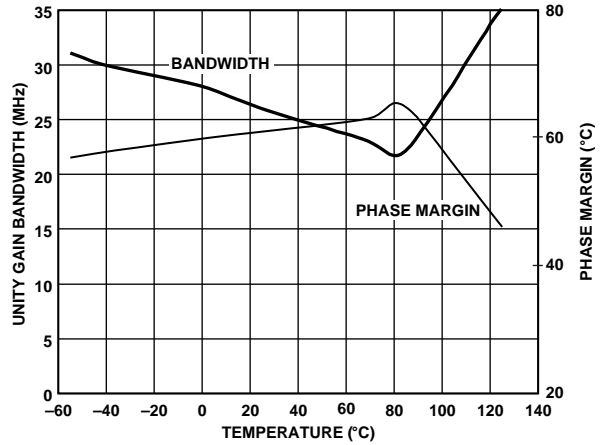


Figure 11. Unity Gain Bandwidth and Phase Margin vs. Temperature

00876-E-009

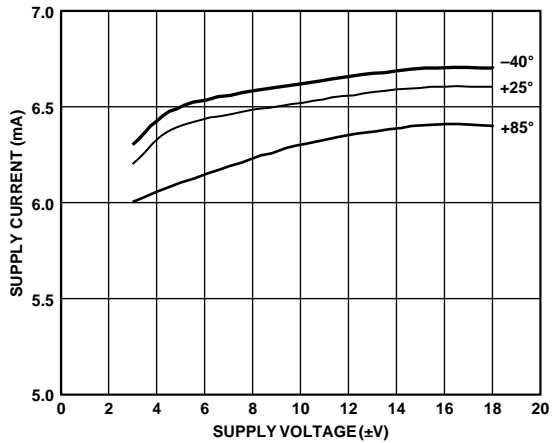


Figure 9. Quiescent Supply Current vs. Supply Voltage for Various Temperatures

00876-E-007

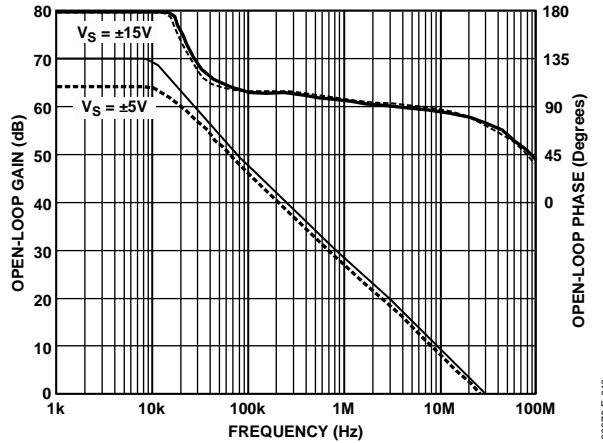


Figure 12. Open-Loop Gain and Phase Margin vs. Frequency

00876-E-010



Figure 13. Open-Loop Gain vs. Load Resistance



Figure 16. Large Signal Frequency Response;  $G = +2$

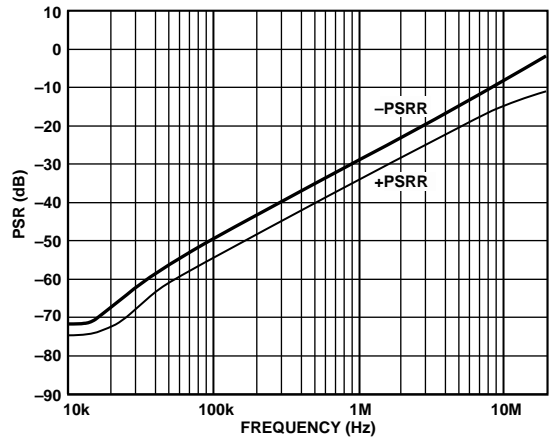


Figure 14. Power Supply Rejection vs. Frequency

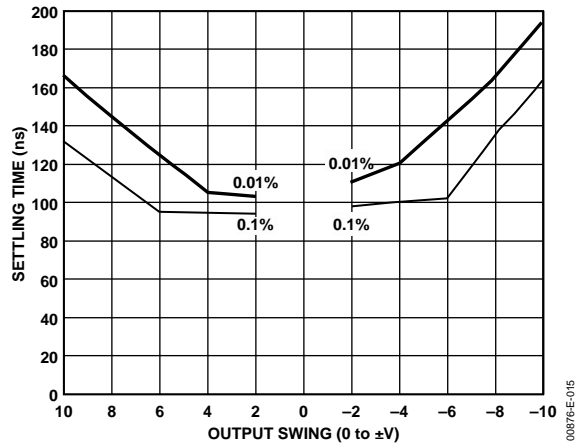


Figure 17. Output Swing and Error vs. Settling Time

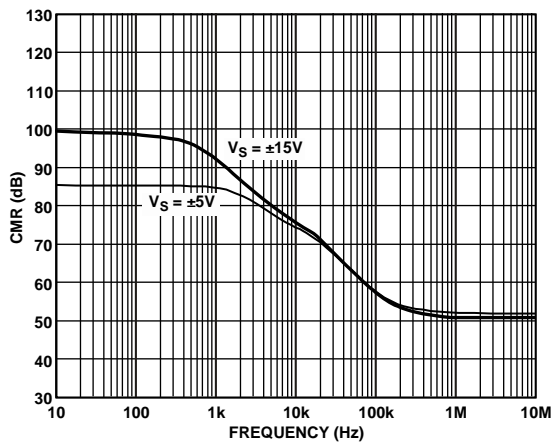


Figure 15. Common-Mode Rejection vs. Frequency

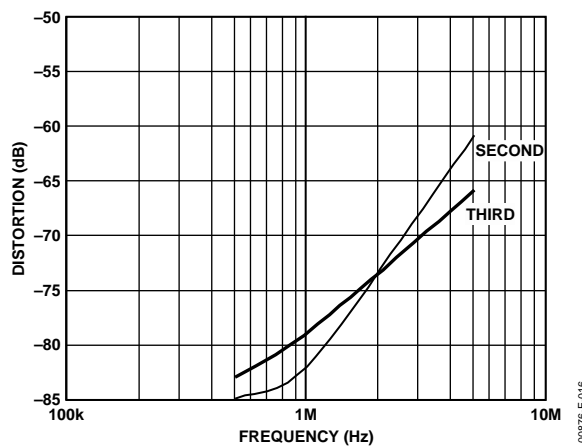


Figure 18. Harmonic Distortion vs. Frequency

# AD825

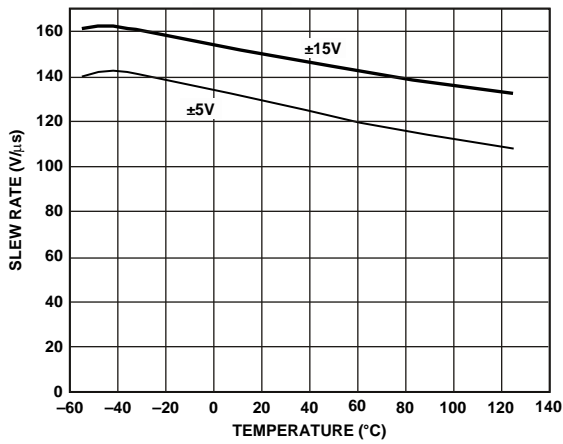


Figure 19. Slew Rate vs. Temperature

00876-E-017

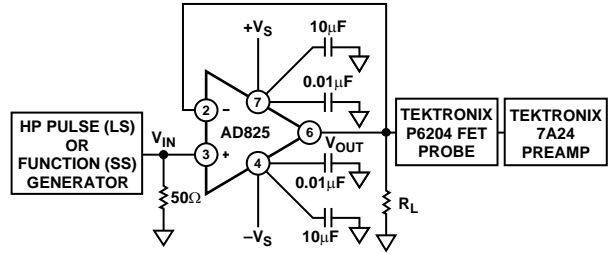


Figure 22. Noninverting Amplifier Connection

00876-E-020

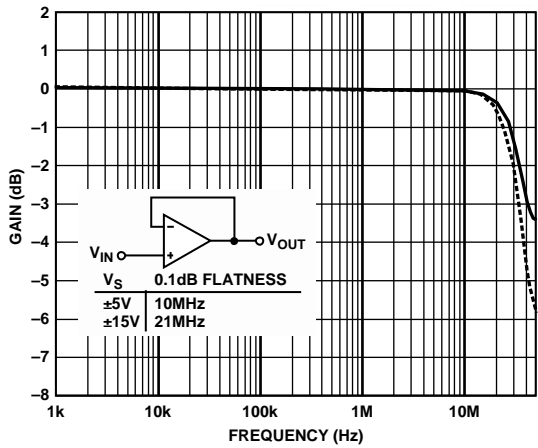


Figure 20. Closed-Loop Gain vs. Frequency, Gain = +1

00876-E-018

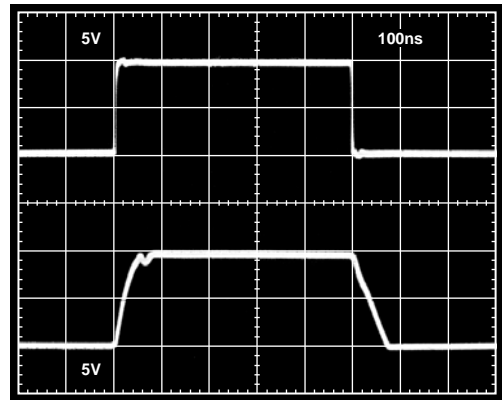


Figure 23. Noninverting Large Signal Pulse Response,  $R_L = 1\text{ k}\Omega$

00876-E-021

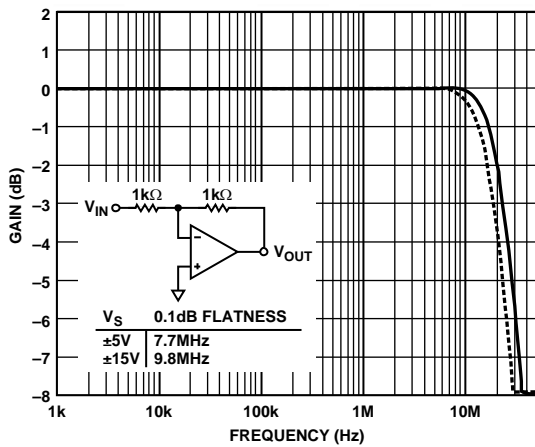


Figure 21. Closed-Loop Gain vs. Frequency, Gain = -1

00876-E-019

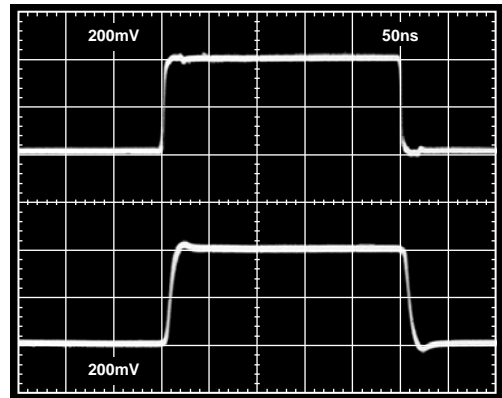


Figure 24. Noninverting Small Signal Pulse Response,  $R_L = 1\text{ k}\Omega$

00876-E-022





Figure 25. Noninverting Large Signal Pulse Response,  $R_L = 150\ \Omega$



Figure 28. Inverting Large Signal Pulse Response,  $R_L = 1\ \text{k}\Omega$



Figure 26. Noninverting Small Signal Pulse Response,  $R_L = 150\ \Omega$



Figure 29. Inverting Small Signal Pulse Response,  $R_L = 1\ \text{k}\Omega$

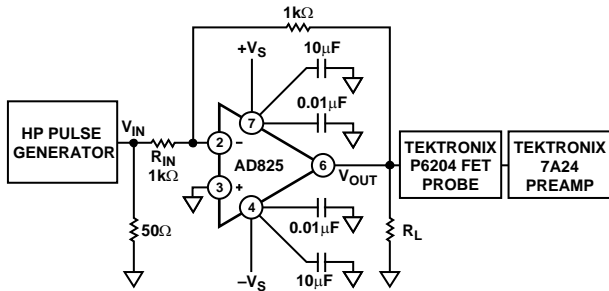


Figure 27. Inverting Amplifier Connection

## DRIVING CAPACITIVE LOADS

The internal compensation of the [AD825](#), together with its high output current drive, permits excellent large signal performance while driving extremely high capacitive loads.

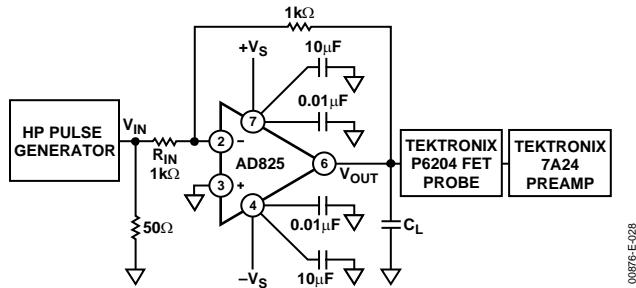


Figure 30. Inverting Amplifier Driving a Capacitive Load

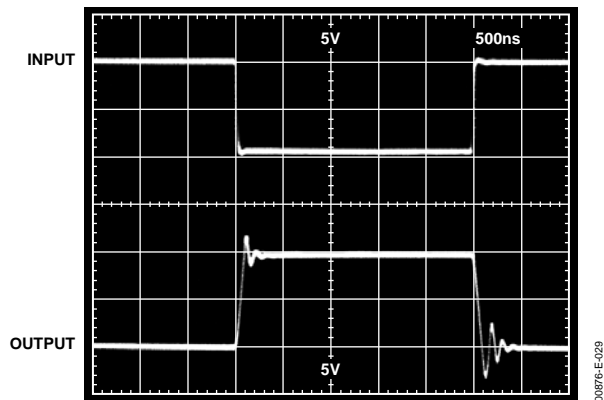


Figure 31. Inverting Amplifier Pulse Response While Driving a 400 pF Capacitive Load

## THEORY OF OPERATION

The [AD825](#) is a low cost, wideband, high performance FET input operational amplifier. With its unique input stage design, the [AD825](#) ensures no phase reversal, even for inputs that exceed the power supply voltages, and its output stage is designed to drive heavy capacitive or resistive loads with small changes relative to no load conditions.

The [AD825](#) (Figure 32) consists of common-drain, common-base FET input stage driving a cascoded, common-base matched NPN gain stage. The output buffer stage uses emitter followers in a Class AB amplifier that can deliver large current to the load while maintaining low levels of distortion.

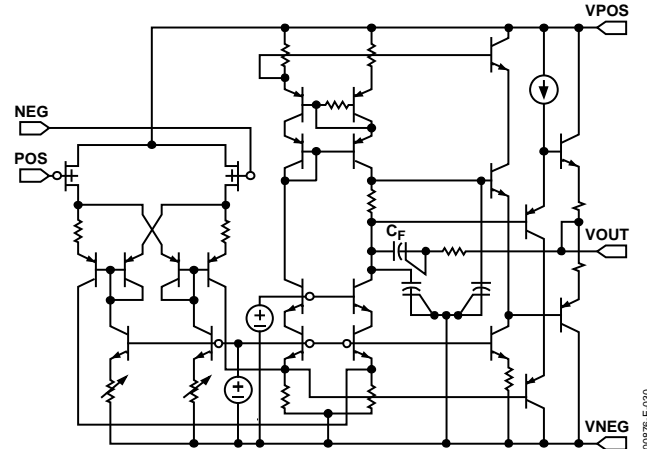


Figure 32. Simplified Schematic

The capacitor,  $C_F$ , in the output stage, enables the [AD825](#) to drive heavy capacitive loads. For light loads, the gain of the output buffer is close to unity,  $C_F$  is bootstrapped, and not much happens. As the capacitive load is increased, the gain of the output buffer is decreased and the bandwidth of the amplifier is reduced through a portion of  $C_F$  adding to the dominant pole. As the capacitive load is further increased, the amplifier's bandwidth continues to drop, maintaining the stability of the [AD825](#).

### INPUT CONSIDERATION

The [AD825](#) with its unique input stage ensures no phase reversal for signals as large as or even larger than the supply voltages. Also, layout considerations of the input transistors ensure functionality even with a large differential signal.

The need for a low noise input stage calls for a larger FET transistor. One should consider the additional capacitance that is added to ensure stability. When filters are designed with the [AD825](#), one needs to consider the input capacitance (5 pF to 6 pF) of the [AD825](#) as part of the passive network.

### GROUNDING AND BYPASSING

The [AD825](#) is a low input bias current FET amplifier. Its high frequency response makes it useful in applications, such as photodiode interfaces, filters, and audio circuits. When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnects, and resistances should have low inductive paths to ground. Power supply leads should be bypassed to common as close as possible to the amplifier pins. Ceramic capacitors of 0.1  $\mu$ F are recommended.

**SECOND-ORDER LOW-PASS FILTER**

A second-order Butterworth low-pass filter can be implemented using the AD825 as shown in Figure 33. The extremely low bias currents of the AD825 allow the use of large resistor values and, consequently, small capacitor values without concern for developing large offset errors. Low current noise is another factor in permitting the use of large resistors without having to worry about the resultant voltage noise.

With the values shown, the corner frequency will be 1 MHz. The equations for component selection are shown below. Note that the noninverting input (and the inverting input) has an input capacitance of 6 pF. As a result, the calculated value of C1 (12 pF) is reduced to 6 pF.

$$C1 = \frac{1.414}{2\pi f_{CUTOFF} R1}$$

$$C2 (farads) = \frac{0.707}{2\pi f_{CUTOFF} R1}$$

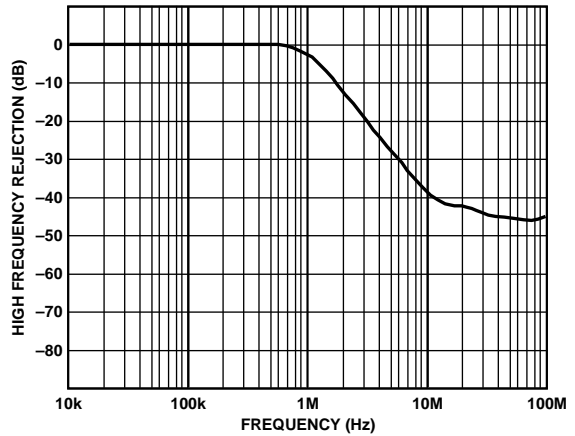
$$R1 = R2 = \text{User Selected (Typically } 10 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega)$$

A plot of the filter frequency response is shown in Figure 34; better than 40 dB of high frequency rejection is provided.



00876-E-031

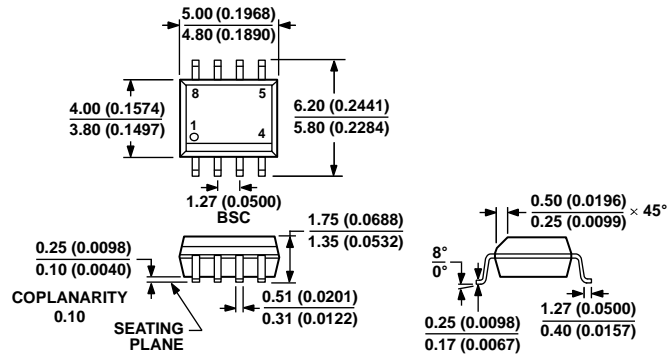
Figure 33. Second-Order Butterworth Low-Pass Filter



00876-E-032

Figure 34. Frequency Response of Second-Order Butterworth Filter

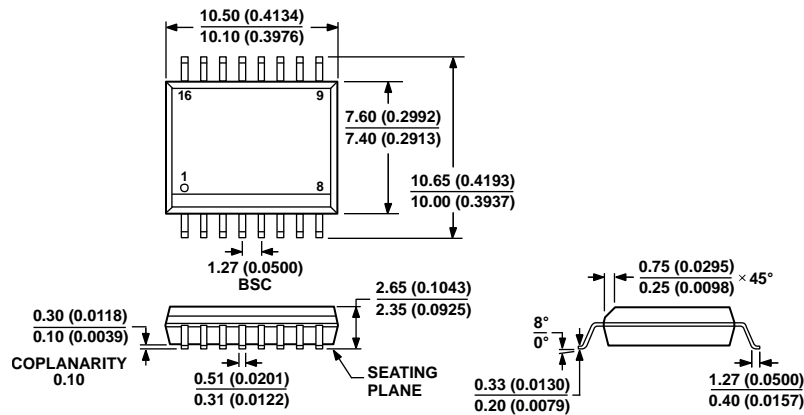
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC]  
Narrow Body (R-8)  
Dimensions shown in millimeters (inches)

012407-A



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 16-Lead Standard Small Outline Package [SOIC\_W]  
Wide Body (RW-16)  
Dimensions shown in millimeters (inches)

03-27-2007-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD825ARZ	-40°C to +85°C	8-Lead SOIC_N	R-8
AD825ARZ-REEL	-40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD825ARZ-REEL7	-40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD825ARZ-16	-40°C to +85°C	16-Lead SOIC_W	RW-16
AD825ARZ-16-REEL	-40°C to +85°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16
AD825ARZ-16-REEL7	-40°C to +85°C	16-Lead SOIC_W, 7" Tape and Reel	RW-16
AD825AR-EBZ		Evaluation Board	
AD825ACHIPS		Die	

<sup>1</sup> Z = RoHS Compliant Part.